Application Note

VSC8664 and Zarlink ZL30138 and ZL30143 SyncE Interoperability Test Results

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Revision 1.1 of this document was published in October 2010. In revision 1.1, Zarlink ZL30143 test results were included.

1.2 Revision 1.0

Revision 1.0 of this document was published in September 2010. This was the first publication.

2 Introduction

Synchronous Ethernet (SyncE) support is a relatively new initiative for the Carrier Ethernet industry due to the push for expanding the telecom infrastructure into the packet network. SyncE facilitates primary timing propagation through physical links between each of the Carrier Ethernet nodes. SyncE depends on Ethernet PHY devices to provide the ability to recover the line clock from the connection to a distant connection or link partner. The goal of the testing outlined in this document is to assess the typical use model of two popular devices used as the basis for a SyncE system utilizing the Vitesse VSC8664 PHY and the Zarlink ZL30138 system synchronizer and timing devices. The information presented here is to be taken as a demonstration of interoperability between the two devices in a SyncE application, not a guarantee of performance in a given user environment.

A subset of the same SyncE interoperability tests were performed with the Zarlink ZL30143 System Synchronizer/SETS. These tests, combined with results derived from ZL30138 testing, were deemed sufficient for full test coverage.

Note: In this document, references are made to Zarlink part numbers beginning with ZL and others beginning with ZLE. ZL part numbers refer to the actual Zarlink system synchronizer devices, while ZLE part numbers refer to the evaluation boards that contain those devices.

2.1 References

2.1.1 Vitesse Documents

- VSC8664 Datasheet - Rev 4.1, 06/10/2009 (http://www.vitesse.com/products/download.php?fid=3947&number=VSC8664)
- Application Note: “The VSC8664 in Synchronous Ethernet Applications” - Rev 1.0, 05/27/2008 (http://www.vitesse.com/products/download.php?fid=3975&number=VSC8664)
- VSC8664 Evaluation Platform - Rev 1.0, 03/06/2008 (http://www.vitesse.com/products/download.php?fid=3946&number=VSC8664)

2.1.2 Zarlink Product Profiles

- ZL30138: OC-192/STM-64 SONET/SDH/10GbE Stratum 2/3/3E System Synchronizer/SETS (http://www.zarlink.com/zarlink/hs/82_ZL30138.htm)
- ZL30143: SyncE SONET/SDH G.8262/Stratum3 System Synchronizer/SETS (http://www.zarlink.com/zarlink/hs/82_ZL30143.htm)

3 Test Case Overview

3.1 Scope of Test Case

The test case chosen as a typical application contains the following.

- 25 MHz system clocking
- Copper media interface for recovering link partner clock
- Copper media test loop for validating

3.2 Test Components

3.2.1 Vitesse Materials

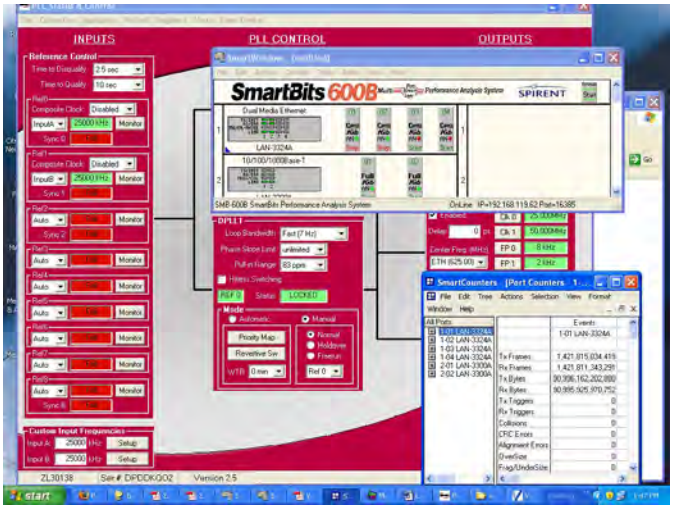
- VSC8664 Evaluation Board
- VSC8664 Control GUI (See the following figure)

Figure 1 • VSC8664 Evaluation Board GUI

3.2.2 Zarlink Materials

- ZLE30138 OC-192/STM-64 SONET/SDH/10GbE/1GbE Stratum 2/3/3E System Synchronizer Evaluation Board (also known as, ZLE30138 Evaluation Board)
- ZLE30116A Base Board
- ZLE30117 Mezzanine Board
- SYNCHRONIZATION EVALUATION SYSTEM GUI (See the following figure)

Figure 2 • ZLE30138 Evaluation System GUI



3.2.3 Test Equipment

- PC: Dell OptiPlex 745, Win XP, used for USB and Ethernet control of boards through GUIs
- Power Supply: Tektronix PS2512G, used for board supply
- Frequency Counter: Leader LF826, used for frequency accuracy
- Oscilloscopes: Tektronix TDS3054, used to observe clock behavior, and Tektronix DPO 7354 with Jitter analysis
- Copper Ethernet traffic generator: Spirent SmartBits 600B with cards LAN-3302A and LAN-3300A
- Jitter Analyzer: LeCroy SDA 5000 Serial Data Analyzer

3.2.4 Test Configuration

The system test setup consisting of the Vitesse VSC8664 and Zarlink ZLE30138 evaluation boards and associated test equipment is shown in the following figures. Control of both evaluation boards is maintained by the external PC by means of the board GUIs shown above. For Zarlink ZL30143 testing, the system test setup consisting of the Vitesse VSC8664 and Zarlink ZLE30143 evaluation boards with the associated test equipment is the same. J24 (Recover Clk 1), J25 (Recover Clk 2), and J26 (ext clk) on the VSC8664 evaluation board were connected to J5 (REF 0), J9 (REF 1), and J24 (SDHCLK0).

Figure 3 • Test Configuration Block Diagram

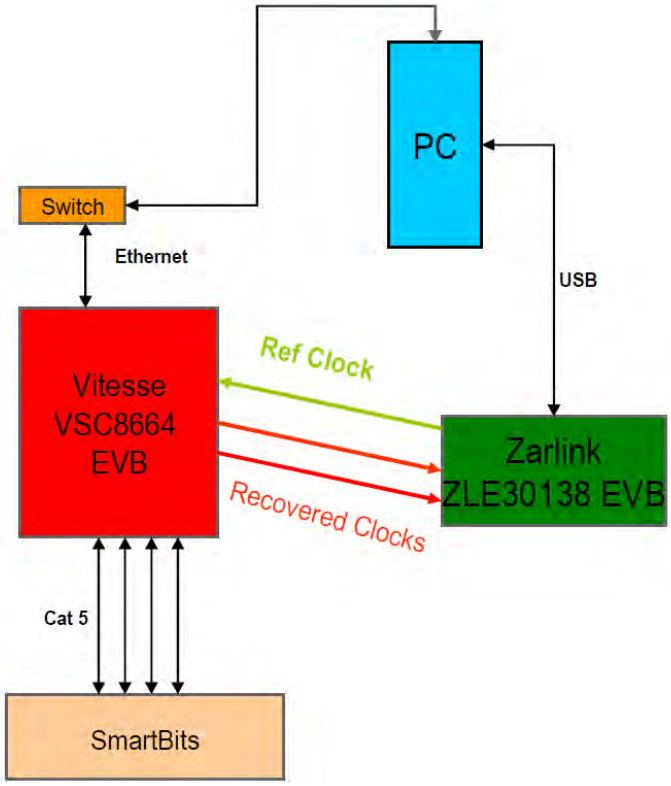
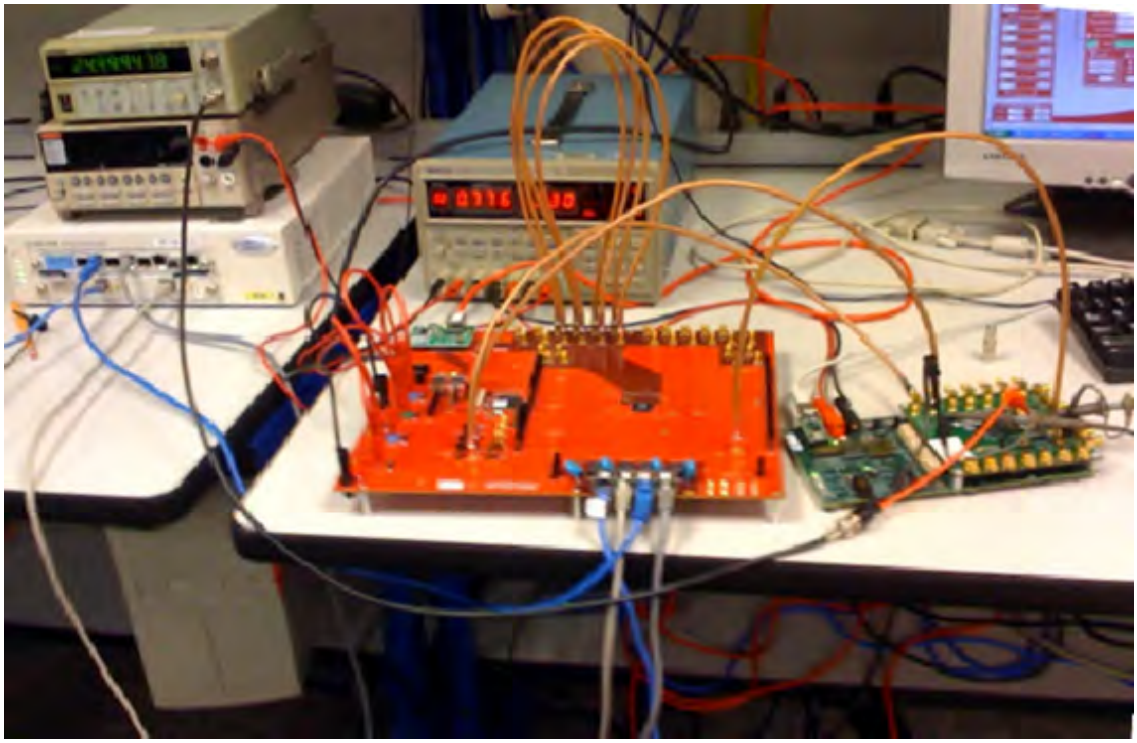


Figure 4 • Test Configuration Bench Setup



3.2.5 VSC8664 Evaluation Board Configuration

The following configuration parameters are established through the VSC8664 Evaluation Board GUI.

- PHY configuration EXT 25 MHz, Media Interface Cat 5
- Micro Page Controls: set Reg 23:15, 0 to enable recovered clock on PHY 0 output based on copper
- Micro Page Controls: set Reg 24:15, 12, 0 to enable recovered clock on PHY 0 output based on copper
- MII Registers: set Reg 9:12 to enable slave configuration and then Reg 0:9 to restart auto negotiation (for PHY 0 and PHY 1)

Using the GUI to set the Micro page Control and MII register.

- Recover Clk 1: Set Reg 23G bit 15 = 1, to enable the recover clock 1
- Recover Clk 2: Set Reg 24G bit 15 = 1, to enable the recover clock 2
- Set recovered clock PHY and media. Set the Register 23G and 24G bit 13:12 and 1:0. For this test it was set it to: 10, 01 for 23G and 11, 01 for 24G
- Set the MII Register 9 bit 12 to enable the Master/Slave Manual Configuration and Register 0 bit 9 to restart auto-negotiation

3.2.6 ZLE30138 Evaluation Board Configuration

The following configuration parameters are established through the Zarlink PLL Status and Control GUI.

OUTPUTS, SONET/SDH/Ethernet APLL

- Set Center Freq to ETH(625)
- Set Clk 0 MHz to 25 MHz
- Check Enabled
  PLL CONTROL, DPLL1
- Mode Automatic
- Loop Bandwidth 14 Hz

INPUTS

- Ref0 set 25000 kHz and InputA
- Ref1 set 25000 kHz and InputB
- Custom Input Frequency - Input A: Set 25000 kHz, In Custom Input A Configuration: Reference Divider 1, Custom Multiplier 3125, Custom Input Locks to : 25000 kHz, SCM: low limit 20 ns – high limit 60, CFM: low limit 19888 ns – High Limit 21112 ns - # Cycles Monitored 128 – check CFM Divides Input By 4
- Custom Input Frequency - Input B: Set 25000 kHz, In Custom Input B Configuration: Reference Divider 1, Custom Multiplier 3125, Custom Input Locks to : 25000 kHz, SCM: low limit 20 ns – high limit 60, CFM: low limit 19888 ns – High Limit 21112 ns - # Cycles Monitored 128 – check CFM Divides Input By 4

4 Testing Procedure

4.1 Basic Operation

Using the setup described, check to ensure that all control GUIs display the correct values. This serves as the necessary starting point for the testing that follows.

4.2 Breaking Links and Auto Configuration

In this test, the four states of synchronization between the Zarlink and Vitesse parts are tested:

1. Sync REF0: the Zarlink device synchronizes with the Vitesse Recovered Clock 0 from port 0 connected to SmartBits
2. Sync REF1: REF0 is disconnected, Zarlink should shift to REF1 from port 1 recovered clock connected to SmartBits
3. Holdover: REF1 is disconnected (REF 0 still disconnected), Zarlink should stay locked to the previous sync state
4. Freerun: with no sync information Zarlink should produce requested frequency

In the various state changes listed above, the SmartBits display should be observed for possible errors or data transfer irregularities. The oscilloscope should also be monitored for possible loss of sync.

The following actions should then be taken to complete the link break testing.

- Connect the Vitesse PHY 2 and 3 MAC sides together to the SmartBits unit and monitor for transfer error and correct transfer quantities
- Randomly reconnect and disconnect to the various states and check for error

4.3 Long Run Testing

Observe SmartBits error and transfer stability and check for steady state operation over the course of many days.

4.4 Pass/Fail Criteria

A dual strategy is used for most tests to determine if they pass or fail.

1. SmartBits – Data and error counters data transfers must match on loop tests. No errors can be detected.
2. Scope sync or disruption.

Accurate frequency and sync between PHY recovered clock and PLL ref clock

4.5 Measurements

The following measurements are reported in the next section.

1. Jitter – Measure the jitter from the Zarlink platform
2. Frequency Accuracy – Measure Zarlink accuracy to reference

5 Test Results

Test results and measurements (obtained at Vitesse in-house lab facilities for the test configuration described previously) are reported in this section.

5.1 Basic Tests

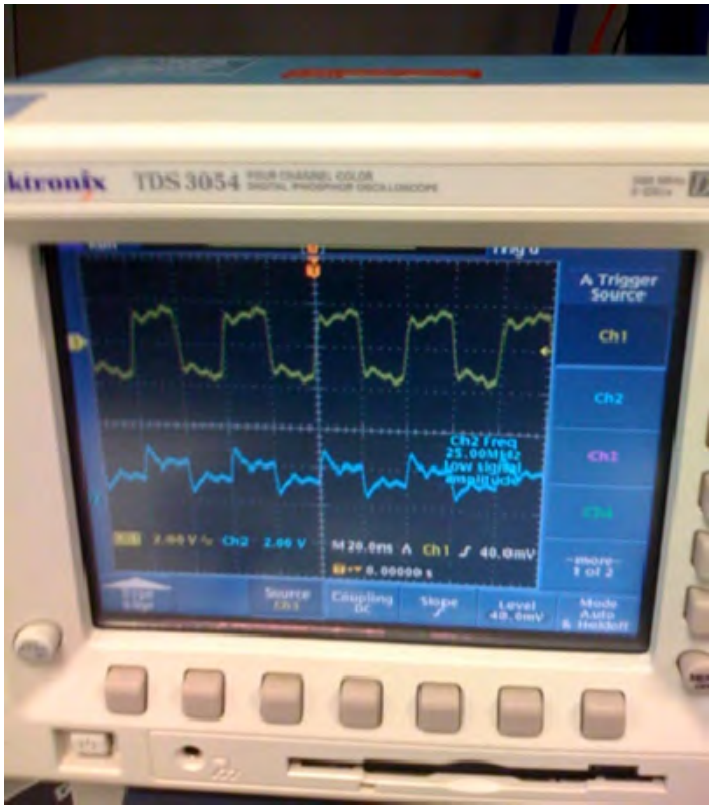
The results obtained for basic operation, recovery from link-breakage, and long run testing are listed as follows:

Table 1 • Test Results of ZL30138 with VSC8664

Test	Result	Comment
Basic Operation	Passed	Ref 0 used
Break Primary Reference	Passed	Ref 1 used
Break Secondary Reference	Passed	Holdover mode
Breaking Links and Auto configuration	Passed	Free-running mode
Random disconnects and connects	Passed	
Long Run Testing	Passed	Length of data through the system with no error: Number of Frames: 1, 421, 815, 034, 419 Number of Bytes: 90, 996, 162, 202, 880

Oscilloscope monitoring of the VSC8664 PHY recovered clock and the ZLE30138 PLL reference clock was maintained during testing with no loss in synchronization or frequency accuracy observed. (See the following figure)

Figure 5 • Oscilloscope Frequency and Sync Monitoring



5.2 Measurements

5.2.1 Jitter

Clock jitter measurements were performed on the clock output from the Zarlink platform. Results are listed as follows:

LeCroy Jitter Tektronix 7354

408.13ps p-p

Table 2 • Jitter Measurements

Population	711156
Median	25.000 MHz
StdDev	8.1136 kHz
Max	25.046 MHz
Min	24.954 MHz
Pk-Pk	92.506 kHz
Max+delta	91.267 kHz
Max-delta	-69.191 kHz

5.2.2 Frequency Accuracy

The measurements taken in the initial state are listed as follows:

Table 3 • Frequency Accuracy Measurements

Clock Source	Frequency (MHz)
Recovered Clock 1*	24.999482
Recovered Clock 2	24.999840
Zarlink Clock*	24.999482
Zarlink Holdover Mode*	24.999482
Zarlink Freerun	24.999991

Notes:

1. The SmartBits connection clock is recovered by Clock 1. It is not exactly 25.000000 MHz.
2. Zarlink provides a frequency back of exactly the same value to the accuracy of the frequency meter.
3. When both Recovered Clocks 1 and 2 are removed Zarlink stays at the last synchronization as shown by the Holdover Mode Value.
4. Zarlink provides the most accurate frequency when it runs without synchronization information in Freerun mode.

6 Design Considerations

6.1 Fast Link Failure Output

The VSC8664 has a quick signal for indication of loss of link called FastFailOver. This signal will occur in less than 1 ms where the IEEE 802.3 standard minimum loss of signal is 750 ms for a Master and 350 ms for a slave. A system designer might use this signal to aid in switching clock sources when there is a loss of link.

6.2 Zarlink Operation Modes

A designer of a SyncE application should consider clocking in all possible situations. The Zarlink control GUI demonstrates a very important feature called “Holdover”. Holdover is the mode transitioned to when all references are lost. The Zarlink device will attempt to keep the same synchronization as the last reference. The experience in this testing was that it performed this function successfully.

6.3 PLL Configuration

It was noted during the testing that selecting PLL configuration values could cause subtle errors that resulted in overnight stress testing failures. The failure rate was beneath the specification level. Care should be taken in configuring PLLs. Stability testing should be done to validate the configuration. In tests running eight or more hours, a couple of CRC errors were detected by SmartBits when the ZLE30138 configuration values were not set correctly.

7 Testing with the Zarlink ZLE30143

VSC8664 was tested with the Zarlink ZLE30143 validation board in a similar manner to the ZLE30138.

Table 4 • Jitter Measurements: ZLE30143

Population	777386	777386
Median	40.000 ns	25.000 MHz
StdDev	11.308 ps	
Max	40.067 ns	24.958 MHz
Min	39.940 ns	25.038 MHz
Pk-Pk	127.49 ps	79.361 kHz
Max+delta	102.12 ps	
Max-delta	-119.04 ps	

Note: Measurements using Tektronix TDS7404

Table 5 • Test Results of ZLE30143 with VSC8664

Test	Result	Comment
Basic Operation	Passed	Ref 0 used
Break Primary Reference	Passed	Ref 1 used
Break Secondary Reference	Passed	Holdover mode
Random disconnects and connects	Passed	
Long Run Testing	Passed	Length of data through the system with no error: Number of Frames: 268,585,726,724 Number of Bytes: 17189486510336

8 Conclusion

The results presented here confirm the basic interoperability between the Vitesse VSC8664 Ethernet PHY and Zarlink ZL30138 PLL and Zarlink ZL30143 PLL synchronizer for SyncE operation at 25 MHz.

Note that that these results were taken under normal laboratory conditions, and in no way replace or extend beyond the product specification information provided in the applicable device datasheets.

Future testing is to include 125 MHz operation, 100BT, SerDes media testing, and noise injection for jitter tolerance evaluation.

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