
AVR32804: Migration from the UC3 B series to the UC3 D series



Features

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- Pinout Comparison
- Migration with the Atmel® AVR® Software Framework

1 Introduction

This application note is a guide to assist current Atmel UC3 B devices users in converting existing designs to the Atmel UC3 D devices.

For detailed information on these products, please refer to the datasheets, available on the Atmel web site.

UC3 B series is made of AT32UC3B{0,1}{64,128,256,512} part numbers.

UC3 D series is made of ATUC{32,64,128}D{3,4} part numbers.

32-bit Atmel Microcontrollers

Application Note

Rev. 32141A-AVR-12/11





2 Features Comparison

Some considerations need to be taken care of when using UC3 B series before migrating to UC3 D series.

Some of the features present on the UC3 B are not present or have a different implementation on the UC3 D. The main differences are detailed in the table below.

The column 'successful migration' explicitly mentions the conditions for a successful UC3 B to UC3 D migration.

Table 2-1. Differences between the UC3 B series and the UC3 D series

Module		UC3 B Series	UC3 D Series	Conditions for a Successful migration
Peripheral	GPIO function multiplexing functions	For UC3Bx512 only, the function D is available to select GPIO alternate functions.	GPIO function D is not available	For UC3Bx512 only, do not use the alternate function D of the GPIOs
	Pulse with Modulation (PWM) Channels	7 programmable centered or left-aligned channels with 20-bit counter, with individual period	7 Left-aligned non-inverted channels with 12-bit counter. All channels share the same counter. Each duty cycle can be set independently	Do not use centered channels Do not use the full 20-bit of the counter Use the same counter configuration for all channels
	USART in Modem mode	Yes on USART1	No	Do not use the Modem mode of the USART1
	Synchronous Serial Controller (SSC)	Capable of I2S protocol	Dedicated I2S controller	Use the SSC in I2S mode only. Do not use SSC receiver (RX) and transmitter (TX) simultaneously Do not connect a clock on the SSC RX to synchronize the SSC TX flow
	GPIO input glitch filter	Yes	No	Do not use the GPIO glitch filter
	Crystal Oscillator Input	2 (OSC0 and OSC1)	1 (OSC0)	Do not use OSC1
	USB	Dedicated 960 Bytes for USB endpoints/pipes	Endpoints/pipes memory allocation in internal CPU RAM memory	Reserve the same amount of RAM used for endpoints/pipes memory in internal RAM
		Dedicated USB DMA	No dedicated USB DMA	Do not use the USB DMA
		Mini-Host+Device	Device	Do not use the mini-host
	ABDAC	Yes, on AT32UC3Bx512 only.	No	Do not use the ABDAC
CPU	Memory Protection Unit (MPU)	Yes	No	Do not use the MPU

Module		UC3 B Series	UC3 D Series	Conditions for a Successful migration
	Maximum Frequency of CPU/HSB	60MHz	48MHz.	Do not use CPU/HSB frequency higher than 48MHz
Flash	Flash memory controller	Dual-bank. 0 wait state up to 30MHz Page size 512Bytes	Single bank. 0 wait state up to 24MHz Page size 256Bytes	Do not use 0 wait state with frequencies higher than 24MHz Write page-size independent code
OCD	Nexus On-chip Debug System Trace on Auxiliary port	Yes	No	Do not use Nexus OCD trace
	JTAG Debug mode entry with TCK pin	JTAG interface is enabled when TCK pin is tied low	The JTAG is enabled if TCK is low while the RESET_N pin is released	Use the correct JTAG debug entry mode according to the device
Electrical	5V tolerant I/O	All I/O except TCK, PA11, PA12, PA18, PA19, PA28, PA29	PA09 (TWI SCL) , PA10 (TWI SCL), PB19 (USB-VBUS)	Do not use 5V tolerant on all I/O except PB19



3 Pinout Comparison

UC3 B and UC3 D series are pin-to-pin compatible, meaning you can safely replace an UC3 B device with an UC3 D device on a hardware design given the limitations listed in the following table.

3.1.1.1 IO

Table 3-1. UC3 B / UC3 D Pinout Comparison

QFP48 Pin	QFP64 Pin	UC3 B	UC3 D	Comment
6 42	8 56	VDDCORE VDDCORE	GPIO PB13 GPIO PB18	<u>On UC3 B design:</u> These 2 pins are VDDCORE pins. VDDCORE is the 1.8V core power supply input on the UC3 B. Has to be connected on VDDOUT (internal regulator output). <u>On UC3 D design:</u> These 2 pins can be used as regular GPIO pins <u>Conditions for a successful Migration:</u> Do not use the GPIO PB13 and PB18
41	53	VDDPLL	GPIO PB17	<u>On UC3 B design:</u> This pin is VDDPLL. VDDPLL is the input power supply (1.8V) for the PLL. <u>On UC3 D design:</u> This pin can be used a GPIO pins. <u>Conditions for a successful Migration:</u> Do not use the GPIO PB17
	41	PA28 / XIN1	GPIO PA28	<u>On UC3 B design:</u> PA28 / Oscillator 1 pin XIN1 <u>On UC3 D design:</u> PA28 <u>Conditions for a successful Migration:</u> Do not use oscillator 1
	42	PA29 / XOUT1	GPIO PA29	<u>On UC3 B design:</u> PA29 / Oscillator 1 pin XOUT1 <u>On UC3 D design:</u> PA29 <u>Conditions for a successful Migration:</u> Do not use oscillator 1
40	52	VBUS	PB17 - VBUS	<u>On UC3 B design:</u> This pin is a dedicated analog input for USB VBUS Monitor and OTG negotiation. <u>On UC3 D design:</u> PB17 is a 5V-tolerant GPIO, VBUS input is an alternate function of this GPIO. <u>Conditions for a successful migration:</u> Configure in software PB17 as an alternate function for VBUS.

3.1.1.2 Package

On the UC3 D series the QFN64 package center ground pad size is different from the UC3 B series.

Other packages are identical.

Fig 3-2. QFN64 Body 9.0x9.0mm – pitch 0.5mm

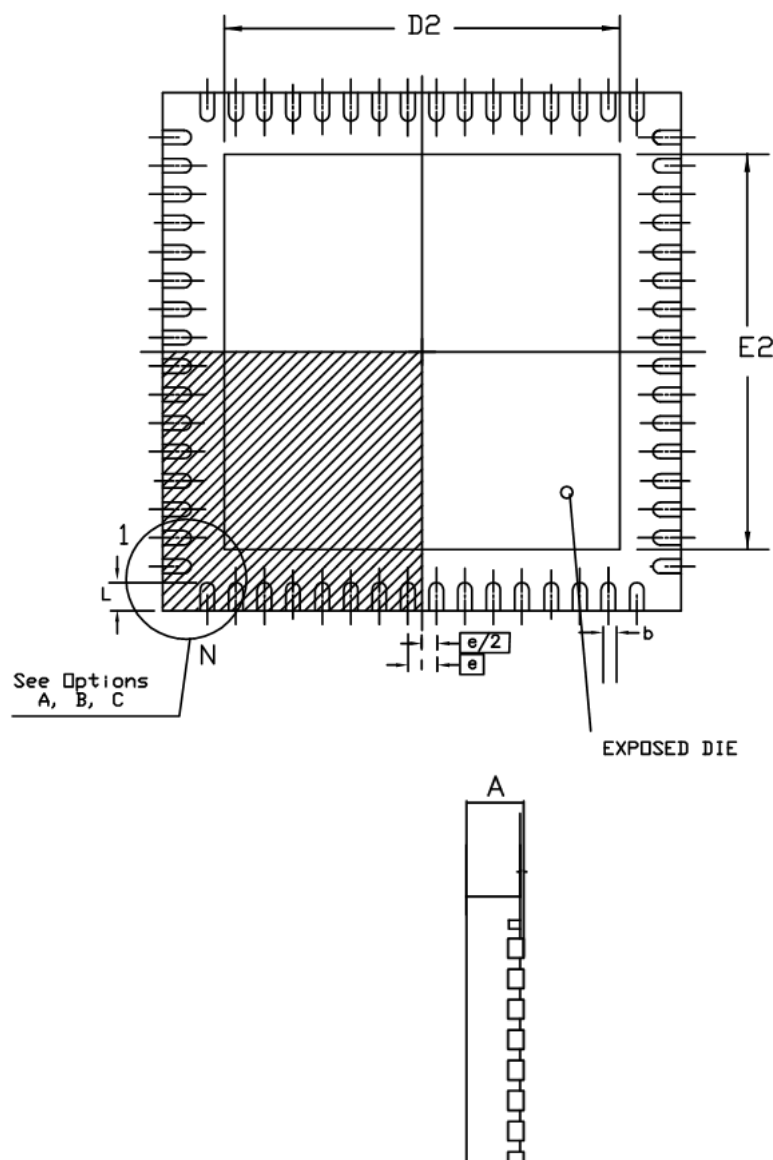




Table 3-3. QFN64 Packages Differences

Device	UC3 B			UC3 D			Conditions for a successful migration
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A (mm)	-	-	0.9	0.8	-	1.00	<u>Conditions for a successful migration:</u> No issue
D2 (mm)	5.55	5.65	5.75	5.30	5.40	5.50	<u>Conditions for a successful migration:</u> Design the hardware with the smallest D2 values i.e. the UC3 D one.
E2 (mm)	4.65	4.75	4.85	5.30	5.40	5.50	<u>Conditions for a successful migration:</u> Design the hardware with the highest E2 values i.e. the UC3 D one.
L (mm)	0.35	0.40	0.45	0.30	0.40	0.55	<u>Conditions for a successful migration:</u> No issue.

4 Porting Considerations

There are 3 major items to consider when migrating:

- Device differences,
- Support of the devices in the tools,
- Software design for compatibility. A driver abstraction layer is implemented in the Atmel AVR Software Framework to write a portable application.

4.1 Device Porting Considerations

4.1.1.1 Maximum Operating Frequency

The flash access provides different frequencies for each series.

The following table gives the maximum operating frequency:

Table 4-1. Maximum Operating Frequency

Device	Max CPU frequency with 0 wait-state	Max CPU frequency with 1 wait-state
UC3 B	30MHz	60MHz
UC3 D	24MHz	48MHz

Conditions for a successful migration: Do not set the operating frequency higher than 48MHz. Use the software framework software driver (FLASHCDW) to handle the 0 to 1 wait-state frequency.

4.1.1.2 Flash Controller: Page buffer Access

The flash memory has a write and erase granularity of one page; data is written and erased in chunks of one page. When programming a page, the user must first write the new data into the Page Buffer. The content of the entire page buffer is copied into the desired page in flash memory when the user issues the Write Page command.

When writing to the page buffer, a special care is required for UC3 D devices:

When writing data to the flash page buffer, the word with the low address must be written to the HSB bus before the word with the high address. To exemplify, to write a 64-bit value to double-word X0 residing in page X, first write a 32-bit word to the byte address pointing to address X0, thereafter write a word to the byte address pointing to address (X0+4). Refer to the UC3 D datasheet, in FLASHCDW section for more details.

Conditions for a successful migration: Use the software framework FLASHCDW software driver to handle the page buffer access.

4.1.1.3 Flash Fuses

The flash general purpose fuse register FGPFRL0 has a different bit implementation on UC3 B and UC3 D series.

Conditions for a successful migration: Use the software framework FLASHCDW software driver to handle the FGPFRL0 read and write access.

4.1.1.4 Flash User Page

On UC3 D series, the first word of the user page (address 0x80800000) is used for the watchdog timer auto-enable at startup configuration.

Conditions for a successful migration: Do not use the first word of the flash user page.

4.1.1.5 USB Controller

UC3 B and UC3 D series have a different USB controller:

Table 4-2. USB Controller differences

Device	USBB Controller	USBC Controller
UC3 B	On UC3 B, USB pipes/endpoints memory is located in the USB module by the 960 Bytes of Dual Port RAM. If several banks are used ("ping-pong" mode), then one DPRAM bank is read or written by the CPU or the DMA while the other is read or written by the USBB core.	-
UC3 D	-	On UC3 D, USB pipes/endpoints memory is located in the CPU RAM, and though need to be allocated when used. If several banks are used as ("ping-pong" mode), then one RAM bank is read or written by the CPU or the DMA while the other is read or written by the USBC core.

Figure 4-3. USBB Controller

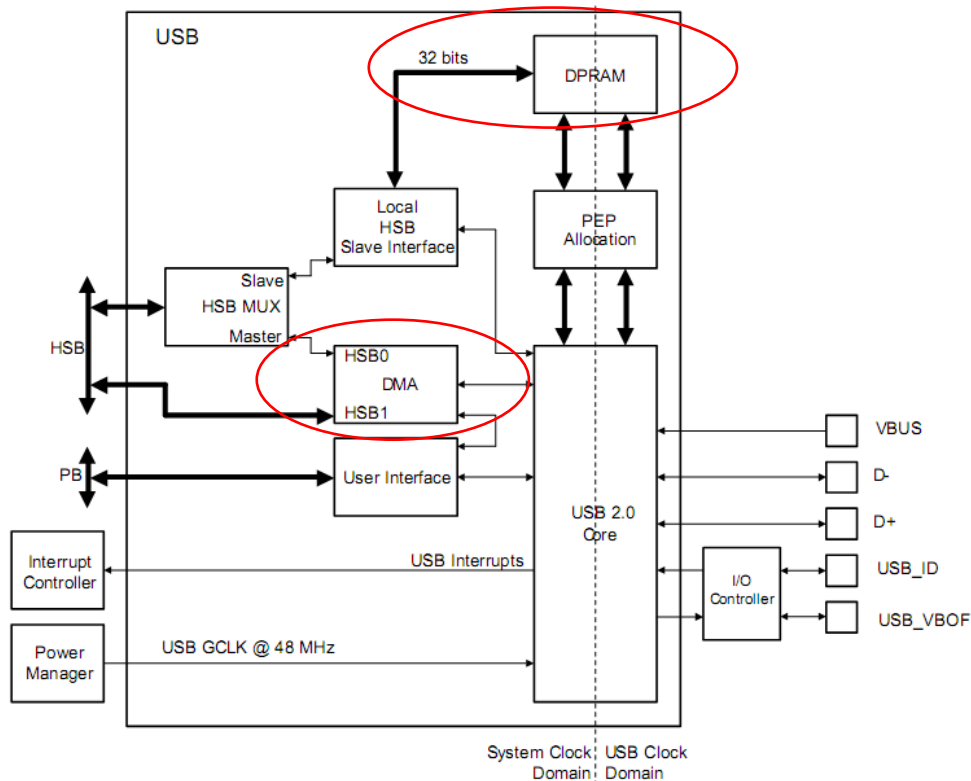
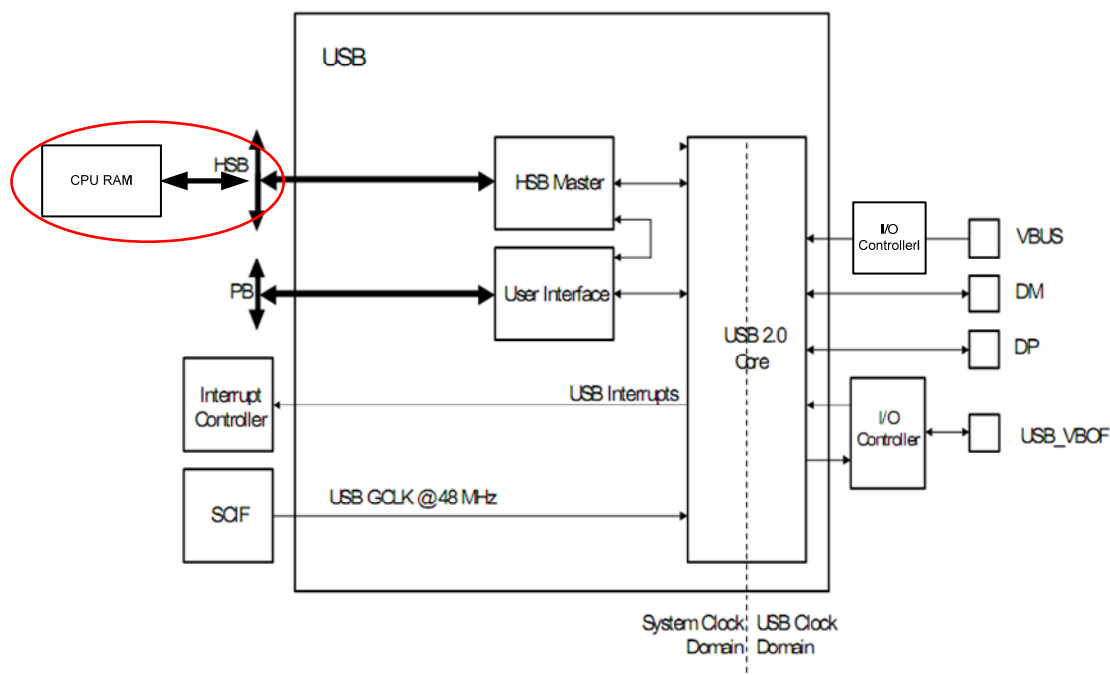


Figure 4-4. USBC Controller



Conditions for a successful migration:

- Use the software framework driver to handle the USB controller.
- Reserve a zone of size 960 Bytes in the CPU RAM.
- Do not use the USB DMA
- Do not use the USB mini-host feature.

4.1.1.6 USB Device Firmware Upgrade (DFU) Bootloader

UC3 B and UC3 D are shipped with a USB DFU bootloader.

On the UC3 B series, the USB DFU bootloader version 1.0.x uses 3 general-purpose fuses (FGPFRLO GP29, GP30, and GP31) and the last word of the flash user page.

On the UC3 D series, the USB DFU bootloader version 1.1.x does not use any of the general-purpose fuses and uses instead the last two words of the flash user page.

Conditions for a successful migration:

- Reserve the last 2 words of the flash user page for the USB DFU bootloader.
- When programming the flash with batchisp, adapt the batchisp command lines to match the part memory layout.
- The bootloader setup needs to be adapted:
 - On UC3 B devices, program the 3 general-purpose fuses GP29, GP30, and GP31 and the last word of the flash user page with the appropriate configuration.
 - On UC3 D devices, program the last two words of the flash user page with the appropriate configuration.



- For more details, refer to the USB DFU bootloader guide.

4.1.1.7 Non Maskable Interrupt

The External Interrupt Controller (EIC) allows pins to be configured as external interrupts. Each external interrupt has its own interrupt request and can be individually masked. A Non-Maskable Interrupt (NMI) has the same properties as the other external interrupts, but is connected to the NMI request of the CPU, enabling it to interrupt any other interrupt mode.

On the UC3 B, the NMI is EXTINT[8].

On the UC3 D, the NMI is EXTINT[0].

This induces that on UC3 B GPIO alternate function A of PA05 is named EXTINT[0] and on UC3 D alternate function A of PA05 is EXTINT[8].

Table 4-5. EXTINT Number

Device	GPIO PA05	GPIO PA13
UC3 B	EXTINT[0]	NMI - EXTINT[8]
UC3 D	EXTINT[8]	NMI - EXTINT[0]

Conditions for a successful migration: Use the software framework EIC driver to handle the EIC controller.

4.1.1.8 PWM

UC3 B and UC3 D have a different PWM controller:

Table 4-6. PWM Controller Differences

Device	PWM Counter	PWM Mode
UC3 B / PWM Controller	20-bit counter per channel	Left aligned non-inverted
UC3 D / PWMA Controller	Common 12-bit time-base counter	Programmable Center or Left Aligned Programmable waveform polarity

Conditions for a successful migration:

- Use the software framework to handle the PWM controller.
- Do not use centered channels
- Do not use more than 12-bit of the counter
- Use the same counter configuration for all channels

4.1.1.9 ADC

UC3 B and UC3 D have a different ADC controller.

Figure 4-7. ADC Controller in UC3 B

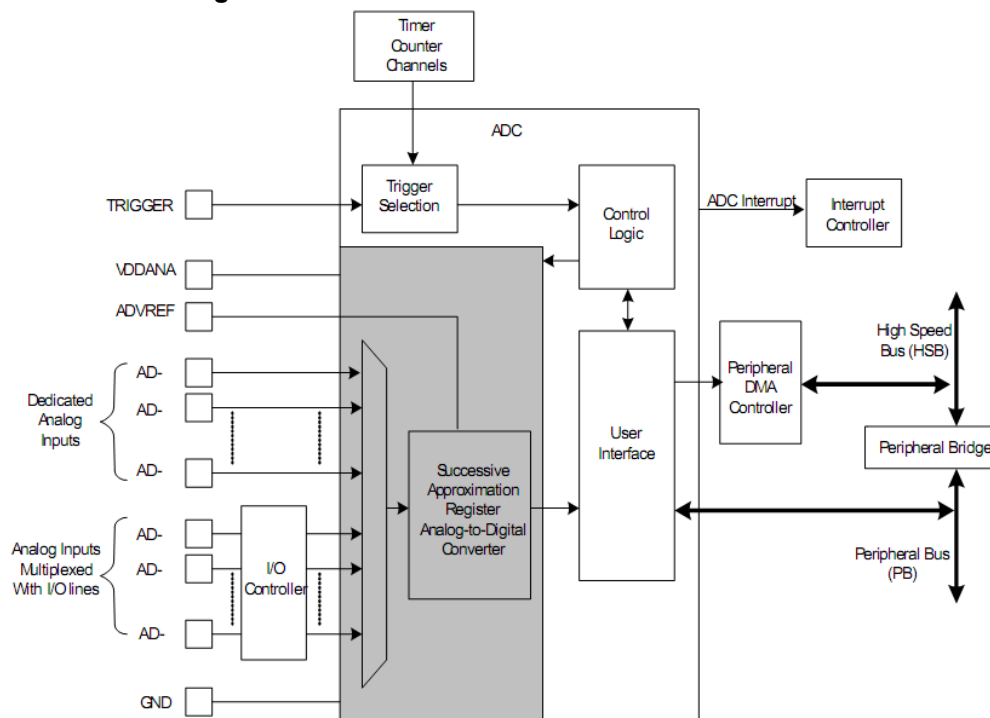


Figure 4-8. ADCIFD Controller in UC3 D

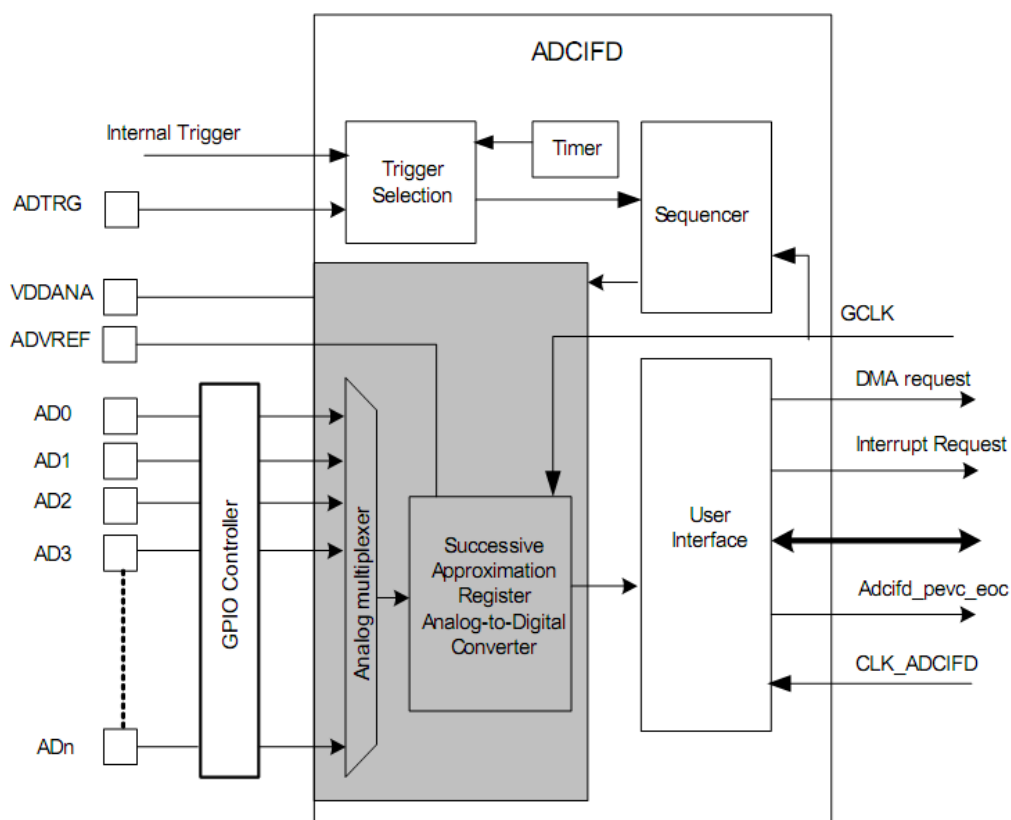


Table 4-9. ADC Controller Trigger Sources

Device	ADC Trigger Sources	ADCIFD Trigger Sources
UC3 B	External trigger pin Any of the timer counter outputs (TIOA)	-
UC3 D	-	Software Embedded 16-bit timer for periodic trigger Continuous trigger External trigger pin Timer counter channel 0 output (TIOA0)

Conditions for a successful migration: Use the software framework to handle the ADC controller.

4.1.1.10 Inter-IC Sound (I2S)

The UC3 B SSC (Synchronous Serial Controller) supports several communication modes, like I2S. The SSC consists of a receiver (RX), transmitter (TX) and a common clock divider. Both the SSC transmitter and receiver have 3 signals. The UC3 D has a dedicated I2S controller, named IISC, compliant with the I2S bus specification. The IISC has 5 signals, including the master clock generation.

Table 4-10. SSC versus IISC I/O Lines

QFP48	QFP64	SSC Controller (UC3 B)	IISC Controller (UC3 D)
-	55	TX_CLOCK (input/output)	ISCK (input/output)
-	38	RX_CLOCK (input/output)	
-	58	TX_FRAME_SYNC (input/output)	IWS (input/output)
-	54	RX_FRAME_SYNC (input/output)	
-	57	TX_DATA (output)	ISDO (output)
-	43	RX_DATA (input)	ISDI (input)
-	55	No equivalent function in the SSC	IMCK (input/output)

Note: some of the IISC functions are also available on other UC3 D pins. These functions are not present on these pins on UC3 B:

ISDO function is also available on UC3 D in QFP48 pin 41 and in QFP64 pin 53.
ISDI function is also available on UC3 D in QFP48 pin 42 and in QFP64 pin 56.
IWS function is also available on UC3 D in QFP48 pin 45 and in QFP61 pin 56.
IWS function is also available on UC3 D in QFP48 pin 46 and in QFP61 pin 62.

On the UC3 B, the I2S master clock is usually generated by a generic clock (GCLK). On the UC3 D, the IISC controller allows outputting a master clock thanks to the IMCK pin (output), but any generic clock (GCLK) can also be used.

Conditions for a successful migration:

- Do not use SSC receiver (RX) and transmitter (TX) simultaneously.
- Do not connect a clock on the SSC RX to synchronize the I2S TX flow.
- Use the software framework to handle the I2S transfer.
- Any of the generic clocks (GCLK) can be used for the I2S master clock.

4.2 Tools Considerations

Selecting the right part number in tools will affect:

- Device header files: the register address map will adjust to your part number.
- Linker file: the flash and RAM memory map
- Interrupt map, GPIO alternate feature map

4.2.1 IAR Embedded Workbench

In project properties:

- General options -> Target -> Device: Select the right UC3 D part number (uc{128,64,32}d{3,4}).
- Linker -> Config: if a specific linker file is specified (overriding default settings), make sure that the proper device one is selected.

4.2.2 AVR32 Studio

In project properties:

- C/C++ Build -> Settings -> MCU Settings -> Target MCU: select the right UC3 D part number (uc{128,64,32}d{3,4}).
- C/C++ Build -> Settings -> AVR32/GNU C Linker: if a specific linker file is specified, make sure that the proper device one is selected.

4.2.3 AVR Studio 5

In project properties:

- Device -> Change device -> Show devices: all parts -> Select the right UC3 D part number (ATUC{128,64,32}d{3,4}).
- Toolchain -> AVR32/GNU C Linker -> Miscellaneous: if a specific linker file is specified, make sure that the proper device one is selected.
- If some ASF modules are in the project, launch the ASF Wizard, remove existing modules and add the wanted available modules for the UC3 D.

4.2.4 Standalone Makefile / GNU Toolchain

Using the standalone makefile / config.mk: Open the associated config.mk and check the following parameter:

- PART = uc{128,64,32}d{3,4} adjust the correct part number
- FLASH = internal@0x80000000,xKb: adjust the correct flash size
- INC_PATH (include path), CSRCS (list of C files) and ASRCS (list of assembly files) variables should be adjusted to match the part driver. Refer to the section “Using the Atmel Software framework” for more details on which files to include.
- LINKER_SCRIPT: adjust the correct linker script path if needed.



4.3 Using the AVR Software Framework (ASF)

The Atmel AVR software framework (ASF) provides a simple abstraction software layers for the migration.

4.3.1 ASF Migration

The /avr32/drivers directory contains the low level devices driver files. Include the correct drivers for the selected peripherals.

Table 4-11. ASF Driver Migration

Module	UC3 B Series	UC3 D Series
ADC	drivers/adc/adc.c,h	drivers /adcifd/adcifc.c,h
Flash	drivers/flashc/flashc.c,h	drivers /flashcdw/flascdw.c,h
PWM	drivers/pwm/pwm.c,h	drivers /pwma/pwma.c,h
Power Manager	drivers/pm/pm.c,h drivers /pm/power_clocks_lib.c,h	drivers/pm/pm_uc3d.c,h drivers/pm/power_clocks_lib.c,h drivers/scif/scif_uc3d.c,h
Real Time Clock	drivers/rtc/rtc.c,h	drivers/ast/ast.c,h
SSC	drivers/ssc/ssc.c,h	drivers/iisc/iisc.c,h
TWI	drivers/twi/twi.c	drivers/twim/twim.c drivers/twis/twis.c
USB	drivers/usbb/_asf_v1/usb_drv.c,h services/usb/_asf_v1/*	drivers /usbc/usbc.c,h services/usbc/*

Note: A software clock services is provided in /common/services/basic/clock/. This module provides the same API for both UC3 B and UC3 D series and can replace the Power Manager driver..

4.3.1.1 GPIO Map (name, alternate feature)

Some GPIO definition name might be changed between UC3 B and UC3 D (eg AVR32_USART1_RXD_x_x_PIN). A specific migration_uc3b_to_uc3d_io.h is provided to ease the migration.

4.3.1.2 Interrupt (name)

Some interrupt definition group name might be changed between UC3 B and UC3 D (eg. AVR32_USART1_RXD_x_x_PIN).

A specific migration_uc3b_to_uc3d_interrupt.h is provided to ease the migration.

Conditions for a successful migration:

- To migrate from UC3 B to UC3 D series using the AVR software framework, replace the wanted set of files and modify the project to match the new API.



Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parking 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
16F, Shin Osaki Kangyo Bldg.
1-6-4 Osaki Shinagawa-ku
Tokyo 104-0032
JAPAN
Tel: (+81) 3-6417-0300
Fax: (+81) 3-6417-0370

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