

Introduction

The ATmega328P Automotive devices you have received conform functionally to the current device data sheet (ww1.microchip.com/downloads/en/DeviceDoc/Atmel-7810-Automotive-Microcontrollers-ATmega328P_Datasheet.pdf), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega328P Automotive devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X Erratum is applicable.
- * This silicon revision was never released to production.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A-C	Rev. D
Device		*	-

2. Silicon Errata Issues

2.1 None

There are no known errata for this silicon.

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (ww1.microchip.com/downloads/en/DeviceDoc/Atmel-7810-Automotive-Microcontrollers-ATmega328P_Datasheet.pdf).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 System Clock and Clock Options

3.1.1 Low-Power Crystal Oscillator

A clarification has been made to *Table 8-4 Start-Up Times for the Low-Power Crystal Oscillator Clock Selection*, where 14 CK in the column *Additional Delay from Reset* ($V_{CC} = 5.0V$) has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-4. Start-Up Times for the Low-Power Crystal Oscillator Clock Selection

Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset ($V_{CC} = 5.0V$)	CKSEL0	SUT[1:0]
Ceramic resonator, fast rising power	258 CK	19 CK + 4 ms ⁽¹⁾	0	00
Ceramic resonator, slowly rising power	258 CK	19 CK + 65 ms ⁽¹⁾	0	01
Ceramic resonator, BOD enabled	1K CK	19 CK ⁽²⁾	0	10
Ceramic resonator, fast rising power	1K CK	19 CK + 4 ms ⁽²⁾	0	11
Ceramic resonator, slowly rising power	1K CK	19 CK + 65 ms ⁽²⁾	1	00
Crystal Oscillator, BOD enabled	16K CK	19 CK	1	01
Crystal Oscillator, fast rising power	16K CK	19 CK + 4 ms	1	10
Crystal Oscillator, slowly rising power	16K CK	19 CK + 65 ms	1	11

Notes:

1. These options should only be used when not operating close to the maximum device frequency and only if frequency stability at start-up is unimportant for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum device frequency and if frequency stability at start-up is unimportant for the application.

3.1.2 Full Swing Crystal Oscillator

A clarification has been made to *Table 8-6 Start-Up Times for the Full Swing Crystal Oscillator Clock Selection*, where 14 CK in the column *Additional Delay from Reset* ($V_{CC} = 5.0V$) has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-6. Start-Up Times for the Full Swing Crystal Oscillator Clock Selection

Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset ($V_{CC} = 5.0V$)	CKSEL0	SUT[1:0]
Ceramic resonator, fast rising power	258 CK	19 CK + 4.1 ms ⁽¹⁾	0	00
Ceramic resonator, slowly rising power	258 CK	19 CK + 65 ms ⁽¹⁾	0	01
Ceramic resonator, BOD enabled	1K CK	19 CK ⁽²⁾	0	10
Ceramic resonator, fast rising power	1K CK	19 CK + 4.1 ms ⁽²⁾	0	11
Ceramic resonator, slowly rising power	1K CK	19 CK + 65 ms ⁽²⁾	1	00
Crystal Oscillator, BOD enabled	16K CK	19 CK	1	01

.....continued

Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset ($V_{CC} = 5.0V$)	CKSEL0	SUT[1:0]
Crystal Oscillator, fast rising power	16K CK	19 CK + 4.1 ms	1	10
Crystal Oscillator, slowly rising power	16K CK	19 CK + 65 ms	1	11

Notes:

1. These options should only be used when not operating close to the maximum device frequency and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device and if frequency stability at start-up is unimportant for the application.

3.1.3 Low-Frequency Crystal Oscillator

A clarification has been made to *Table 8-8 Start-Up Times for the Low-Frequency Crystal Oscillator Clock Selection - SUT Fuses*, where 14 CK in the column *Additional Delay from Reset ($V_{CC} = 5.0V$)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-8. Start-Up Times for the Low-Frequency Crystal Oscillator Clock Selection - SUT Fuses

SUT[1:0]	Additional Delay from Reset ($V_{CC} = 5.0V$)	Recommended Usage
00	19 CK	Fast rising power or BOD enabled
01	19 CK + 4.1 ms	Slowly rising power
10	19 CK + 65 ms	Stable frequency at start-up
11	Reserved	

3.1.4 Calibrated Internal RC Oscillator

A clarification has been made to *Table 8-11 Start-Up Times for the Calibrated Internal RC Oscillator Clock Selection - SUT*, where 14 CK in the column *Additional Delay from Reset ($V_{CC} = 5.0V$)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-11. Start-Up Times for the Calibrated Internal RC Oscillator Clock Selection - SUT

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset ($V_{CC} = 5.0V$)	SUT[1:0]
BOD enabled	6 CK	19 CK ⁽¹⁾	00
Fast rising power	6 CK	19 CK + 4 ms	01
Slow rising power	6 CK	19 CK + 65 ms ⁽²⁾	10
Reserved			11

Notes:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.
2. The device is shipped with this option selected.

3.1.5 128 kHz Internal Oscillator

A clarification has been made to *Table 8-13 Start-Up Times for the 128 kHz Internal Oscillator*, where 14 CK in the column *Additional Delay from Reset* ($V_{CC} = 5.0V$) has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-13. Start-Up Times for the 128 kHz Internal Oscillator

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset	SUT[1:0]
BOD enabled	6CK	19 CK ⁽¹⁾	00
Fast rising power	6CK	19 CK + 4 ms	01
Slowly rising power	6CK	19 CK + 65 ms	10
Reserved			11

Note:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.

3.1.6 External Clock

A clarification has been made to *Table 8-15 Start-Up Times for the External Clock Selection*, where 14 CK in the column *Additional Delay from Reset* ($V_{CC} = 5.0V$) has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 8-15. Start-Up Times for the External Clock Selection

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset ($V_{CC} = 5.0V$)	SUT[1:0]
BOD enabled	6 CK	19 CK ⁽¹⁾	00
Fast rising power	6 CK	19 CK + 4.1 ms	01
Slow rising power	6 CK	19 CK + 65 ms ⁽²⁾	10
Reserved			11

Notes:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.
2. The device is shipped with this option selected.

3.2 Power Management and Sleep Modes

3.2.1 Sleep Modes

A clarification for the selection of the appropriate sleep modes and their wake-up sources has been made.

Figure “Clock Distribution” presents the different clock systems in the ATmega328P Automotive and their distribution. The figure helps select an appropriate sleep mode. The table below shows the various sleep modes and their wake-up sources BOD disable ability.

Table 9-1. Active Clock Domains and Wake-up Sources in the Different Sleep Modes

Sleep Mode	Active Clock Domains					Oscillators		Wake-Up Sources							Software BOD Disable
	clkCPU	clkFLASH	clkIO	clkADC	clkASY	Main Clock Source Enabled	Timer Oscillator Enabled	INT and PCINT	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other I/O	
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X ⁽²⁾	X	X	X ⁽²⁾	X	X	X		
Power-Down								X	X				X		X
Power-Save					X		X ⁽²⁾	X	X	X			X		X
Standby ⁽¹⁾						X		X	X				X		X
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X	X	X			X		X

Notes:

1. Only recommended with an external crystal or resonator selected as the clock source.
2. If Timer/Counter2 is running in Asynchronous mode.

Write the SE bit in the Sleep Mode Control (SMCR) register to logic one, and execute a SLEEP instruction to enter any six sleep modes. The SM2, SM1, and SM0 bits in the SMCR register select which sleep mode (Idle, ADC Noise Reduction, Power-Down, Power-Save, Standby, or Extended Standby) to be activated by the SLEEP instruction. See *Table “Sleep Mode Select”* for a summary.

If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up. The MCU is then halted for four cycles in addition to the start-up time, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The register file and SRAM contents are unaltered when the device wakes up from a sleep mode. If a reset occurs during a sleep mode, the MCU wakes up and executes from the Reset Vector.

3.3 Interrupts

3.3.1 Interrupt Vectors in ATmega328P Automotive

A clarification for the source names of the Interrupt vectors has been made to comply with the header file naming convention.

Table 11-1. Reset and Interrupt Vectors in ATmega328P Automotive

Vector No	Program Address(2)	Source	Interrupts definition
1	0x0000 ⁽¹⁾	RESET	External pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2_COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2_COMPB	Timer/Counter2 Compare Match B
10	0x0012	TIMER2_OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1_CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1_COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1_COMPB	Timer/Counter1 Compare Match B
14	0x001A	TIMER1_OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0_COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0_COMPB	Timer/Counter0 Compare Match B
17	0x0020	TIMER0_OVF	Timer/Counter0 Overflow
18	0x0022	SPI_STC	SPI Serial Transfer Complete
19	0x0024	USART_RX	USART Rx complete
20	0x0026	USART_UDRE	USART Data Register Empty
21	0x0028	USART_TX	USART Tx complete
22	0x002A	ADC	ADC Conversion complete
23	0x002C	EE_READY	EEPROM Ready
24	0x002E	ANALOG_COMP	Analog Comparator
25	0x0030	TWI	Two-wire Serial Interface (I ² C)
26	0x0032	SPM_READY	Store Program Memory Ready

Notes:

1. When the BOOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See *"Boot Loader Support – Read-While-Write Self- Programming"*.
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

The most typical and general program setup for the Reset and Interrupt Vector Addresses for ATmega328P Automotive is:

Address	Labels	Code		Comments
0x0000		jmp	RESET	; Reset
0x0001		jmp	INT0	; IRQ0


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0x0002      jmp      INT1          ; IRQ1
0x0003      jmp      PCINT0        ; PCINT0
0x0004      jmp      PCINT1        ; PCINT1
0x0005      jmp      PCINT2        ; PCINT2
0x0006      jmp      WDT           ; Watchdog Timeout
0x0007      jmp      TIMER2_COMP_A ; Timer2 CompareA
0x0008      jmp      TIMER2_COMP_B ; Timer2 CompareB
0x0009      jmp      TIMER2_OVF     ; Timer2 Overflow
0x000A      jmp      TIMER1_CAPT    ; Timer1 Capture
0x000B      jmp      TIMER1_COMP_A ; Timer1 CompareA
0x000C      jmp      TIMER1_COMP_B ; Timer1 CompareB
0x000D      jmp      TIMER1_OVF     ; Timer1 Overflow
0x000E      jmp      TIMER0_COMP_A ; Timer0 CompareA
0x000F      jmp      TIMER0_COMP_B ; Timer0 CompareB
0x0010      jmp      TIMER0_OVF     ; Timer0 Overflow
0x0011      jmp      SPI_STC        ; SPI Transfer Complete
0x0012      jmp      USART_RXC      ; USART RX Complete
0x0013      jmp      USART_UDRE     ; USART UDR Empty
0x0014      jmp      USART_TXC      ; USART TX Complete
0x0015      jmp      ADC            ; ADC Conversion Complete
0x0016      jmp      EE_READY       ; EEPROM Ready
0x0017      jmp      ANA_COMP       ; Analog Comparator
0x0018      jmp      TWI            ; 2-wire Serial
0x0019      jmp      SPM_READY      ; SPM Ready
;
0x001A      RESET:  ldi      r16,high(RAMEND) ; Main program start
0x001B      out      SPH,r16              ; Set Stack Pointer to top of RAM
0x001C      ldi      r16,low(RAMEND)
0x001D      out      SPL,r16
0x001E      sei                          ; Enable interrupts
0x001F      <instr> xxx
...          ...          ...          ...

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3.4 16-bit Timer/Counter1 with PWM

3.4.1 Fast PWM Mode in ATmega328P Automotive

A clarification for the description of the COM_nx1:0 in the Timer/Counter1 PWM Mode has been made.

The procedure for updating ICR1 differs from updating OCR1A when used for defining the TOP value. The ICR1 register is not double-buffered, meaning that if ICR1 is changed to a low value when the counter is running with none or a low prescaler value, there is a risk that the new ICR1 value written is lower than the current value of TCNT1. Then the result will be that the counter will miss the compare match at the TOP value. The counter will then have to count to the MAX value (0xFFFF) and wrap around starting at 0x0000 before the compare match can occur. The OCR1A register, however, is double-buffered. This feature allows the OCR1A I/O location to be written anytime. When the OCR1A I/O location is written, the written value adds to the OCR1A buffer register. The OCR1A compare register will then be updated with the value in the buffer register at the next timer clock cycle TCNT1 matches TOP. The update is done at the same timer clock cycle as the TCNT1 is cleared, and the TOV1 flag is set.

Defining TOP using the ICR1 register works well when using fixed TOP values. By using ICR1, the OCR1A register is free to be used to generate a PWM output on OC1A. However, if the base PWM frequency is changed actively (by changing the TOP value), using the OCR1A as TOP is a better choice due to its double buffer feature.

In fast PWM mode, the compare units allow the generation of PWM waveforms on the OC1x pins. Setting the COM1x1:0 bits to two will produce a non-inverted PWM. If setting the COM1x1:0 to three (see Table “Compare Output Mode, Fast PWM”), an inverted PWM output is generated. The actual OC1x value will only be visible on the port pin if the data direction for the port pin is set as output (DDR_OC1x). The PWM waveform is generated by setting (or clearing) the OC1x register at the compare match between OCR1x and TCNT1. Clearing (or setting) the OC1x register at the timer clock cycle, the counter is cleared (changes from TOP to BOTTOM).

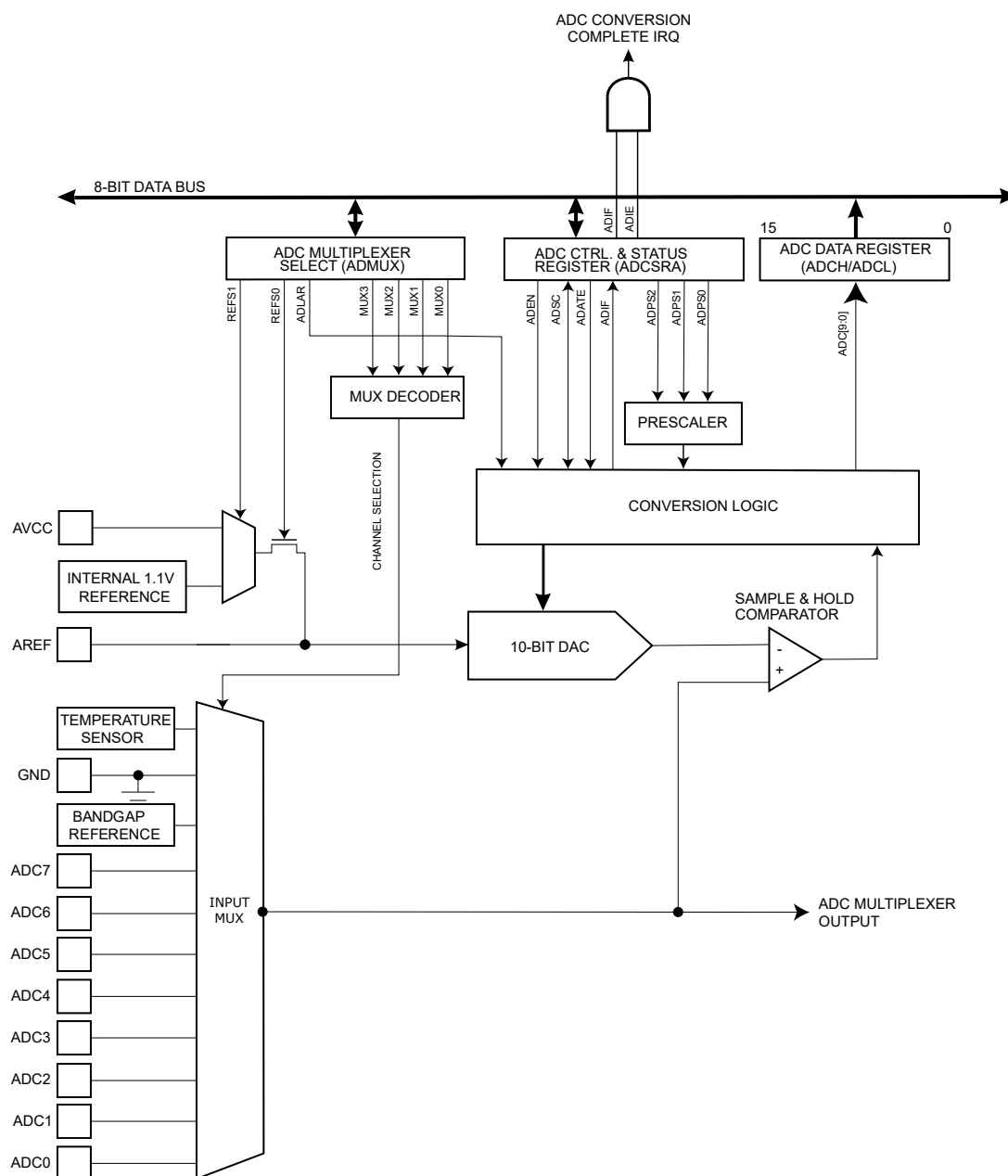
3.5 ADC - Block Diagram

3.5.1 ADC - Analog-to-Digital Converter Block Diagram

A clarification for the Analog-to-Digital Converter (ADC) block diagram has been made.

In the ADC block diagram ADFR is changed to **ADATE**, and **ADSC** is now **bidirectional**.

Figure 23-1. Analog-to-Digital Converter Block Schematic Operation



3.6 Electrical Characteristics

3.6.1 Electrical Characteristics

All DC/AC characteristics in this data sheet are based on characterization of Microchip ATmega328P Automotive AVR® microcontroller manufactured in an automotive process technology.

3.6.1.1 Absolute Maximum Ratings

Stresses beyond those listed under “*Absolute Maximum Ratings*” may cause permanent damage to the device, as this is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Min.	Typ.	Max.	Unit
Operating temperature	–55		+125	°C
Storage temperature	–65		+150	°C
Voltage on any pin except RESET with respect to ground	–0.5		$V_{CC} + 0.5$	V
Voltage on RESET with respect to ground	–0.5		+13.0	V
Maximum Operating Voltage		6.0		V
DC current per I/O pin		40.0		mA
DC current V_{CC} and GND pins		200.0		mA
Injection current at $V_{CC} = 0V$		$\pm 5.0^{(1)}$		mA
Injection current at $V_{CC} = 5V$		± 1.0		mA

Note:

1. Maximum current per port = ± 30 mA

3.6.1.2 DC Characteristics

A clarification for Analog Comparator Input Offset Voltage has been made. Two more characteristics in **bold** have been added.

$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 2.7V$ to $5.5V$ (unless otherwise noted)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input low-voltage, except XTAL1 and RESET pin	$V_{CC} = 2.7\text{--}5.5V$	V_{IL}	–0.5		$0.3V_{CC}^{(1)}$	V
Input high-voltage, except XTAL1 and RESET pins	$V_{CC} = 2.7\text{--}5.5V$	V_{IH}	$0.6V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Input low-voltage, XTAL1 pin	$V_{CC} = 2.7\text{--}5.5V$	V_{IL1}	–0.5		$0.1V_{CC}^{(1)}$	V
Input high-voltage, XTAL1 pin	$V_{CC} = 2.7\text{--}5.5V$	V_{IH1}	$0.7V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Input low-voltage, RESET pin	$V_{CC} = 2.7\text{--}5.5V$	V_{IL2}	–0.5		$0.1V_{CC}^{(1)}$	V
Input high-voltage, RESET pin	$V_{CC} = 2.7\text{--}5.5V$	V_{IH2}	$0.9V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Output low-voltage ⁽³⁾	$I_{OL} = 20\text{ mA}$, $V_{CC} = 5V$ $I_{OL} = 5\text{ mA}$, $V_{CC} = 3V$	V_{OL}			0.8 0.5	V
Output high- voltage ⁽⁴⁾	$I_{OH} = -20\text{ mA}$, $V_{CC} = 5V$ $I_{OH} = -10\text{ mA}$, $V_{CC} = 3V$	V_{OH}	4.1 2.3			V

.....continued

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input leakage current I/O pin	$V_{CC} = 5.5V$, pin low (absolute value)	I_{IL}			1	μA
Input leakage current I/O pin	$V_{CC} = 5.5V$, pin high (absolute value)	I_{IH}			1	μA
Reset pull-up resistor		R_{RST}	30		60	$k\Omega$
I/O pin pull-up resistor		R_{PU}	20		50	$k\Omega$
Analog Comparator Input Offset Voltage	$V_{CC} = 5V$ $V_{in} = V_{CC}/2$	V_{ACIO}		<10	40	mV
Analog Comparator Input Offset Voltage	$V_{CC} < 3.6V$ $V_{in} < 0.5V$	V_{ACIO}		<15	60⁽⁵⁾	mV
Analog Comparator Input Offset Voltage	$V_{CC} > 3.6V$ $V_{in} < 0.5V$	V_{ACIO}		<15	500⁽⁵⁾	mV
Analog Comparator Input Leakage current	$V_{CC} = 5V$ $V_{in} = V_{CC}/2$	I_{ACLK}	-50		+50	nA
Analog Comparator Propagation Delay	$V_{CC} = 2.7V$ $V_{CC} = 4.0V$	t_{ACID}		750 500		ns

Notes:

1. "Max." means the highest value where the pin is ensured to be read as low.
2. "Min." means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at $V_{CC} = 5V$, 10 mA at $V_{CC} = 3V$) under steady-state conditions (non-transient), observe the following:
 - a. For ports C0 - C5, the sum of all I_{OL} may not exceed 100 mA.
 - b. For ports B0 - B5, D5 - D7, XTAL1 and XTAL2, the sum of all I_{OL} may not exceed 100 mA.
 - c. For ports D0 - D4, the sum of all I_{OL} may not exceed 100 mA.

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not ensured to sink a current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at $V_{CC} = 5V$, 10 mA at $V_{CC} = 3V$) under steady-state conditions (non-transient), observe the following:
 - a. For ports C0 - C5 and D0 - D4, the sum of all I_{OH} may not exceed 150 mA.
 - b. For ports B0 - B5, D5 - D7, XTAL1 and XTAL2, the sum of all I_{OH} may not exceed 150 mA.

If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not ensured to source a current higher than the listed test condition.
5. These values are based on characterization. The maximum limit is not tested in production and, therefore, cannot be ensured.

 $T_A = -40^\circ C$ to $+125^\circ C$, $V_{CC} = 2.7V$ to $5.5V$ (unless otherwise noted)

Parameter	Condition	Symbol	Min.	Typ. ⁽²⁾	Max.	Units
Power supply current ⁽¹⁾	Active 4 MHz, V _{CC} = 3V	I _{CC}		1.5	2.4	mA
	Active 8 MHz, V _{CC} = 5V			5.2	10	mA
	Active 16 MHz, V _{CC} = 5V			9.2	14	mA
	Idle 4 MHz, V _{CC} = 3V			0.25	0.6	mA
	Idle 8 MHz, V _{CC} = 5V			1.0	1.6	mA
	Idle 16 MHz, V _{CC} = 5V			1.9	2.8	mA
Power-down mode ⁽³⁾	WDT enabled, V _{CC} = 3V	I _{CC}			44	μA
	WDT enabled, V _{CC} = 5V				66	μA
	WDT disabled, V _{CC} = 3V				40	μA
	WDT disabled, V _{CC} = 5V				60	μA

Notes:

1. Values with Section “Minimizing Power Consumption” enabled (0xFF).
2. Typical values at 25°C. Maximum values are test limits in production.
3. The current consumption values include input leakage current.

3.7 Ordering Information

3.7.1 Ordering Information

A clarification has been made to tables titled ‘Package Type’ for all devices documented in the data sheet:

- A note to the PN row was added informing that the package type can be delivered in two different styles

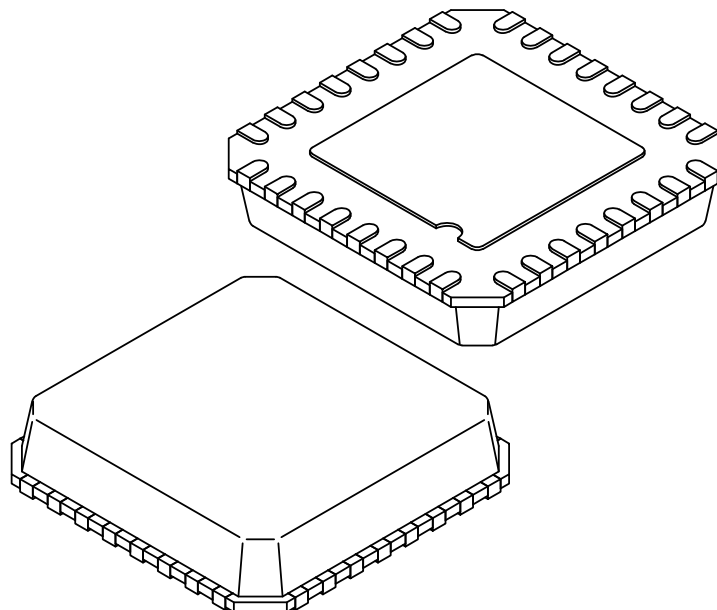
Package Type	
MA	32-lead, (7x7x1.0 mm) Plastic Thin Quad Flat Package (TQFP)
PN ⁽¹⁾	32-pad, (5x5x0.9 mm) body, Lead Pitch 0.50 mm Thin Plastic Quad Flat No-Lead (VQFN)

Note:

1. This package type can be delivered with two different styles in reference numbers ‘C04-21400’ (punched) and ‘C04-21395’ (sawn), as shown in section 3.8.1. PN. For PCB layouts, it is recommended to consider both *recommended land patterns*.

32-Lead Thin Plastic Quad Flat, No Lead Package (S4B) - 5x5 mm Body [VQFN] Punch Singulated; 3.10x3.10 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	32		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Mold Cap Thickness	A2	-	0.65	0.70
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Mold Cap Length	D1	4.75 BSC		
Exposed Pad Length	D2	2.95	3.10	3.25
Overall Width	E	5.00 BSC		
Mold Cap Width	E1	4.75 BSC		
Exposed Pad Width	E2	2.95	3.10	3.25
Terminal Width	b	0.18	0.23	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

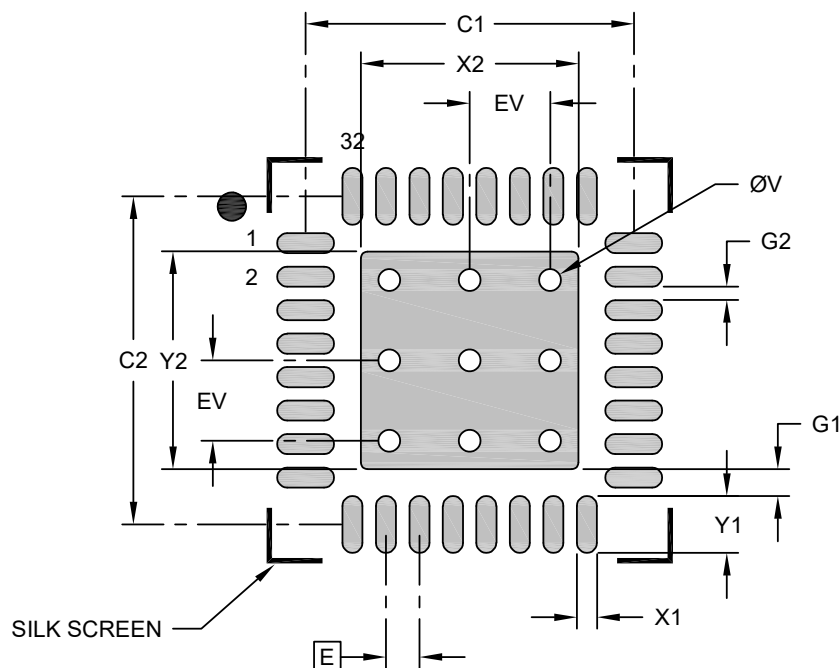
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is punch singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21400 Rev B Sheet 2 of 2

32-Lead Thin Plastic Quad Flat, No Lead Package (S4B) - 5x5 mm Body [VQFN] Punch Singulated; 3.10x3.10 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.25
Optional Center Pad Length	Y2			3.25
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.40		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

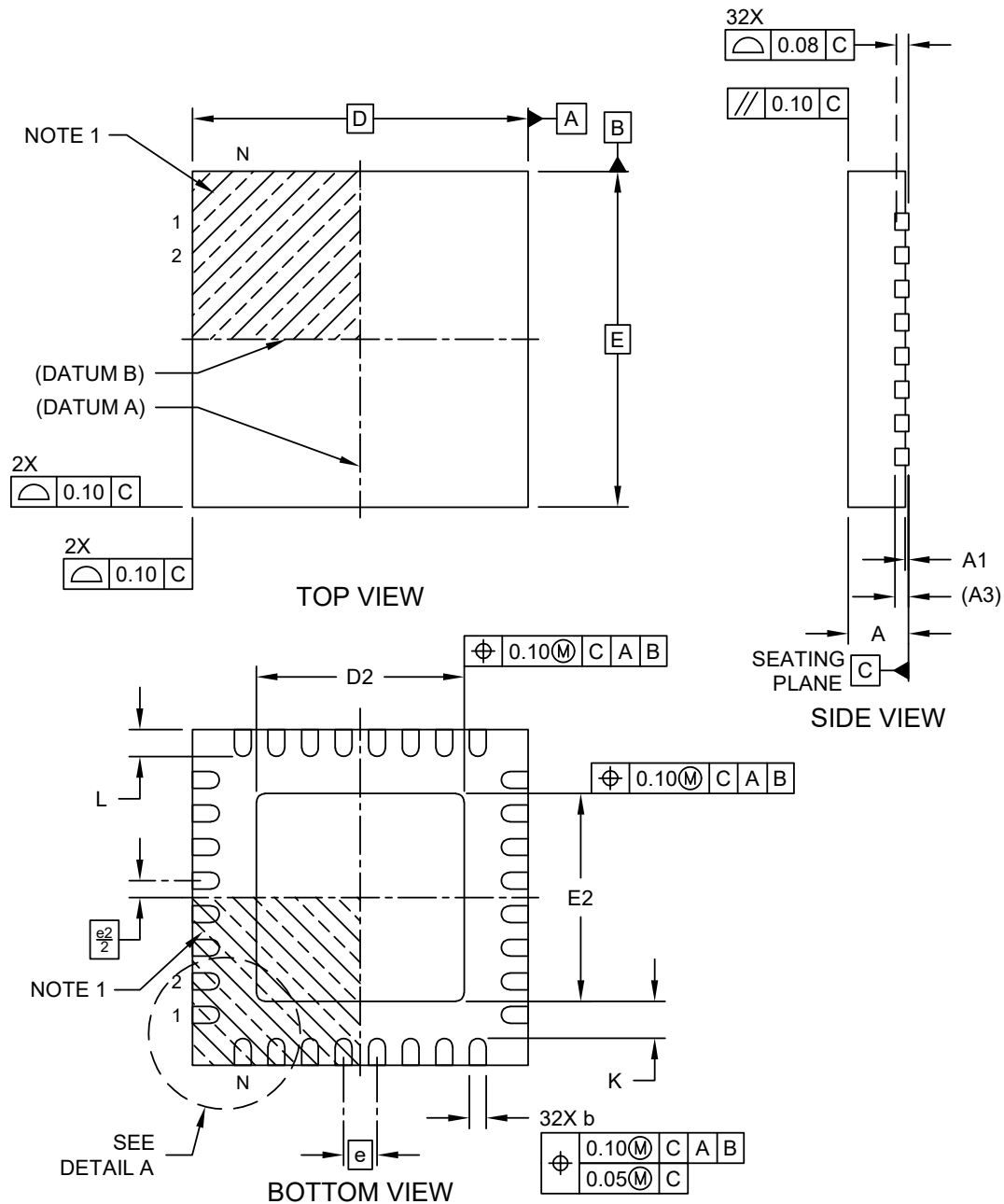
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23400 Rev B

**32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN]
With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF**

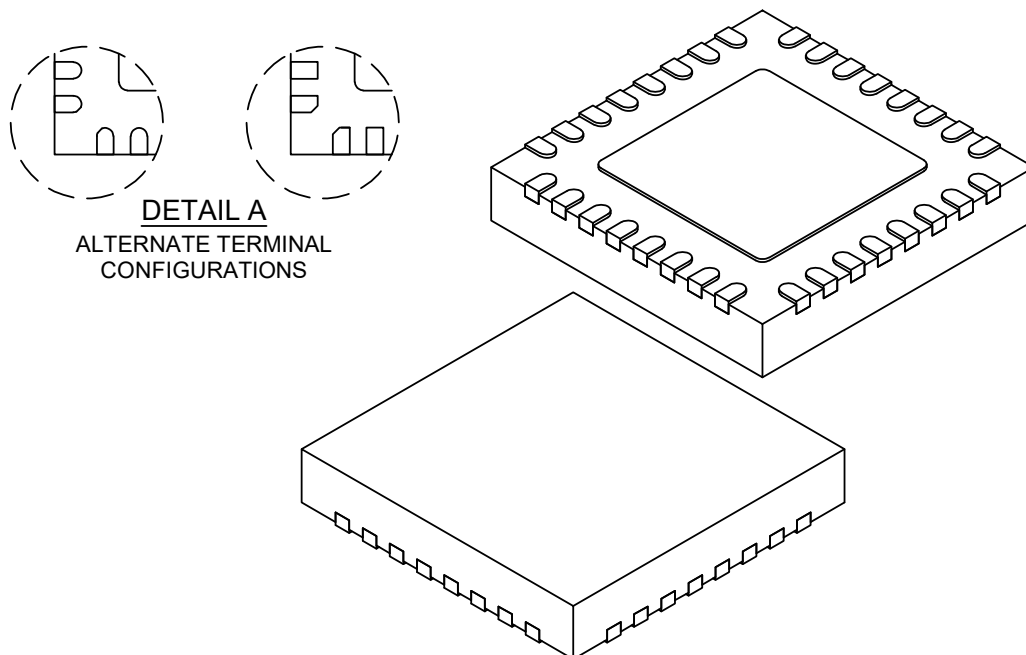
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21395-UBB Rev C Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN] With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	32		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.00	3.10	3.20
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.00	3.10	3.20
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

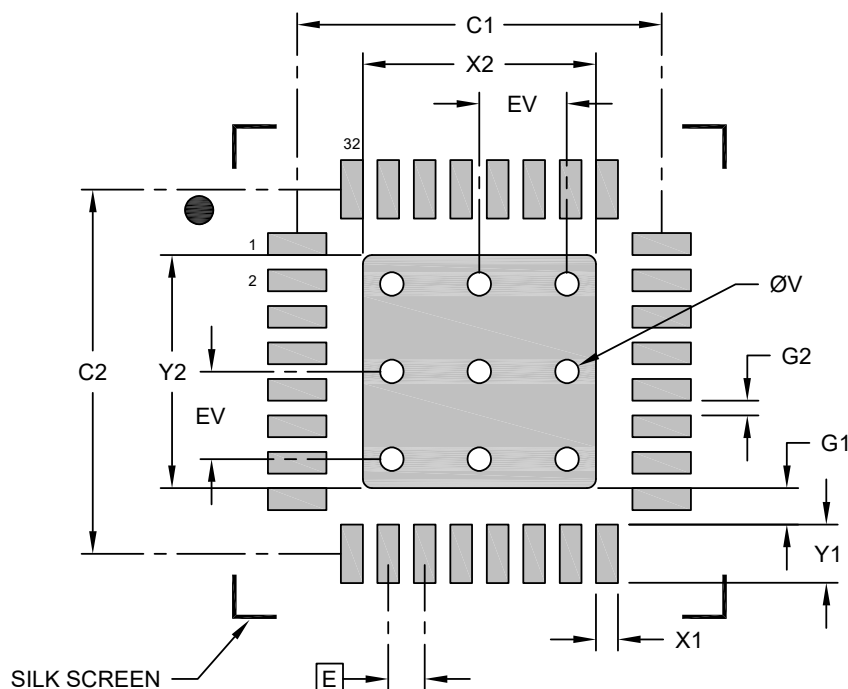
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21395-UBB Rev C Sheet 2 of 2

**32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN]
With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			3.20
Center Pad Length	Y2			3.20
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.20		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

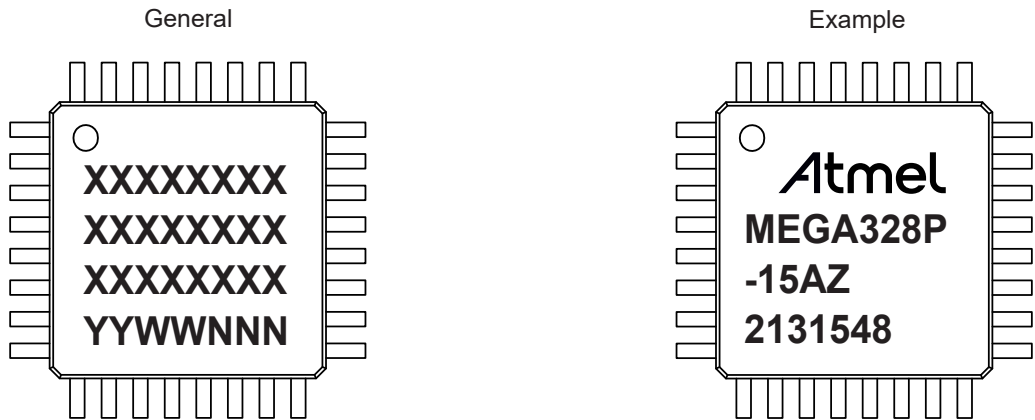
Microchip Technology Drawing C04-23395-UBB Rev C

3.9 Package Marking Information

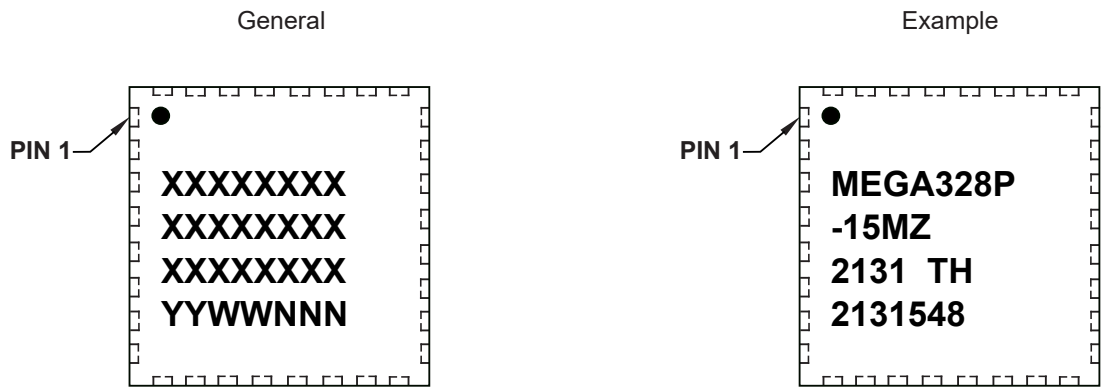
Legend:	XX...X	Customer-specific information or Microchip part number
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3.9.1 32-Pin TQFP



3.9.2 32-Pin VQFN



4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
B	04/2024	- Document: - Editorial updates - Added new data sheet clarifications: - System Clock and Clock Options: 3.1.1. Low-Power Crystal Oscillator 3.1.2. Full Swing Crystal Oscillator 3.1.3. Low-Frequency Crystal Oscillator 3.1.4. Calibrated Internal RC Oscillator 3.1.5. 128 kHz Internal Oscillator 3.1.6. External Clock
A	11/2022	Initial release of this document - Errata content moved from the data sheet and restructured to the new document template - Data sheet clarifications added: - Power Management and Sleep Modes: 3.2.1. Sleep Modes - Interrupts: 3.3.1. Interrupt Vectors in ATmega328P Automotive 16-bit Timer/Counter1 with PWM: 3.4.1. Fast PWM Mode in ATmega328P Automotive - ADC - Block Diagram: 3.5.1. ADC - Analog-to-Digital Converter Block Diagram - Electrical Characteristics: 3.6.1.2. DC Characteristics - Ordering Information: 3.7.1. Ordering Information - Packaging Information: 3.8.1. PN - Package Marking: 3.9. Package Marking Information

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