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Component Placement Checklist for the LAN9420I, 128-pin VTQFP Package

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Component Placement Checklist for LAN9420I

Information Particular for the 128-pin VTQFP Package

LAN9420I VTQFP Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TPO+, pin 101) as close to the LAN9420I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TPO-, pin 100) as close to the LAN9420I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (TPI+, pin 106) as close to the LAN9420I as possible.

4. Place the 49.9 Ω RX termination pull-up (TPI-, pin 104) as close to the LAN9420I as possible.

LAN9420I VTQFP Magnetics:

1. Place the 10.0 Ω TX/RX Channel Center Tap feed resistor as close to the magnetics as possible.

2. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

3. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN9420I VTQFP as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9420I VTQFP.

3. Select and place the magnetics as to set up the best routing scheme from the LAN9420I VTQFP to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

4. Place the Unused Wire Pair termination resistors and the 1000 ρF, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.

5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

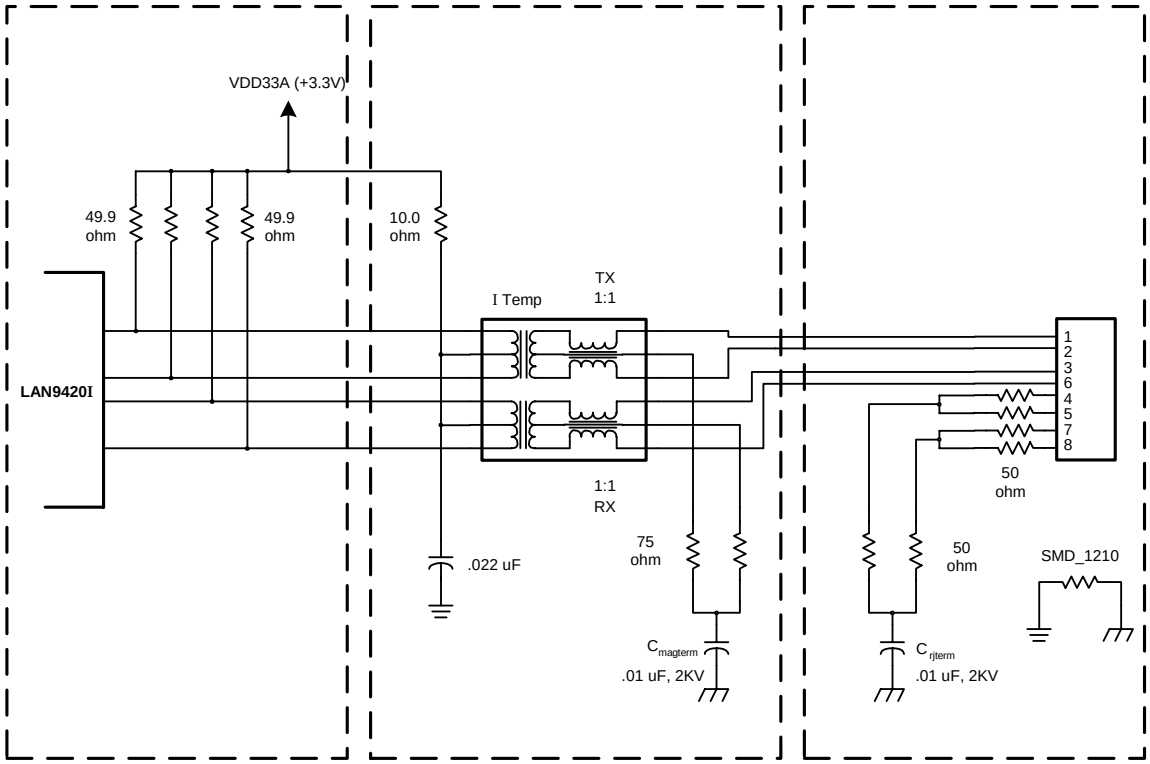

Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TX+ & TX- signals placed close to the LAN9420I for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

+3.3V Power Supply Connections:

1. Place the (15) VDD33IO decoupling capacitors for the LAN9420I VTQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the (2) VDD33A decoupling capacitors for the LAN9420I VTQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the (1) VDD33BIAS decoupling capacitor for the LAN9420I VTQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

VDD18CORE:

1. VDD18CORE (pin 8) requires a 0.01 μF bypass capacitor and a low ESR 4.7 μF bulk capacitor placed as close as possible to pin 8.

2. The other VDD18CORE pins (pins 9 & 82) only require a 0.01 μF bypass capacitor placed as close as possible to pin 9 & 82.

3. Place the (1) VDD18PLL decoupling capacitor for the LAN9420I VTQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

4. Place the (1) VDD18TX decoupling capacitor for the LAN9420I VTQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

Ground Connections:

1. There are no component placement issues associated with the LAN9420I VTQFP ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25 MHz crystal, the 1.0 M Ω parallel resistor and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN9420I VTQFP (XI, pin 120 & XO, pin 119) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all crystal components are referenced to the same reference plane.

EEPROM Interface:

1. There are no component placement issues associated with the EEPROM Interface.

EXRES Resistor:

1. Place the EXRES resistor as close to pin 109 of the LAN9420I VTQFP as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN9420I VTQFP.

PCI Bus Required External Pull-ups:

1. There are no component placement issues associated with the PCI Bus Required External Pull-ups. The only stipulation is that these pull-ups should be located on the baseboard of the design. They should *not* be located on the add-in card (if applicable).

PCI Device Interface:

1. The design engineer must review placement issues associated with the PCI Interface. Specific processor design guidelines should be reviewed in determining the placement of the LAN9420I device with respect to the processor. Address, data and control signal trace lengths must be considered when placing these two devices. Critical timing issues may arise if recommended trace lengths are exceeded. Both the PCI specification and the LAN9420I Routing Guideline document must be reviewed in order to determine the optimum placement.

Miscellaneous:

1. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.

2. Bulk capacitors for each power plane can reside anywhere on the plane they serve.