TB3268

Using the CRC-on-Boot

Introduction

Cyclic Redundancy Checks (CRCs) are a common means of performing error checking on areas of Non-Volatile Memory (NVM) and ensuring data integrity of this memory. In many safety-critical applications, it can be useful or necessary to perform this kind of check, independent of the program memory of the device. It may also be a useful check to perform before any of this program memory is executed to prevent any erroneous code from executing and causing potential issues in the system.

The CRC-on-Boot feature was designed with these applications in mind. It can perform a CRC on several areas of NVM on its device without relying on the program memory. It can also hold the device in Reset prior to code execution if errors are found. This technical brief provides information about the CRC-on-Boot feature of the 32-bit CRC module on a range of PIC® microcontrollers. This feature builds on and utilizes hardware based on the previously existing 16-bit CRC module. Therefore, it is recommended that those unfamiliar with the PIC16F/PIC18F CRC module to read **TB3128: "CRC and Memory Scan on 8-Bit Microcontrollers"** to gain a familiarity with how the CRC module functions, as well as CRC calculations in general.

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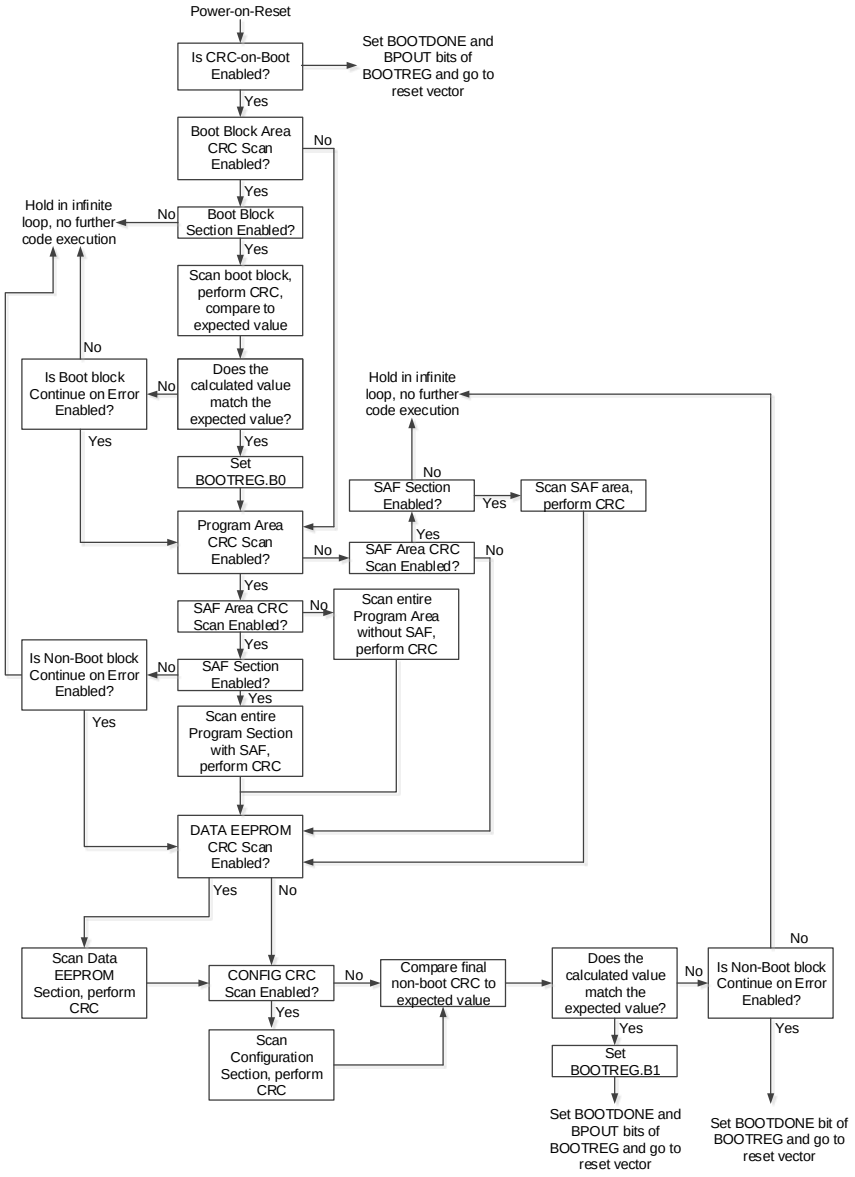
1. CRC-on-Boot

The CRC-on-Boot feature of the microcontroller, when enabled, performs a CRC on selected areas of non-volatile memory upon device power-up before any user code is executed. It is set up purely through Configuration Words, and the function of the module is performed by hardware on the device without any user code intervention to function. Figure 1-1 shows a flowchart outlining the functionality of the CRC-on-Boot feature.

Figure 1-1. CRC-on-Boot Flowchart



The CRC-on-Boot controls which sections of NVM to scan and 32-bit CRC to run on, as well as the polynomial and seed for the CRC calculation. This feature scans all chosen areas of memory and runs the CRC calculation on the

data contained in those areas of memory. It then compares the result of that calculation against the preconfigured expected result and indicates whether the expected result matches the calculated result, identifying whether any of the scanned area of memory has deviated from the expected values.

1.1 Scanning Segments

The CRC-on-Boot can scan the following primary areas of NVM:

- Program Memory Boot Sector
- Non-Boot NVM

The Non-Boot NVM is further subdivided into four smaller segments:

- Non-Boot Program Memory
- Storage Area Flash
- Data EEPROM
- Configuration Words

Scanning of all five segments, the program memory boot sector and the four segments of non-boot NVM can be individually enabled or disabled. In addition, the two primary areas that the CRC-on-Boot scans will each have their own set of Configuration registers to store their polynomial, seed, and expected result values in. It also separates Status bits to indicate whether a CRC mismatch is found in that primary area, and Configuration bits to determine if execution will continue upon detecting a mismatch or if the device will instead trap.

Note: The boot area calculation is completed first, so unless the $\overline{\text{BOOTCOE}}$ bit is cleared, a mismatch in the boot section of the CRC will cause the non-boot section calculation to not occur.

1.2 CRC-on-Boot Output

When the CRC-on-Boot operation begins, it clears the BPOUT bit of the BOOTREG register. If all enabled CRC calculations are found to match their respective expected values, the BPOUT bit is set and normal user code execution begins. The BPOUT bit also controls the state of any selected output pin, pulling the pin low until a successful CRC match is determined, and then either driving or releasing the pin high. The output pin can be enabled or disabled and steered to several output pins, as well as configured in either Normal or Open-Drain modes.

Note: Any CRC calculations that are not enabled are treated as if the calculated and expected values match.

2. CRC Module

The CRC-on-Boot feature uses the 32-bit CRC module to perform its CRC calculations. The polynomial and seed values (CRCXOR and CRCACC) are loaded from their respective Configuration Words. For the boot section, the BCRCPOL Configuration registers are loaded into the CRCXOR registers and the BCRCSEED Configuration registers are loaded into the CRCACC registers. For the other sections, CRCPOL is loaded into CRCXOR and CRCSEED is loaded into CRCACC. For boot, application and SAF sections are the following:

- CRC input data is set to 16 bits (CRCCON2 = 0x0F)
- Polynomial is set to 32 bits (CRCCON1 = 0x1F)
- CRC shifts left (MSb first, SHIFTM = 0)
- Accumulator is augmented with zeroes (ACCM = 1)

For data EEPROM and Configuration scans, the CRC settings remain the same, with the exception that the CRC input data is set to 8 bits, instead of 16 bits (CRCCON2 = 0x07).

The area that is selected for scanning is determined by several factors, both inside and outside the CRC-on-Boot. The three major sections that are affected by outside sources are the program, SAF, and boot sections. These three sections are all one contiguous area of NVM, just broken into different sized sections. The boot section scan will adjust to match the configured size of the boot section, which is determined by the BOOTSIZ Configuration bits, and the program memory section will adjust to match. The program memory section will scan to the end of program memory, unless the SAF section is enabled, at which point the SAF scan must be enabled separately. The data EEPROM scan will scan the entirety of the data EEPROM section of memory. The configuration scan will scan all Configuration bytes, except for the four Configuration bytes of the non-boot section's expected value as scanning these bytes would make the process impossible.

Notes:

1. Enabling scans on a section of memory that is not enabled (for example, enabling scans of the SAF section when SAFEN is disabled) is treated as an expected value mismatch by the CRC-on-Boot.
2. The CRC-on-Boot uses whichever clock is selected by the RSTOSC Configuration bits of the device. This is important as configuring the source clock to be a slow source (such as 32k LFINTOSC or 32k SOSC input sources) can make the CRC-on-Boot take an undesirably long time to complete. If operation at a slower clock frequency is desired (for example, power consumption purposes), a solution is to set the RSTOSC Configuration bits to a higher clock frequency, and then do a clock switch to the slower frequency at the beginning of user code. This will allow the CRC-on-Boot to finish in a reasonable amount of time, while then allowing the device to run at a slower speed.

3. CRC-on-Boot Configuraion

3.1 Scan Area Enabling and Selection

Enabling the CRC-on-Boot is achieved by clearing the BOOTPOR Configuration bit. Enabling the scanning of individual segments is controlled by the CFGSCEN, DATSCEN, SAFSCEN, APPSCEN, and BOOTSCEN Configuration bits. By default, the module will halt operation of the device upon detecting a mismatch. Clearing the COE or BOOTCOE bits will disable this functionality and allow the device to continue with further operation. As each section (boot or non-boot) is completed, it will set or clear the B0 and B1 bits of BOOTREG to indicate if each section passed or failed its CRC.

3.2 Output Control

The output pin is configured through the ODCON, BPEN, and BOOTPINSEL Configuration bits. The BPEN bit enables or disables the output pin, the BOOTPINSEL bits choose which pin will have the module output, and the ODCON bit controls whether the output pin will drive both high- and low-going signals or be in Open-Drain mode (only driving low-going signals). The level of the output pin is determined by the BPOUT bit of the BOOTREG register. This bit is automatically set to the appropriate level by the CRC-on-Boot after finishing its calculation, but can also be controlled in software to manually control the pin selected by the BOOTPINSEL bit.

Note: If the BPEN bit is cleared, the pin selected by BOOTPINSEL is fully controlled by the CRC-on-Boot and cannot be used for GPIO, PPS, or analog functions.

Table 3-1. CRC-on-Boot Output Pin Selections

BPEN	BOOTPINSEL	Output Pin
1	x	None
0	00	RA4
0	01	RA2
0	10	RC4
0	11	RC5

3.3 Polynomial, Seed, and Expected Value Configuration and Calculation

If the CRC-on-Boot is enabled, it will run on all Power-on Reset (POR) events. If the calculation completes and continues to user code execution (either through matching the expected value or the continue-on-error feature is enabled), the BOOTDONE bit in BOOTREG will be set. With this bit set, all non-POR events will immediately go to user code without performing a CRC-on-Boot. However, if such a calculation is desired after a non-POR event, clearing this bit will cause the CRC-on-Boot to occur on the next Reset of any source.

The polynomial and seed values, as previously mentioned, are taken directly from their respective Configuration bytes and loaded into the CRC module's associated bytes. For more details on CRC calculations, see **"TB3128: CRC and Memory Scan on 8-bit Microcontrollers"**. For the expected value, the calculation must be done knowing the areas of the memory that will be scanned and checked. The expected value is loaded into respective Configuration registers, with the BCRCRES registers being compared against the boot section's final calculated CRC value, and the CRCRES registers being compared against the non-boot sections' final calculated CRC value.

4. Example Use Cases

The examples below show a few example Configuration settings for different use cases for the CRC-on-Boot. Example 4-1 shows a case in which there is no boot or SAF sectors of program memory. In this case, only the application memory is scanned, the output is an open-drain setup on pin RA2 (for a shared error line), and the device will not continue upon encountering an error. This keeps the whole system in Reset for use in a safety-critical system.

Example 4-2 shows a case that scans both the boot and application segments of program memory. If an error in the boot segment occurs, it will not continue as that error is not recoverable. But if an error is found in the application segment, the boot segment can react to and (potentially) allow for a fix to errors in the application segment.

Example 4-3 shows a case that only scans the data EEPROM. As such, all error handling can be performed at the beginning of the application code, and no output signal or halting on error is required with both features being disabled.

Example 4-1. Application Code only, no Boot Sector or SAF, open-drain on pin RA2, no continue on error

```
CONFIG7=0xFF //Debug disabled, SAF disabled, Boot Block Disabled
CONFIG9=0xCD //Output pin is enabled and open-drain, and on pin RA2
CONFIG11=0x7B //CRC-on-Boot enabled, Application section enabled
```

Example 4-2. Scan both Boot and Application code, no continue on error for Boot, continue on error

```
CONFIG7=0xF4 //Debug disabled, SAF disabled, Boot Block enabled, 16 kW Boot
Block
CONFIG9=0xEC //Output pin is enabled and drives both high and low on pin RA4
CONFIG11=3A  //CRC-on-Boot enabled, Continue on Error for Non-Boot enabled,
Application scan enabled
             //Boot scan enabled, Continue on Error for Boot disabled
```

Example 4-3. Scan only Data EEPROM, no output pin, continue on error

```
CONFIG7=0xF4 //Debug disabled, SAF disabled, Boot Block enabled, 16 kW Boot
Block)
CONFIG9=0xEC //Output pin is enabled and drives both high and low on pin RA4)
CONFIG11=3A  //CRC-on-Boot enabled, Continue on Error for Non-Boot enabled,
Application scan enabled
             //Boot scan enabled, Continue on Error for Boot disabled)
```

5. Conclusion

Cyclic Redundancy Check (CRC) is a common method used for verifying the integrity of data in Non-Volatile Memory (NVM) on PIC microcontrollers. The CRC-on-Boot is a feature of some 32-bit CRC modules on 8-bit PIC microcontrollers, which allows for scanning and verifying integrity of this data while being independent of application code. This technical brief outlines the main features of the CRC-on-Boot, as well as several errors to avoid in its use. It has also outlined and demonstrated several example use cases with configuration settings for using the feature.

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