
MCP3X6XR Silicon Errata and Data Sheet Clarification

The functionality of the MCP346X/356XR Two/Four/Eight-Channel 24-Bit Delta-Sigma ADCs is described in the device Data Sheets (**DS20006404C** and **DS20006391C**, respectively), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the MCP346XR/356XR silicon.

Contact Microchip for the latest silicon fix.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Applies to the current silicon revision (Rev. A).

1. Module: Data-Ready Events

A Data-Ready (\overline{DR}) Conversion complete event is indicated using three independent mechanisms:

1. The $\overline{DR_STATUS}$ Bit in the SPI STATUS Byte
2. The $\overline{DR_STATUS}$ Bit in the IRQ Register
3. An \overline{IRQ} Pin falling edge.

If a \overline{DR} event occurs between the Command Byte of an IRQ Register read operation and the reception of the IRQ Register Data Byte, the event will not be indicated in the Data Byte or any subsequent IRQ Register read operations where the CS Pin is toggled between operations.

The \overline{IRQ} Pin and STATUS Byte mechanisms to indicate a DR event are not affected by this errata.

Work around

If Data-Ready (\overline{DR}) events need to be detected via the STATUS Byte, the state of the $\overline{DR_STATUS}$ Bits for both the STATUS Byte and the IRQ Register can be verified within a single communication sequence. To do this, a read command of the IRQ Register must be executed.

During the transmission of the IRQ Register read command over SDI, a STATUS Byte containing the state of the $\overline{DR_STATUS}$ Bit will be simultaneously transmitted over SDO.

Continued clocking of the SCK Pin while the \overline{CS} Pin remains asserted low will transmit the Data Byte of the IRQ Register containing the state of the $\overline{DR_STATUS}$ Bit. Comparing the state of the $\overline{DR_STATUS}$ Bit of the STATUS Byte with the $\overline{DR_STATUS}$ Bit of the IRQ Register can determine if a new Data-Ready event has occurred.

If either mechanism indicates a $\overline{DR_STATUS}$ Bit state of '0', new data is available and can be read from the ADCDATA Register. If neither mechanism indicates a $\overline{DR_STATUS}$ Bit state of '0', no new data is available since the last check.

If Data-Ready (\overline{DR}) events need to be detected via the IRQ Register, the user should leave the \overline{CS} Pin asserted low while continuously applying SCK pulses to repeatedly read the IRQ Register until the $\overline{DR_STATUS}$ Bit indicates a Data-Ready (\overline{DR}) event has occurred.

Data Sheet Clarifications:

In the MCP346XR/356XR Data Sheets (**DS20006404C** and **DS20006391C**, respectively), the following clarifications and corrections should be noted:

- a) None to report at this time.

MCP3X6XR

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (June 2024)

- Initial release of this document.

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Worldwide Sales and Service

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Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
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