

Using Low Power Modes in AT91SAM7L Microcontrollers

1. Scope

The Atmel® AT91SAM7L ARM® Thumb®-based microcontroller family features several low-power modes that can be used to optimize power consumption in applications where low power is a key.

The purpose of this document is to describe how to enter and exit low-power modes and to give suggestions on how to cope with the main constraints related to using low-power modes.

The source code can be found at [AT91 Software Packages](#) for AT91SAM7L-EK and AT91SAM7L-STK.

2. Power Supply Considerations

The AT91SAM7L128/64 is particularly adapted for battery operated applications such as calculators, toys, remote controls, medical devices, mobile phone accessories and wireless sensors. It can be directly supplied from any Lithium battery or a double NiMH, NiCd and Alkaline battery.

The chip embeds an adjustable voltage regulator, a regulated charge pump and a LCD voltage regulator allowing it to operate with a single supply source in the range of 1.8V to 3.6V even with the LCD display running.

Depending on the application requirements and the power saving strategy, several power supply topologies are available.

The different powering schemes are illustrated through the diagrams that follow.



AT91 ARM Thumb-based Microcontrollers

Application Note



Figure 2-1. Typical Single Supply Topology (the Charge Pump Supplies the LCD Regulator)

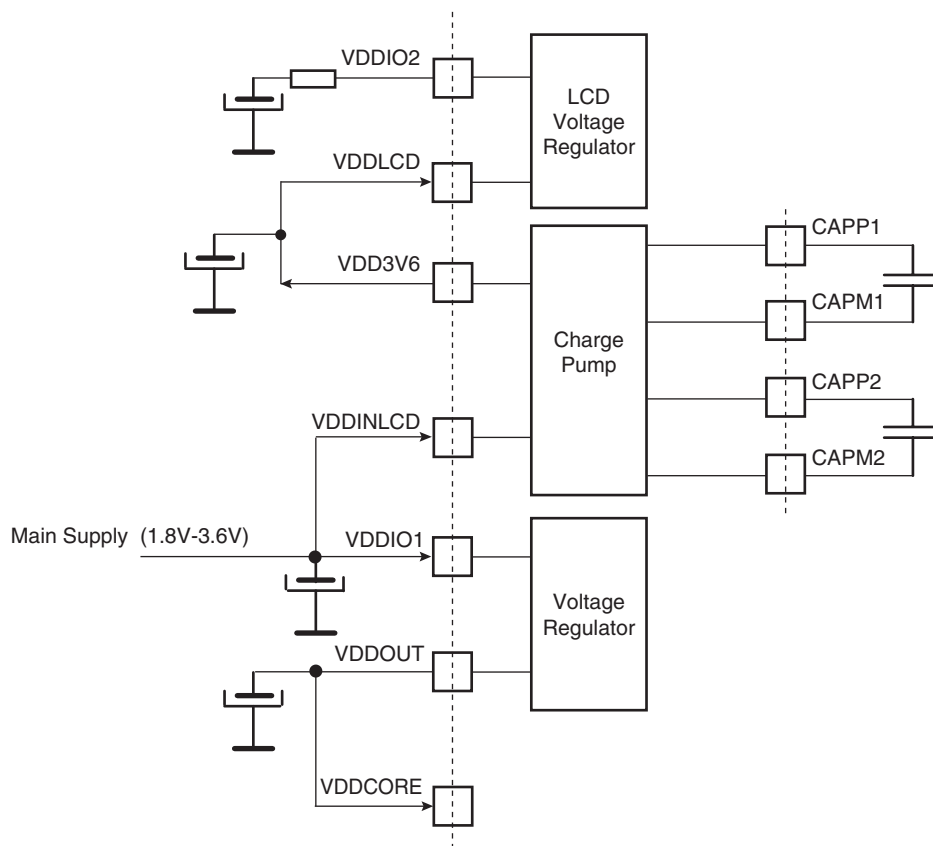


Figure 2-2. Dual Supply Internal Contrast Topology (The LCD Regulator is Externally Supplied)

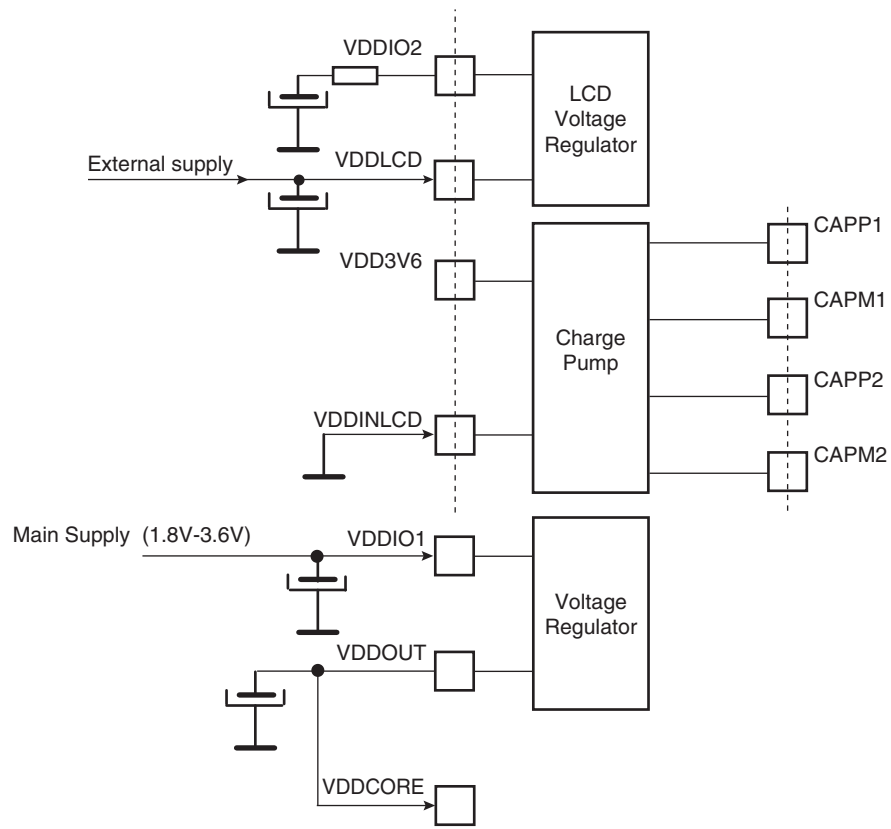
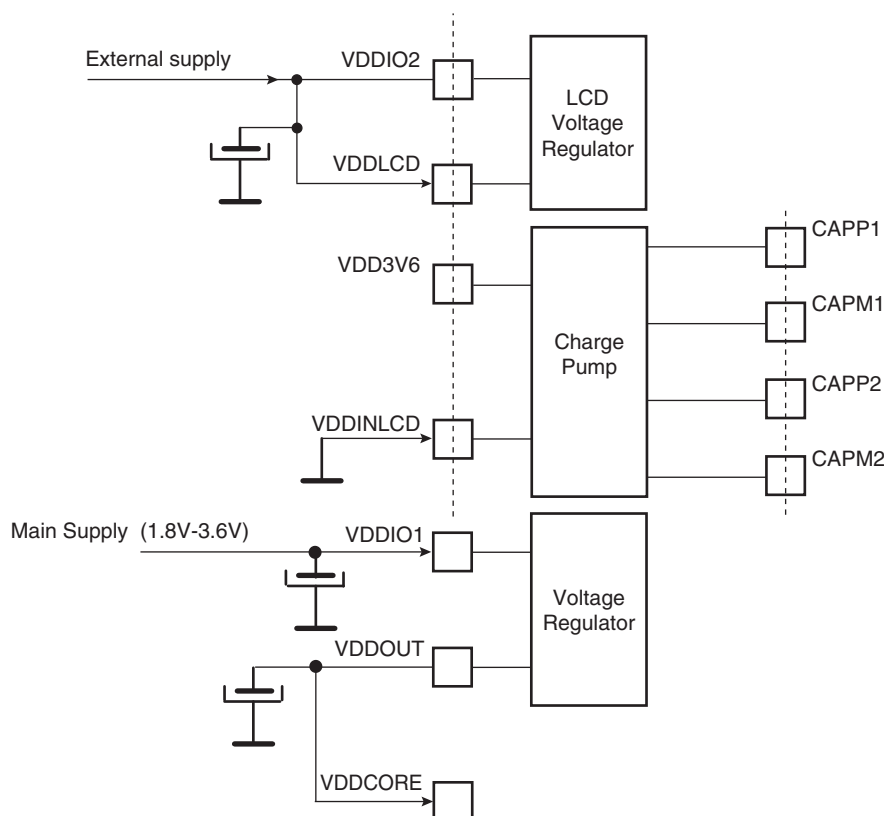


Figure 2-3. Dual Supply External Contrast Topology (The Charge Pump and the LCD Regulator are Not Used)



For further hardware considerations, please refer to the Application note referenced, [“AT91SAM7L Microcontroller Series Schematic Check List”](#) available on Atmel’s web site.

For further details on register settings, please refer to the [AT91SAM7L series](#) datasheet and the “Electrical Characteristics” contained therein.

Depending on the hardware power supply topology, the LCD supply source has to be selected by software.

By default, both the internal and external supply sources are not selected. The charge pump and the LCD regulator are off.

The supply source can be selected by writing the relevant value in the LCDMODE field and writing 0xA5 in the KEY field of the SUPC_MR register. Once the supply source is selected, software must wait until the LCD controller can be used by checking that the LCDS field of the SUPC_SR is set to 1.

3. Low-Power Modes Overview

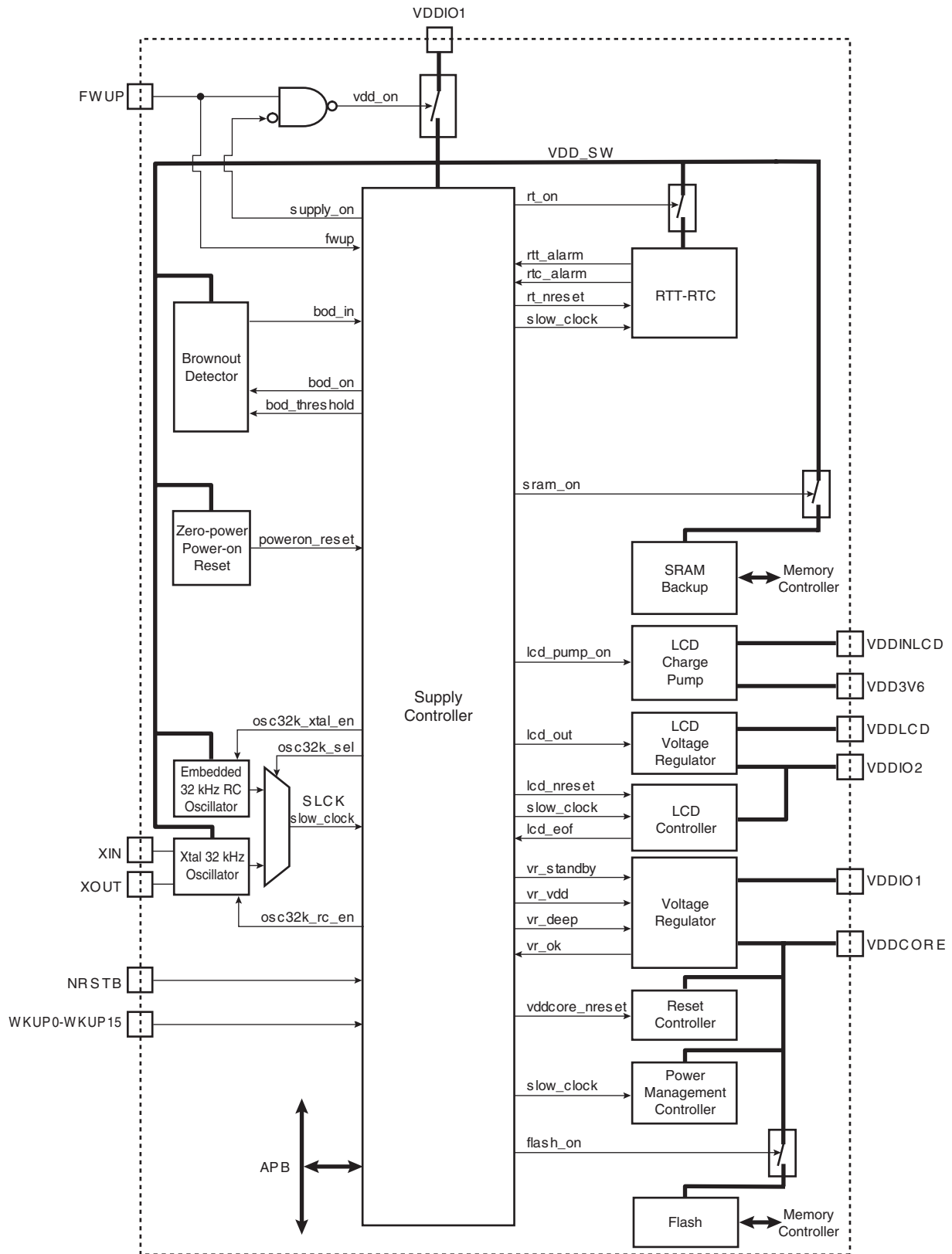
3.1 Introduction

The AT91SAM7L128/64 embeds a Supply Controller (SUPC) and a Power Management Controller (PMC) which respectively control the supply voltages and the clocking of the system.

The combined features of the Supply Controller and the Power Management Controller provide a wide range of low power modes allowing system designers to choose the best trade-off between power consumption, wake-up time, clock frequency, wake-up sources and context backup.

[Figure 3-1 on page 6](#) gives a comprehensive overview of the Supply Controller.

Figure 3-1. Supply Controller Block Diagram



3.2 Off (Power Down) Mode

In Off (power down) mode, the entire chip is shutdown. Only a low level on the FWUP pin can activate the AT91SAM7L128/64 (by a push button for example). Internally, except for FWUP pin through VDDIO1, none of the chip is supplied.

Once the internal main power switch is active, the 32 kHz RC oscillator and the Supply Controller are supplied, then the core and peripherals are reset and started to then set the AT91SAM7L128/64 chip in active mode. Note that if the user does not need to use this mode, FWUP must be tied to ground.

At first power-up, if FWUP is tied high, the chip enters Off mode, PIOA and PIOB pins states are undefined, PIOC and NRST pins are initialized as high impedance inputs.

Once the device enters active mode, the core and the parallel input/output controller are reset. Then, if the chip enters off mode, PIOA and PIOB pins are configured as inputs with pull-ups and PIOC pins as high impedance inputs. Current consumption in this mode is typically 100 nA.

3.3 Backup Mode

In Backup mode, the supply controller, the zero-power power-on reset and the 32 kHz oscillator (software selectable internal RC or external crystal) remain running. The voltage regulator and the core are switched off.

Prior to entering this mode, the RTC, the backup SRAM, the brownout detector, the charge pump, the LCD voltage regulator and the LCD controller can be set on or off separately.

When entering this mode, all PIO pins keep their previous states, they are re-initialized as inputs with pull-ups at wake-up.

The AT91SAM7L128/64 can be awakened from this mode through the FWUP pin, an event on WUP0-15 pins, or an RTC alarm or brownout event.

Current consumption is 3.5 μ A typical without the LCD contribution.

3.4 Wait Mode

In Wait mode, it is highly advised to set the voltage regulator in deep mode and decrease its output voltage to minimum in order to decrease leakage in the digital core. The core and peripherals are not clocked. From this mode, a fast start-up is available through an event on WUP0-15 pins.

When entering and exiting this mode, all PIO pin states remain unchanged.

Current consumption in this mode is typically 9 μ A.

3.5 Idle Mode

The processor is in Idle mode which means that the core is not clocked but the Master clock (MCK) remains running. The processor can be awakened by an IRQ or an FIQ.

Current consumption in this mode depends on Master clock speed and the number of peripherals enabled.

3.6 Active Mode

The total dynamic power consumption is less than 30 mA at full speed (36 MHz) when running out of the Flash. The Power Management Controller can be used to adapt the frequency and the regulator output voltage can be adjusted to optimize power consumption.

3.7 Low Power Mode Summary Table

The modes detailed above are the main modes. In off mode, no options are available but once the Shutdown Controller is set to on, each part can be set to on, or off, separately and more modes can be active. The table below shows a summary of the configurations of the low power modes.

Table 3-1. Low Power Mode Configuration Summary

Mode\Supplied part	Main power switch	SUPC, 32 kHz Osc, POR	2 MHz Osc	BOD	RTC	LCD (Charge pump and LCD regulator)	Backup SRAM	Flash Memory	Regulator	PLL	Core	Potential Wake-up Sources
Off Mode												FWUP pin
Backup Mode	X ⁽¹⁾	X		O ⁽²⁾	O	O	O					FWUP pin WUP0-15 pins BOD alarm RTC alarm
Wait Mode	X	X		O	O	O	X	O	Deep Mode	O	X ⁽³⁾	Fast start-up through WUP0-15 pins
Idle Mode	X	X	O	O	O	O	X	O	Deep Mode	O	X ⁽³⁾	IRQs FIQ
Active Mode	X	X	O	O	O	O	X	O	Normal Mode	O	X	

Notes: 1. This indicates that the part is supplied and active.
2. This indicates that the part is optionally supplied and active.
3. In this mode, the core is supplied but not clocked.

4. Using Low Power Modes

4.1 Off (Power Down) Mode

4.1.1 Entering Off (Power Down) Mode

The chip enters Off mode automatically if FWUP pin is tied high at when first powered up.

When the chip is in active mode, Off mode can be entered by setting the SHDWN field and writing 0xA5 in the KEY field of the SUPC_CR register.

If the LCD controller is running, the chip will enter Off mode after displaying the end of the current frame by setting the SHDWNEOF field and writing 0xA5 in the KEY field of the SUPC_CR register.

Asserting the NRSTB pin low from any mode will release the backup power switch which leads to entering Off mode (if FWUP pin is tied high).

4.1.2 Exiting Off Mode

As soon as FWUP pin is tied low longer than 30 slow clock cycles, the main power switch is enabled, the core and peripherals reset and the chip enters active mode.

4.2 Backup Mode

4.2.1 Programming Backup Mode Wake-up Sources

Backup mode can be exited from several wake-up sources that must first be programmed prior to entering this mode.

4.2.1.1 FWUP Pin Wake-up Source

A low level on FWUP pin can wake-up the chip from Backup mode by setting the FWUPEN field in the SUPC_WUMR register.

By default, when this wake-up source is activated, the chip exits Backup mode as soon as a low level is detected on FWUP pin. The FWUP pin level can be de bounced with 3, 32, 512, 4096 or 32768 slow clock cycles by writing the appropriate value, from 0x1 to 0x5, in the FWUPDBC field of the SUPC_WUMR register.

4.2.1.2 WUP0-15 Pins Wake-up Sources

A level transition on WUP0-15 pins can wake-up the chip from Backup mode by setting the corresponding WKUPEN0-15 field in the SUPC_WUIR register.

By default, when a wake-up source is activated, the chip exits Backup mode as soon as a level transition is detected on the enabled wake-up source pin. The WUP0-15 pin transition level can be debounced with 3, 32, 512, 4096 or 32768 slow clock cycles by writing the relevant value in the WUPDBC field of the SUPC_WUMR register.

By default, when this wake-up source is activated, a high to low transition level wakes-up the chip, polarity can be inverted by setting the corresponding WKUPT0-15 field in the SUPC_WUIR register.

Please note that WUP0-15 pins can detect a level transition and operate as wake-up sources only if they are setup as inputs in the PIO controller.

4.2.1.3 *Brownout Alarm Wake-up Source*

The brownout wake-up alarm can be enabled by setting the BODEN field in the SUPC_WUMR register.

By default, the brownout detector is disabled, it can be scheduled to monitor VDDIO1 continuously or periodically every 32, 256 or 2048 slow clock cycles by writing the relevant value in the BODSMPL field of the SUPC_BOMR register.

The brownout threshold voltage is programmable in the range of 1.9 to 3.4V by writing the appropriate value in the BOTH field of the SUPC_BOMR register.

4.2.1.4 *RTC Alarm Wake-up Source*

By default, the RTC is not supplied, it can be powered on by setting the RTON field and writing 0xA5 in the KEY field of the SUPC_MR register.

The RTC wake-up alarm source is enabled by setting the RTCEN field in the SUPC_WUMR register.

The RTC wake-up alarm event has to be programmed through the RTC user interface.

4.2.2 **SRAM Backup**

The AT91SAM7L128/64 features 2 Kbytes of SRAM that can be backed up when entering Backup mode, the content of this memory space will be unchanged upon waking up from Backup mode.

Activating SRAM backup is performed prior to entering Backup mode by setting the SRAMON field and writing 0xA5 in the KEY field of the SUPC_MR register.

4.2.3 **LCD Controller**

The charge pump, the LCD regulator and the LCD controller can be left running while the chip is in Backup mode.

4.2.3.1 *Switch On the LCD Display Before Entering Backup Mode*

Once the LCD supply source is selected (Please refer to section [Section 2. “Power Supply Considerations” on page 1](#)), the LCD controller can be enabled by setting the LCDEN field of the SLCDC_CR register.

Software should wait until the LCD controller is ready by checking that the ENA field of the SLCDC_SR is set to 1.

Please note that LCD configuration parameters such as frame rate, number of segments, number of commons, type of bias, etc., should be programmed before activating the LCD controller through the LCD user interface.

4.2.3.2 *Switch Off the LCD Display Before Entering Backup Mode*

The LCD controller can be disabled after the end of a frame by setting the LCDDIS field of the SLCDC_CR register. Software should wait until the end of the current frame and that the LCD controller has tied all commons to ground by checking that the ENA field of the SLCDC_SR is set to 0.

The LCD controller can also be disabled instantaneously through a software reset by setting the SWRST field of the SLCDC_SR register. In this case, all commons are immediately tied to ground.

Please note that before entering Backup mode, the charge pump and the LCD Voltage regulator should be switched off through the SUPC_MR register in order to optimize power consumption.

4.2.4 Input/Output States

As noted previously, all PIO pins preserve their state when the chip enters Backup mode. It is up to the user to prevent PIOs from sinking or sourcing current in order to save power when the chip is in Backup mode.

Prior to entering Backup mode, particular attention has to be paid between the configured output logical states and the connected external components, which may generate power consumption. In order to avoid internal current sinking, it is also highly recommended to disable internal pull-up resistors of any pin configured as low-level output.

4.2.5 Entering Backup Mode

Backup mode is entered by setting the VROFF field and writing 0xA5 in the KEY field of the SUPC_CR register.

It takes about 2 slow clock cycles resynchronization between the writing of VROFF bit and the effective entry in Backup mode. In the meantime, the master clock remains running and the core continues to fetch the following instructions. It is highly recommended to add an infinite loop after setting VROFF, in order to avoid execution of undesired instructions.

4.2.6 Exiting Backup Mode

Backup mode is exited as soon as an enabled wake-up event occurs. The core and all peripherals are reset, the PIOs state are lost and initialized as inputs with pull-ups.

4.3 Wait Mode

4.3.1 Programming Wait Mode Fast Start-up Sources

Wait mode can be exited from several asynchronous fast start-up sources that have to be programmed prior to entering this mode. As soon as a fast start-up condition is detected, the embedded 2 MHz fast RC oscillator is automatically restarted and selected to clock the core and the peripherals.

A high to low level transition on WUP0-15 pins can wake-up the chip from Wait mode by setting the corresponding FSTT0-15 field in the PMC_FSMR register.

Please note that WUP0-15 pins can detect a level transition and operate as fast start-up sources only if they are setup as inputs in the PIO controller.

4.3.2 Flash Memory Power Supply

The Flash memory is automatically switched on when the core power supply is enabled at start up.

Before entering Wait mode, the Flash memory power supply can be switched off by opening the Flash memory power switch (connected to VDDCORE) in order to save standby power consumption. Switching off the Flash memory power supply is done by setting to 0 the FLASHON bit and writing 0xA5 in the KEY field of the Supply Controller Mode Register (SUPC_MR).

If the program is running out of Flash after a fast start-up, the Flash memory power supply can be restored by setting to 1 the FLASHON bit and writing 0xA5 in the KEY field of the Supply Controller Mode Register (SUPC_MR).

When enabling or disabling the Flash memory power supply, software should wait that the FLASHS flag state in the SUPC_SR is correctly set.

Please note that before setting FLASHON to 0, the SUPC_FWUT register must be programmed with the relevant value in accordance with the Flash memory wake up time specification (refer to “Electrical Characteristics” section of the [AT91SAM7L series](#) datasheet).

The Flash memory power supply disable and enable instructions must be to be executed out of SRAM.

4.3.3 Voltage Regulator

Before entering Wait mode, the voltage regulator output voltage should be adjusted to a minimum in order to reduce power consumption. Adjusting the voltage regulator output voltage to 1.55V can be done by writing 0x02 in the VRVDD field and writing 0xA5 in the KEY field of the SUPC_MR register.

In order to reduce leakage to a minimum, the voltage regulator must be switched to deep mode prior to entering Wait mode. Enabling deep mode is done by setting to 1 the VRDEEP field of the SUPC_MR register. Going back to normal mode is done by setting to 0 the VRDEEP field of the SUPC_MR register.

Voltage regulator deep mode can also be used when the chip is running in active mode as long as VDDCORE power consumption remains below the maximum DC output current (refer to “Electrical Characteristics” section of the [AT91SAM7L series](#) datasheet).

4.3.4 PLL Management

In order to save power consumption, the PLL should be switched off prior to entering Wait mode. Switching off the PLL can be done by writing to 0x00 the MUL field of the CKGR_PLLR register.

Note that the STMODE field of the CKGR_PLLR register must be set to 0x02 when the PLL is shutdown.

Re-enabling the PLL can be performed by writing a value higher than 0 in the MUL field.

Whenever the PLL is re-enabled or one of its parameters is changed, the LOCK bit in PMC_SR is automatically cleared.

Software must wait until the LOCK bit is set to 1 to ensure that the PLL clock is ready. The transient time depends on the PLL filter and the target frequency. The PLL filter and transient time can be calculated using a specific tool provided by Atmel.

The number of slow clock cycles required to cover the PLL transient time has to be programmed into the PLLCOUNT field.

The value written in the PLLCOUNT field in CKGR_PLLR is loaded in the PLL counter which will be decremented at slow clock speed until it reaches 0. At this time, the LOCK bit is set in PMC_SR and can trigger an interrupt to the processor.

Two PLL startup schemes are available:

- The fast startup scheme allows the PLL to reach at least 70% of its target frequency in less than 60 μ s. In this mode the STMODE field must be set to 0x0 and the PLLCOUNT field can be programmed at 0x01 in the CKGR_PLLR register.
- The normal startup procedure of the PLL is performed when the STMODE field of the CKGR_PLLR register is set to 0x02. In this startup scheme, the PLLCOUNT field must be set with the relevant value function of the programmed PLL frequency.

4.3.5 Brownout Detector

The brownout detector can be left running while the chip is in Wait mode, but it can not wake it up.

By default, the brownout detector is disabled, it can be scheduled to monitor VDDIO1 continuously or periodically every 32, 256 or 2048 slow clock cycles by writing the relevant value in the BODSMPL field of the SUPC_BOMR register.

The brownout threshold voltage is programmable in the range of 1.9V to 3.4V by writing the appropriate value in the BOTH field of the SUPC_BOMR register.

In Wait mode, the brownout detector can generate a system reset when VDDIO1 voltage drops below the programmed threshold. The brownout reset feature is enabled by setting to 1 the BODRSTEN field in the SUPC_BOMR register.

4.3.6 LCD Controller

The charge pump, the LCD regulator and the LCD controller can be left running while the chip is in Wait mode.

4.3.6.1 *Switch On the LCD Display Before Entering Wait Mode*

Once the LCD supply source is selected (Refer to section [Section 2. "Power Supply Considerations"](#)), the LCD controller can be enabled by setting the LCDEN field of the SLCDC_CR register.

Software should wait until the LCD controller is ready by checking that the ENA field of the SLCDC_SR is set to 1.

Note that LCD configuration parameters such as frame rate, number of segments, number of commons, type of bias, etc., should be programmed before activating the LCD controller through the LCD user interface.

4.3.6.2 *Switch Off the LCD Display Before Entering Wait Mode*

The LCD controller can be disabled after the end of a frame by setting the LCDDIS field of the SLCDC_CR register. Software should wait until the end of the current frame and that the LCD controller has tied all commons to ground by checking that the ENA field of the SLCDC_SR is set to 0.

The LCD controller can also be disabled instantaneously through a software reset by setting the SWRST field of the SLCDC_SR register. In this case, all commons are instantaneously tied to ground.

Note that before entering Wait mode, the charge pump and the LCD Voltage regulator should be switched off through the SUPC_MR register in order to optimize power consumption.

4.3.7 Input/Output States

As noted previously, all PIO pins preserve their state when the chip enters Wait mode. It is up to the user to prevent PIOs from sinking or sourcing current in order to save power when the chip is in Wait mode.

Prior to entering Wait mode, particular attention has to be paid between the configured output logical states and the connected external components which may generate power consumption. In order to avoid internal current sinking, it is also highly recommended to disable internal pull-up resistors of any pin configured as low-level output.

4.3.8 Entering Wait Mode

Wait mode is entered by disabling the 2 MHz fast RC oscillator, if it is selected as Master Clock. The 2 MHz fast RC oscillator can be selected as Master Clock (MCK) to clock the core and peripherals (PCK) by writing 0x01 in the CSS field of the PMC_MCKR register. The Master Clock (MCK) can be divided in the range of 1 to 64 by writing the relevant value in the PRES field of the PMC_MCKR register.

Wait mode is entered by setting to 0 the MAINCKON field and writing 0x37 in the KEY field of the CKGR_MOR register.

It takes up to 3.5 main clock cycles resynchronization between the writing of MAINCKON bit and the effective entry in Wait mode. In the meantime, the master clock remains running and the core continues to fetch the following instructions. It is highly recommended to add a loop while waiting for the MAINCKON bit to return to 1, (at wake up) after the clear command, in order to avoid execution of undesired instructions.

If the Flash memory power supply is left switched on when the device enters Wait mode, it is recommended to execute the 2 MHz fast RC oscillator disable command in SRAM. This will prevent that Flash memory remains in read mode when the clock is disabled, hence generating over consumption.

4.3.9 Exiting Wait Mode

As soon as the fast start-up event occurs, Wait mode is exited, the PMC automatically restarts the embedded 2 MHz fast RC oscillator and the core executes the next instruction of the program counter.

4.4 Idle Mode

4.4.1 Programming Idle Mode Wake-up Sources

Idle mode can be exited from any occurring IRQ or FIQ that has been enabled prior to entering this mode.

4.4.2 Clock Selection

In order to reduce power consumption to a minimum, it is highly recommended to slow down the master clock as much as possible.

Selecting the Slow Clock (SLCK) as Master Clock (MCK) is done by writing to 0x00 the CSS field of the PMC_MCKR register.

The user can select the crystal oscillator to be the source of the slow clock, as it provides a more accurate frequency. The command is made by setting to 1 the XTALSEL bit and writing 0xA5 the Key field of the SUPC_CR register. This results in a sequence which first enables the crystal oscillator, then waits for 32,768 slow clock cycles, then switches the slow clock on the output other crystal oscillator and then disables the RC oscillator to save power. The switch of the slow clock source is glitch free. Software should wait that the switch sequence is completed by checking that the OSCSEL bit of the SUPC_SR register is set to 1. Returning to the RC oscillator is only possible by shutting down the backup power supply.

The Master Clock (MCK) can be divided in the range of 1 to 64 by writing the relevant value in the PRES field of the PMC_MCKR register.

If the CSS or PRES fields are modified, the MCKRDY bit in the PMC_SR register will be set to 0 to indicate that the master clock and the processor clock are not ready yet. Software must wait for MCKRDY bit to be set to 1 again before using the master clock.

The master clock can be slowed down to 512 Hz if the slow clock is divided by a factor of 64.

4.4.3 PLL

In order to save power consumption, the PLL should be switched off prior to entering idle mode. Switching off the PLL can be done by writing to 0x00 the MUL field CKGR_PLLR register. Refer to section [Section 4.3.4 “PLL Management” on page 12](#).

4.4.4 Main Clock

If the 2 MHz fast RC oscillator is not used to clock the system in idle mode, it should be disabled by setting to 0 the MAINCKON field and writing 0x37 in the KEY field of the CKGR_MOR register. Note that software should wait that the MAINRDY flag is set to 0 in the PMC_SR register before the 2 MHz fast RC oscillator disable command is effective.

4.4.5 Voltage Regulator

Before entering idle mode, the voltage regulator output voltage should be adjusted to a minimum in order to reduce power consumption. In order to reduce leakage to a minimum, the voltage regulator must be switched to deep mode prior to entering idle mode. Refer to section [Section 4.3.3 “Voltage Regulator” on page 12](#).

4.4.6 Flash Memory Power Supply

Before entering idle mode, the Flash memory power supply can be switched off by opening the Flash memory power switch (connected to VDDCORE) in order to save standby power consumption. Refer to section [Section 4.3.2 “Flash Memory Power Supply” on page 11](#).

4.4.7 Brownout Detector

The brownout detector can be left running while the device is in idle mode but it can not generate an interrupt to wake it up.

4.4.8 Entering Idle Mode

The processor idle mode is achieved by disabling the processor clock, which is automatically re-enabled by any enabled fast or normal interrupt, or by the reset of the system.

The Power Management Controller features a Processor Clock Controller (PCK) that implements the processor idle mode. The processor clock can be disabled by writing to 1 the PCK bit in the PMC_SCDR register. The status of this clock can be read in the PMC_SCSR register.

When the Processor Clock is disabled, the current instruction is finished before the clock is stopped, but this does not prevent data transfers from other masters of the system bus.

4.4.9 Exiting Idle mode

As soon an IRQ or FIQ is detected, idle mode is exited, the PMC automatically re-enables the processor clock (PCK) and the core executes the next instruction of the program counter.

4.5 Active mode

While the device is running in active mode, power consumption can be optimized by using the Supply Controller and the Power Management Controller.

4.5.1 Clock Sources

Core clock speed should be adjusted in accordance with application requirements. Unused clock sources and peripheral master clocks should be disabled.

4.5.2 Flash Memory

The Flash memory is automatically switched on when the core power supply is enabled at start up. If code is fetched from SRAM, the Flash memory power supply can be switched off by opening the Flash memory power switch (connected to VDDCORE), in order to save standby power consumption. Number of wait states should be adjusted according to MCK frequency and VDDCORE voltage (refer to the “Electrical Characteristics” section of the [AT91SAM7L series](#) datasheet)

4.5.3 Voltage Regulator

The voltage regulator output voltage should be adjusted to a minimum in accordance with application requirements and MCK frequency.

5. Conclusion

Thanks to the embedded low-power mode features, AT91SAM7L devices are particularly adapted for battery powered high performance applications. The Supply Controller and the Power Management Controller provide flexible clock frequencies and operating voltage adjustment to optimize power consumption.

The following table summarizes the characteristics of each mode:

Mode	Wake-up Sources	Power ^{(2) (3)} Consumption	Wake-up Time ⁽¹⁾	Core State	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up
Off Mode	FWUP pin	100 nA typ	< 5 ms	Off (Not powered)	Reset	PIOA & PIOB Inputs with pull-up PIOC high-Z inputs	PIOA & PIOB & PIOC Inputs with pull ups
Backup Mode (with backup SRAM and RTC)	FWUP pin WUP0-15 pins BOD alarm RTC alarm	3.5 μ A typ	< 0.5 ms	Off (Not powered)	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups
Wait Mode	Fast start-up through WUP0-15 pins	9 μ A typ	< 2 μ s	Powered (Not clocked)	Clocked back	Previous state saved	Unchanged
Idle Mode	IRQs FIQ	⁽⁴⁾	⁽⁴⁾	Powered (Not clocked)	Clocked back	Previous state saved	Unchanged

- Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the AT91SAM7128/L64 works with the 2 MHz RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken from wake up until the first instruction is fetched.
 2. The external LCD current consumption and the external loads on PIOs are not taken into account in the calculation.
 3. BOD current consumption is not included.
 4. Depends on MCK frequency.

Revision History

Doc. Rev	Comments	Change Request Ref.
6404A	First issue	



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

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