Schematic Review Checklist for Microsemi Timing IC Devices

Introduction

CLEAR FORM

This application note provides a schematic review checklist for designs using Microsemi timing IC devices. We encourage customers, to be proactive and start using it as a reference from early stages of schematic capture. It can also be used for the final schematic review before committing to PCB design.

Since different Microsemi timing IC devices have different requirements, the reviewer should always use as reference the latest documentation available on the Microsemi web page of the timing IC device. For a successful design, customer must use as reference the latest datasheet and all relevant application notes provided by Microsemi for a specific timing IC device. These application notes provide important design recommendations not covered in the datasheet, such as but not limited to: power supply decoupling, crystal circuit design, PCB placement and routing, list of available oscillator/crystal part numbers.

Prior to submitting a schematic to Microsemi for review, it is for our customers to perform their own review first using this checklist. It would be beneficial, if the resulting review checklist document is submitted together with the schematic and the below tables filled in.

Schematic Info

Company:	
Project:	
Schematic Name/Revision:	
Contact (Name, e-mail)	
Microsemi Timing IC Devices:	
Reviewer (Name, e-mail)	
Date of Review:	

Reference Material Used for Review

Datasheets and Application Notes Used as Reference for the Review (with revision number or release date**)**

Schematic Review Checklist

Y= Correct, NA= Not Applicable, Leave Blank= Not Sure/Haven't Checked

1. Schematic Symbol

1.1. Check if the pin names/numbers of the schematic symbol match the datasheet specifications. .....

1.2. Check if the thermal pad has a pin assigned in the schematic symbol. .....

2. General Control and Status Pin Connection

2.1. Check if the pins involved in power-up setup or auto-configuration are not floating and are driven to the proper logic level. .....

2.2. Check if all Open-drain outputs have external pull-up resistors. .....

2.3. Check for correct JTAG connection (see datasheet JTAG pins description). .....

2.4. Check voltage level compatibility driver-receiver for all control and status signals. .....

2.5. Check if the 'NC' and 'IC' pins connection follows datasheet recommendations. .....

3. Reset

3.1. Check if the reset pulse has the right duration and is issued after all voltages supplying the IC reached nominal level. .....

3.2. Check if the power-up reset configuration signals are stable and at the right level during and after reset. .....

3.3. Check if the reset implementation scheme doesn't rely on clocks generated by the timing IC device to generate the reset pulse for the timing IC device. .....

4. Host Interface connection

4.1. Check if the host interface implemented in the schematic: SPI or I2C matches the host interface enabled at power-up. .....

4.2. Check if I2C SCL/SDA signals are properly connected between master and slave devices. .....

4.3. Check for I2C address duplication if there are multiple devices with the same part number. .....

4.4. Check if pull-up resistors are present on the I2C SCL/SDA lines and have the right value. .....

4.5. Check if the SPI interface signals are properly connected between the master and slave device. Check the direction of data pins (output to input not output to output and input to input). .....

4.6. Check the SPI interface signals connection in the case of timing IC devices using external configuration EEPROM. In these cases, the timing IC device is master and slave in different stages after power-up. Check if the datasheet recommendations regarding the SPI_CS implementation is followed. The timing IC device drives the EEPROM SPI_CS pin when is in master mode.
The processor drives the timing IC device SPI_CS pin when in slave mode and the EEPROM SPI_CS pin should be pulled-up. .....

4.7. In the case of timing IC devices without an active auto-configuration, check if there is a host device in the system to support the configuration of the timing IC device. .....

4.8. If a debug header (used to provide access to the host interface) is present, check for correct pinout. Check also if the host interface section between the debug header and the timing IC device can be separated from the host controller to prevent conflicts between the host controller and the debug tool. .....

5. APLL Loop Filter

5.1. Check if the external PLL loop filter components have the value recommended in the datasheet. .....

6. Master Clock, Local Reference

6.1. Check if the frequency of the oscillator/crystal is correct. .....

6.2. Check if the master clock frequency selection at power-up matches the frequency of the master clock device in the schematic. .....

6.3. Check the power supply decoupling of the oscillator. .....

6.4. Check if the accuracy and the stability of the master clock reference is adequate for the application. .....

6.5. Check if the values of the resistors and capacitors which are part of the crystal oscillator circuit were selected based on the datasheet or application note recommendations. .....

6.6. Check if the unused master clock or local reference inputs are handled according to the datasheet or application note recommendations. .....

7. Reference Input Clocks

7.1. Check if the input termination is correct and follows Microsemi specifications. .....

7.2. Check if the driver logic type and electrical specification (DC and AC) meets the input specifications. .....

7.3. Check if the unused inputs are handled according to datasheet recommendations. .....

8. Output clocks

8.1. Check if the output termination is correct and follows Microsemi specifications. .....

8.2. Check if the output logic type and electrical specifications meets the receiver input specifications. .....

8.3. In the case of AC coupling, check if a DC path is implemented in schematic for the outputs requiring a DC path P-to-N. .....

8.4. Check for proper assignment of output clocks. Output clocks belonging to different clocking domains should not be assigned to the outputs of the same clock generator. (for example, SyncE and 1588 output clocks). .....

8.5. Check if the output driver supply pins are supplied from the right voltage. .....

9. Power Supply

9.1. Check if the power supply pins connection to supply voltages follows the datasheet recommendations. .....

9.2. Check if the decoupling scheme (value / number of decoupling capacitors and grouping in power decoupling islands) follows the recommendations in Microsemi datasheet or application notes. .....

9.3. Check if the power supply implementation meets the power-up/down sequencing requirement specified in the datasheet. .....

9.4. Check the power dissipation. .....

10. Schematic Correlation with the Configuration File

10.1. Check if special features which are added manually to the configuration file, are present in the configuration file. (Output Clock Valid status signal for example). .....

10.2. Check if the input / output type setup in the configuration file matches the schematic implementation. .....

10.3. Check if the input / output frequency setup in the configuration file matches the design requirements. .....

10.4. Check if the master clock frequency in the configuration file matches the master clock frequency in the schematic. .....

10.5. Check if the unused clock inputs and unused local reference inputs are disabled. .....

10.6. Check if all internal features not required in that application are disabled to minimize power consumption. .....

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