Migrating to the New PIC24F Pipeline and Sigma-Delta ADCs

INTRODUCTION

The Microchip PIC24FJ128GC010 family of 16-bit microcontrollers has two types of Analog-to-Digital Converters (ADCs): the 12-Bit, High-Speed Pipeline ADC (P_ADC) and the high-accuracy, 16-Bit Sigma-Delta ADC (SD_ADC).

For specific information on each of these peripherals, refer to the following sections in the *"dsPIC33/PIC24 Family Reference Manual"* (FRMs):

- **"12-Bit, High-Speed Pipeline A/D Converter"** (DS30686)
- **"16-Bit Sigma-Delta A/D Converter"** (DS30687)

This migration document describes how these two ADCs differ from the standard Successive Approximation Register ADC (SAR ADC) in terms of architecture and the impact of these variations on the application. For more information on implementation, refer to the specific device data sheet.

OVERVIEW

The P_ADC and SD_ADC Converters have the following two major differences over the standard SAR Converter:

- The timing generating method and its usage by the application
- The method of handling the final result by the application

The SAR Converters used by the PIC24 family (refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit A/D Converter with Threshold Detect"** (DS39739)) have the following characteristics:

- The timing is programmable and simple control and status bits are used to start or end the conversion
- The result of the conversion can be directly used by the application
- The errors given in the electrical specifications for each specific device is accounted for in the conversion result, such as gain, offset, INL, etc.
- The input signal's maximum frequency is set by the Nyquist criteria (sample rate/2)

The following sections describe how the two new ADCs differ from the SAR Converter in these and other specific areas.

The P_ADC, SD_ADC and SAR ADC have the same basic scheme: an input voltage, which is usually selected through a MUX, is sampled for a specified amount of time. This sample time is programmable and is usually a multiple of the ADC clock. The input voltage is stored by charging an internal, small valued capacitor (on the order of 6 pF), then disconnecting it from the input and presenting it to the additional circuitry that generates a digital representation of this voltage. The main difference in the three ADCs is how this conversion, from a voltage on a capacitor to a fixed binary result, is implemented. The implementation, in turn, affects the end result and how the result must be used by the application.

Features of the SAR A/D Converter

The SAR timing model is based on a two-part sequence to obtain the final result: a sampling or charging time, which is variable, and a fixed conversion period of 14 clock cycles (the period of this clock is called TAD and is programmable).

The sample time depends on the source impedance of the analog driving signal and has to be long enough to fully charge the internal sample capacitor. A typical sample time is 2 to 6 TAD clocks. For more information on the minimum time to charge the capacitor, refer to the "**Electrical Characteristics**" chapter in the specific device data sheet.

The handshake scheme is sometimes referred to as Start-of-Conversion/End-of-Conversion (SOC/EOC), because the user sets when conversion starts (external trigger, a timer interrupt, setting a bit in a register, etc). After the conversion is over, the SAR will store the data in RAM and flag the application (interrupt, setting a status bit, etc). The timing and the overall sample rate is easily controlled and the converter halts after each SOC/EOC cycle. Specific Microchip parts may add features, such as channel scanning. The SAR ADC is a one-shot type of a converter. One SOC/EOC sequence generates one data result. The sample rate is the sum of the capacitor charge time and the 14 TAD clocks of the conversion time. The sample rate of a typical SAR converter in the PIC24F series of parts ranges from 10K samples per second to 250K samples per second (the lower boundary is the discharge time of the sample cap into the load and its ESR).

The SAR accuracy model is simple. The result of the conversion contains the sum of all errors. For errors and limitations, refer to the specific device data sheets. The accuracy is not the same as the resolution. The resolution is a fixed number of bits (10, 12, etc), but the actual result of the conversion will vary based on these errors. The errors cause the expected digital output, known as the code word, to deviate from the ideal expected value. The code word will be within the range of errors. If the overall error for a SAR is ±4 LSB, and the expected code word was 400H, it will be in the range of 3FCH to 404H and is still accurate to the specification. In an actual application, some of these errors can be compensated for by calibration measurements or software correction tables.

The P_ADC and SD_ADC have error mechanisms that are not present in the SAR Converter and are discussed in the following sections.

Features of the Pipeline A/D Converter

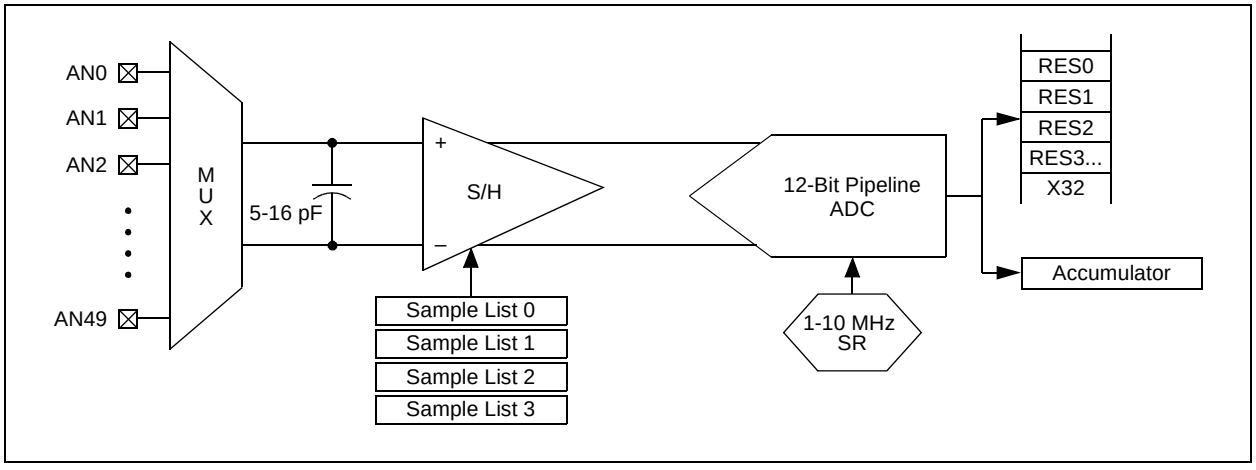
The P_ADC is a specific architecture that trades off speed for accuracy. The conversion speed of the P_ADC in the PIC24F ranges from 1M samples per second to 10M samples per second. The timing model and accuracy model for the P_ADC varies from the SAR Converter (see Figure 1).

The Pipeline ADC gets its name from the timing scheme used internally in the converter architecture and the fact that the code word is a result of a serial pipeline of smaller resolution converters. The output code word requires a fixed number of clock cycles (latency) before being valid. Once the pipeline is filled, the code words are updated every clock cycle. This differs from the SAR Converter, where every new code word requires a sample time plus a conversion time, usually 16-18 TAD clocks. For the P_ADC, a 10 MHz sample clock generates 10M samples per second after the latency period of 8.5 clocks is met. There is a 1:1 correspondence between the output data rate and the sample rate. This makes the P_ADC unique among the SD_ADC and SAR ADC. However, the fixed latency skews the input-to-output time relationship, where the current code word generated is the representation of the analog signal applied to the P_ADC Converter's sample capacitor, 8.5 clocks prior.

The extremely fast conversion rate of the P_ADC brings up the following concern: if the MPU is running at the full speed of 16 MIPS, how can samples generated at 10M/sec be handled? There are dedicated RAM buffers to capture snapshots of 32 samples and a DMA (Direct Memory Access) must be used. The snapshot concept is important for the P_ADC, as a common technique is to capture 32 samples, have DMA input them into RAM and process them while the P_ADC refills the buffer with the next snapshot. At a 1 MHz sample rate, the processor has approximately 470 MPU cycles to process the data before the buffer is filled. Most P_ADC applications take a fixed number of samples in a single burst (the snapshot), do the processing and then repeat the sequence. A typical use for the P_ADC is a line array camera scanning items on a fast moving conveyor belt. The P_ADC will convert the analog camera video data quickly and process it before the next item moves in front of the camera. The P_ADC has integrated hardware to make filling the buffer transparent to the user code.

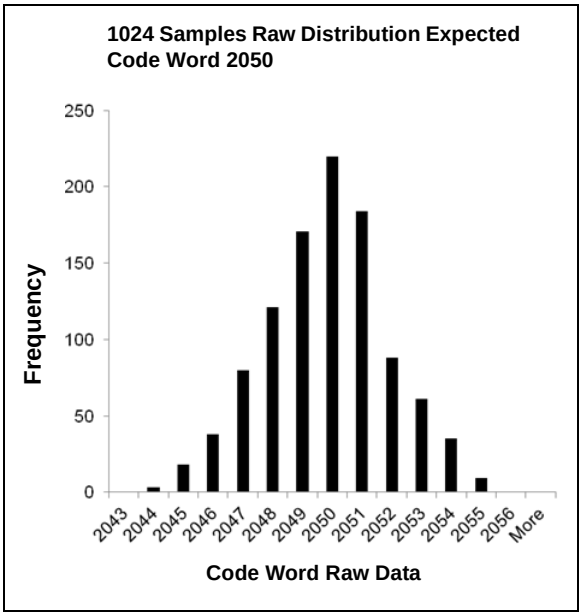
The pipeline latency is more critical when multiple channels are used. The P_ADC can support over 50 analog input channels. While switching from one channel to another, the application has to wait until the pipeline is flushed a minimum of 9 sample clocks. This is carried out using the sample list feature. The hardware scans the channels in the sample list and places the results in the buffer, which is transparent to the user. The pipeline latency is automatically taken into account and the results are aligned with the input channel multiplexer. The user code does not have to be programmed to flush the pipeline; the hardware will perform the operation. The SD_ADC also has channel switching latency issues and these are discussed in the following section.

FIGURE 1: PIPELINE A/D CONVERTER



The accuracy model of the P_ADC is different compared to other converter architectures. The initial error is identical to the SAR_ADC as all the error sources are present in the code word. However, an additional noise error is added and this noise error has to be averaged over multiple samples in order to get the full resolution from the converter. The effect of the noise error is a Gaussian histogram of the expected code word, as shown in Figure 2.

FIGURE 2: PIPELINE_RAW

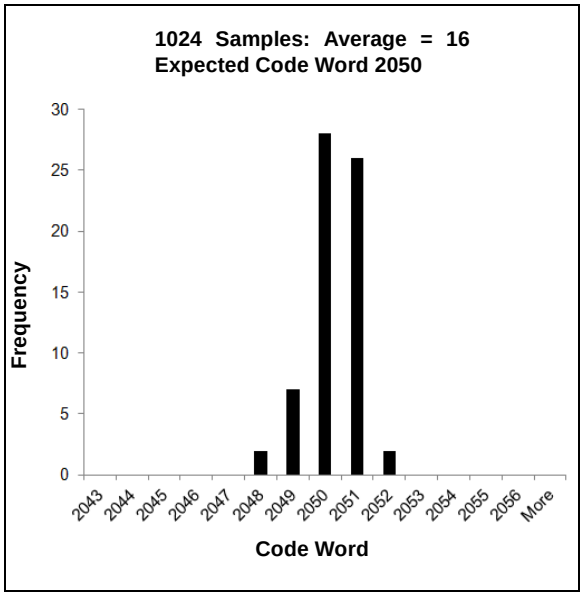


The spread of possible code words generated by a constant input voltage is wider than expected. The higher noise floor of the P_ADC causes the resolution to be less than 12 bits.

The converter cannot achieve the 12-bit accuracy without averaging at least 16 consecutive samples. In some designs, due to other noise contributors, such as a printed circuit board layout and power supply noise, the averaging may require 32 or 64 samples. It is recommended to average by powers of two, so that the division is a simple shift operation.

Figure 3 shows the improvement when averaging 16 samples of data with a stable input voltage.

FIGURE 3: PIPELINE_AVERAGE



The averaging will not reduce the non-noise errors in the P_ADC, such as Integral Nonlinearity (INL) and Differential Nonlinearity (DNL). The averaging will cause the data rate of the result to be less than the sample rate. The sample rate must be within 1 MHz and 10 MHz, which in turn, will determine the Nyquist frequency for AC signals. It is the throughput which will be lower by the number of averages taken.

The following are important considerations when using the 12-Bit Pipeline ADC:

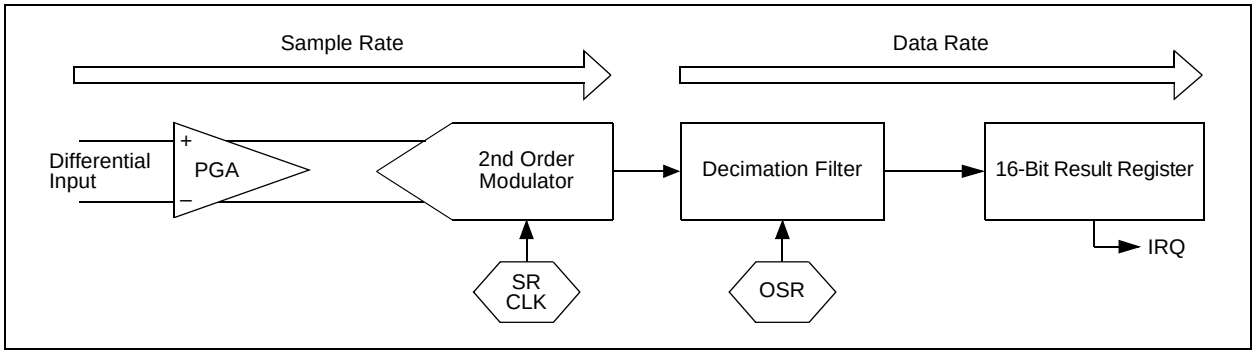
- The sample rate is restricted to be within 1 MS/sec and 10 MS/sec
- Once the 8.5 clock latency is met, each sample clock produces a new result
- Averaging is required for the highest accuracy applications
- Use the sample list feature when scanning multiple inputs

For code examples using the Pipeline ADC, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit, High-Speed Pipeline A/D Converter"** (DS30686).

Features of the Sigma-Delta A/D Converter

The 16-Bit Sigma-Delta Converter uses a combination of a high sample rate and a low data rate to achieve high accuracy. The low data rate is a result of a digital filtering algorithm that converts a serial data stream into a parallel code word and is referred to as a 'Decimation Filter' or an 'Oversampled Converter'. This filtering is inherently low-pass in nature and restricts the bandwidth of the input signal. Figure 4 shows the simplified block diagram of the SD_ADC.

FIGURE 4: SD_ADC ARCHITECTURE



The SD_ADC Converter allows three possible sample rates for the Sigma-Delta modulator: 1 MHz, 2 MHz or 4 MHz. The modulator produces a serial bit stream whose pulse density is proportional to the input voltage. This serial data is used as the input to a 64-bit, fixed-point math processor that executes the digital filtering algorithm to produce the 16-bit code word. This filter can be set to one of seven possible Oversampling Ratios (16, 32, 64 …1024), which produces the data rate. The relationship between the sample clock and the data rate is given by Equation 1.

EQUATION 1:

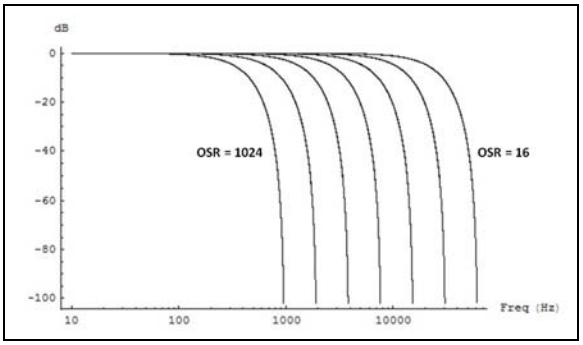
$$DataRate = \frac{(SampleClock)}{(4)(OSR)}$$

This bounds the lowest data rate at 244.1 Hz (1 MHz sample clock and an OSR of 1024). The higher the sample rate clock, the more accurate the results will be. The noise is higher in the spectra of the pulsed data stream, and hence, filtered out by the decimation filter, which is referred to as 'Noise Shaping' in the literature.

In terms of sample rate, it is the data rate, programmed by the application, which determines the overall behavior of the SD_ADC. The SD_ADC is unlike the SAR or the P_ADC in terms of architecture. The sample rate is usually fixed at the highest rate of 4 MHz and the data rate is set depending on the required bandwidth of the input signal. The selected Oversampling Ratio (OSR) determines the bandwidth of the filter and restricts the type of signal to be measured.

Figure 5 shows the effect of the Oversampling Ratio on the bandwidth.

FIGURE 5: DECIMATION FILTER BANDWIDTH vs. OSR



The decimation filter has a response similar to an analog low-pass filter. As the OSR increases, the bandwidth of the decimation filter decreases. The actual transfer function is a $sinc^3$ shape (similar to an elliptical filter) and the pass band has a gradual roll-off up to the 3 dB point, where it rapidly drops off. As a rule of thumb, the flat portion of the decimation filter's response is one eighth of the bandwidth, where flat is <0.1 dB of attenuation. A 1-pole Butterworth filter has about one fourth of the pass-band flat to 0.1 dB in comparison. The -3 dB point of the decimation filter is approximately one third of the data rate. This corresponds to a 325 Hz bandwidth for the highest OSR of 1024. For DC measurements, it is a fairly wide bandwidth, as it includes AC power line harmonics which would pass through the ADC unfiltered. In the SD_ADC, taking multiple readings and averaging the results will improve the overall accuracy. External low-pass filters and software notch/comb filters are other methods to reduce AC interference.

The low-pass filtering nature of the decimation filter plays an important role in using the SD_ADC. The ideal input signal should be DC or have low harmonic content, like a sine wave. High harmonic content signals, such as narrow pulses, are not accurately converted by the SD_ADC. Sigma-Delta Converters can be designed for higher frequency and higher harmonic content signals like audio, but in this implementation, the converter is limited to low harmonic content signals. The decimation filter also exhibits a variable transient response delay based on the OSR. The larger the OSR, the slower the filter's transient response (see Figure 6 and Figure 7).

If a high harmonic signal is converted by the SD_ADC, the higher OSR settings will have large errors and be delayed longer in time. The decimation filter's transient response is slower as the OSR is larger. Even at the fastest data rate/smallest OSR, there is some attenuation and distortion as the higher harmonics are filtered out by the decimation algorithm. Hence, the SD_ADC is best applied for DC/bridging measurements, such as weight, pressure and temperature, or for AC power measurements (50/60 Hz sine waves). The low-pass filtering helps in removing noise injected by Electromagnetic Interference (EMI)/Radio Frequency Interference (RFI), printed circuit board layout and power supplies. Figure 6 shows a narrow pulse signal and the effects of a high OSR (128) and a low OSR (16). The stair-stepping of the output is due to the DAC update being the same as the data rate.

FIGURE 6: SD_ADC INPUT/OUTPUT DELAY WITH OSR = 128

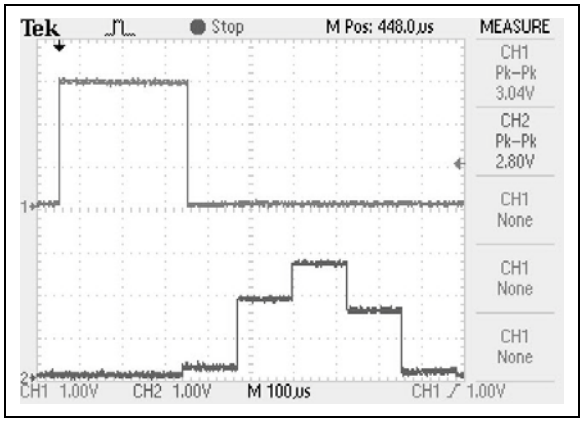
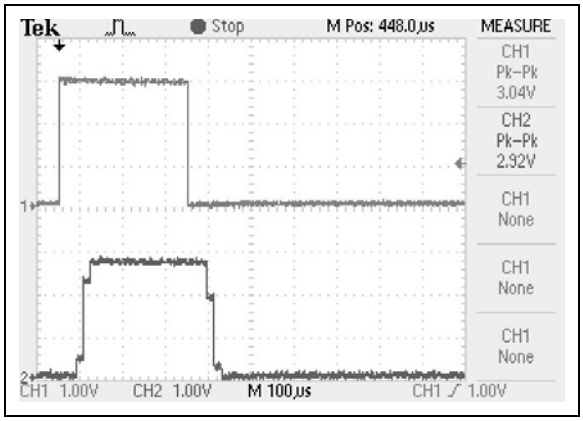


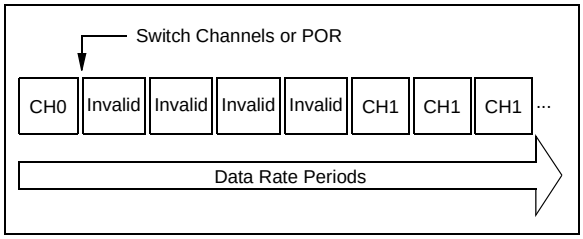
FIGURE 7: SD_ADC INPUT/OUTPUT DELAY WITH OSR = 16



The accuracy model of the SD_ADC has higher gain and offset errors than the SAR or P_ADC. There are special measurement modules built into the hardware that allows the firmware to correct these errors and increase the overall accuracy. For more information, refer to the code examples included in the **"16-Bit Sigma-Delta A/D Converter"** (DS30687A) section in the *"dsPIC33/PIC24 Family Reference Manual"*.

The timing model of the SD_ADC is different from other converters. It is not a SOC/EOC type of handshake. Once enabled, the SD_ADC free runs at the programmed data rate without any MPU resources. At the end of every conversion, an interrupt is generated and the conversion cycle continues, even if the interrupt is not serviced. The prior code word is over-written by the next conversion cycle. The SD_ADC continues to run and convert at the data rate until disabled. In addition, there is a 4-data cycle pipeline delay caused by the decimation filter's internal timing requirements. Similar to P_ADC, the SD_ADC pipeline has to be flushed when switching input channels or when first enabled (see Figure 8).

FIGURE 8: SD_ADC PIPELINE DELAY



This 4-data cycle pipeline delay has an interesting side effect. When first enabled, or after a channel switch, the data for these four code words is neither the prior input result nor the new input result. Rather, the four code words generated by the decimation filter is a mixture of both readings. Hence, these four code words must be discarded by the application firmware.

The free-running conversion of the SD_ADC can make syncing the result to a specific point in time difficult. Therefore, the SD_ADC is ideally suited for non-time-critical measurements, like temperature, where the reading can be 10s of milliseconds delayed from the actual input event without adverse effects. Contrast this to a SAR Converter, where the delay from the input voltage to the code word is one conversion cycle. In the SD_ADC Converter, every sample placed in the result register is seen at the input pins, four data clock periods prior.

Dithering is another important feature of the SD_ADC that is not found on the other converters. Dithering is the purposeful adding of Gaussian white noise to the input voltage. Adding dithering causes the removal of Idle tones and reduces jitter in the code word when the input voltage is at the bit transition threshold.

An Idle tone is a signal that is generated by the decimation filter when an input voltage to the SD_ADC causes the pulse density spectra out of the modulator to repeat in certain patterns. This is sometimes called a limit cycle, although Idle tones are part of the noise spectra and tones generated by a limit cycle are not. The result is the same; the decimation filter will generate a sine tone in addition to the correct code words. Different input voltages may generate several different frequencies of Idle tones. Dithering will modulate the input voltage in a way that there is no fixed repeating pulse density spectra fed to the decimation filter; this will remove the Idle tones.

Dithering is useful for all ADC architectures which have bit transitions near the noise floor, usually at 16 bits and above. Consider a 16-bit converter with an input range of 2.5V; this means every bit is a change of only approximately 38 μV. If an input voltage is close to the transition point for the next code word (±5 μV), and noise would cause the code word to jitter back and forth sporadically between the two possible values, and if the right amount of white noise is applied, then the code word will alternate between the two possible values. The code word would alternate in a way so that after being filtered by the decimation filter, the code word has a dominate value and is stable. Dithering has the effect of spreading the spectral spurious content of the input signal over the output spectrum. This will lower the signal-to-noise ratio and increase Spurious-Free Dynamic Range (SFDR), which is the difference between the input signal level and the highest harmonic level. Dithering will raise the overall noise floor while reducing the spurious peaks a large amount (on the order of 8-10 dB).

The following are important considerations when using the 16-Bit Sigma-Delta ADC:

- The data rate, not the sample rate, defines the bandwidth of the converter
- There is a fixed, 4-data cycle pipeline delay during POR or switching input channels
- Dithering is required in most cases for best accuracy
- The converter runs continuously once started and older data is automatically overwritten

SUMMARY

The P_ADC and SD_ADC Converters are more application-specific than the standard SAR Converter. If the analog inputs are DC or low-frequency content AC, the SD_ADC is best suited to make the measurement. Higher frequency AC signals require the use of the P_ADC. For code examples using the new ADCs, refer to the specific FRMs at:

http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=2575

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