
Atmel AVR539: Migrating from AT90PWM216/316 to AT90PWM81/161



8-bit Atmel Microcontrollers

Application Note

Features

This application note is a guide to help current Atmel® AT90PWM216/316 users convert existing designs to Atmel AT90PWM81/161.

Additionally, the electrical characteristics of the AT90PWM81/161 are different from those of AT90PWM216/316.

Check the datasheets of both products for detailed information.

The main features of the AT90PWM216/316 have been carried over to the AT90PWM81/161.

The most important evolutions in the AT90PWM81/161 are the clock peripheral and the analog comparator implementations.

Some features such as a temperature sensor, have been added.

The AT90PWM81/161 has also some improvements on:

- Analog to digital converter
- Analog amplifier
- V_{REF}
- EEPROM access
- PSC
- Reset pin
- Some features have been reduced in AT90PWM81/161:
 - PSC numbers
 - Timer numbers

Rev. 8428B-AVR-01/12



1 Introduction

Table 1-1 is a summary of the comparison between Atmel AT90PWM216/316 and Atmel AT90PWM81/161 features.

Table 1-1. AT90PWM81/161 versus AT90PWM216/316 (the differences between the products are grayed).

	AT90PWM216	AT90PWM316	AT90PWM81	AT90PWM161
Core	AVR [®]	AVR	AVR	AVR
Pins	24	32	20/32	20/32
Flash	16KB	16KB	8KB	16KB
SRAM	1KB	1KB	256B	1024B
EEPROM	512B	512B	512B	512B
I/O's	19	27	16/20	16/20
A/D 10 bits	8 inputs	11 inputs	8/11 inputs	8/11 inputs
Amplifier for ADC	1	2	1	1
Temperature sensor			1	1
Analog comparator	2	3	3	3
D/A 10 bits	1	1	1	1
Time 8b	1	1		
Timer 12b: PSC	2	3	1	1
Timer 12b: PSCR			1	1
Timer 16b	1	1	1	1
PSC 12 bits	2	3	2 (1 PSCR)	2 (1 PSCR)
SPI	Yes	Yes	Yes	Yes
DALI/UART	Yes	Yes	No	No

The features differences are detailed in following sections:

- Reset
- Interrupt vectors
- Clock
- PLL
- Bandgap
- V_{REF}
- Temperature sensor
- PortC
- EEPROM
- INT3
- Timers (Timer 0 / Timer 1)
- SPI
- UART
- PSC0

- PSC1
- PSC2
- ADC
- Analog comparators
- DAC
- I/O registers

2 Reset

Atmel AT90PWM81/161 provide an additional configuration of the RESET pin, which is not present on Atmel AT90PWM216/316.

The reset pin can be leaved for functional use. This can be achieved thanks to the RSTDIS bit (Reset Pin Disable) in the MCUCR register (see [Table 2-1](#)).

The reset function can be disabled, leaving the pin PEO free:

- When the RSTDIS bit is written to zero, the reset signal is active (default configuration)
- When the RSTDIS bit is written to one, the reset signal is inactive and pin PEO can be used for alternate function purpose (OCD, INT2, or I/O)

Table 2-1. MCUCR - MCU Control Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	PUD	RSTDIS	CKRC81	IVSEL	IVCE	MCUCR
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

A fuse bit RSTDISBL (Bit 7 of Fuse High Byte) can be used to force the reset disable at startup:

- If the RSTDISBL fuse is programmed, PE0 is used as an I/O pin. Note that the electrical characteristics of PE0 differ from those of the other pins. If the RSTDISBL fuse is un-programmed (default fuse configuration), PE0 is used as a reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running

The default configuration provides software compatibility.

3 Interrupt vectors

The Interrupt vector addresses are same between Atmel AT90PWM216/316 and Atmel AT90PWM161 but are different in Atmel AT90PWM81. Interrupt addresses of AT90PWM81 have an increment equal to one word, whereas interrupt addresses of AT90PWM161/216/316 have an increment equal to two words (see [Table 3-1](#)).

Table 3-1. Reset and Interrupt Vectors.

Vector no.	AT90PWM81 address	AT90PWM161/216/316 program address	Source	Interrupt definition
1	0x0000	0x0000	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and Emulation AVR Reset
2	0x0001	0x0002	PSC2 CAPT	PSC2 Capture Event
3	0x0002	0x0004	PSC2 EC	PSC2 End Cycle
4	0x0003	0x0006	PSC2 EEC	PSC2 End of Enhanced Cycle
5	0x0004	0x0008	PSCr CAPT	PSC reduced Capture Event
6	0x0005	0x000A	PSCr EC	PSC reduced End Cycle
7	0x0006	0x000C	PSCr EEC	PSC reduced End of Enhanced Cycle
8	0x0007	0x000E	ANACOMP 0	Analog Comparator 0
9	0x0008	0x0010	ANACOMP 1	Analog Comparator 1
10	0x0009	0x0012	ANACOMP 2	Analog Comparator 2
11	0x000A	0x0014	INT0	External Interrupt Request 0
12	0x000B	0x0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	0x000C	0x0018	TIMER1 OVF	Timer/Counter1 Overflow
14	0x000D	0x001A	ADC	ADC Conversion Complete
15	0x000E	0x001C	INT1	External Interrupt Request 1
16	0x000F	0x001E	SPI, STC	SPI Serial Transfer Complete
17	0x0010	0x0020	INT2	External Interrupt Request 2
18	0x0011	0x0022	WDT	Watchdog Time-Out Interrupt
19	0x0012	0x0024	EE READY	EEPROM Ready
20	0x0013	0x0026	SPM READY	Store Program Memory Ready

4 Clock

4.1 Clock sources

The clock source of Atmel AT90PWM81/161 can be switched dynamically. It allows dynamic switch between RC, WD RC, PLL output and crystal oscillator. The new registers which must be configured to control this dynamic switch are CLKSELR and CLKCSR described in [Table 4-1](#) and [Table 4-2](#). The clock switching requires using the sequences provided in “Dynamic Clock Switch” section of the AT90PWM81/161 datasheet.

4.1.1 CLKSELR – Clock Selection Register

Table 4-1. CLKSELR - Clock Selection Register.

Bit	7	6	5	4	3	2	1	0	
	-	COUT	CSUT1	CSUT0	CSEL3	CSEL2	CSEL1	CSEL0	CLKSELR
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	CKOUT fuse	SUT1..0 fuses			CKSEL3..0 fuses			

- **Bit 6 – COUT: Clock Out**

The COUT bit is initialized with CKOUT fuse bit.

The COUT bit is only used in case of ‘CKOUT’ command. Refer to “Clock Output Buffer” section of the AT90PWM81/161 datasheet when using it.

In case of ‘Recover System Clock Source’ command, COUT it is not affected (no recovering of this setting).

- **Bits 5:4 – CSUT1:0: Clock Start-up Time**

CSUT bits are initialized with the values of SUT fuse bits.

In case of ‘Enable/Disable Clock Source’ command, CSUT field provides the code of the clock start-up time. Refer to subdivisions of “Clock sources” section of the AT90PWM81/161 datasheet for code of clock start-up times.

In case of ‘Recover System Clock Source’ command, CSUT field is not affected (no recovering of SUT code).

- **Bits 3:0 – CSEL3:0: Clock Source Select**

CSEL bits are initialized with the values of CKSEL fuse bits.

In case of ‘Enable/Disable Clock Source’, ‘Request for Clock Availability’ or ‘Clock Source Switch’ command, CSEL field gets back the code of the clock source. Refer to “Clock sources” section of the AT90PWM81/161 datasheet for clock source codes.

In case of ‘Recover System Clock Source’ command, CSEL field receives the code of the clock source used to drive the clock control unit.

4.1.2 CLKCSR – Clock Control and Status Register

Table 4-2. CLKCSR – Clock Control and Status Register.

Bit	7	6	5	4	3	2	1	0	
	CLKCCE	-	-	CLKRDY	CLKC3	CLKC2	CLKC1	CLKC0	CLKCSR
Read/write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 – CLKCCE: Clock Control Change Enable**

The CLKCCE bit must be written to logic one to enable change of the CLKCSR bits. The CLKCCE bit is only updated when the other bits in CLKCSR are simultaneously written to zero. CLKCCE is cleared by hardware four cycles after it is written or when the CLKCSR bits are written. Rewriting the CLKCCE bit within this timeout period does neither extend the timeout period, nor clear the CLKCCE bit.

- **Bit 4 – CLKRDY: Clock Ready Flag**

This flag is the output of the 'Clock Availability' logic.

This flag is reset once the 'Request for Clock Availability' command is entered.

It is set when 'Clock Availability' logic confirms that the (selected) clock is running and is stable. The delay from the request and the flag setting is not fixed; it depends on the clock start-up time, the clock frequency and, of course, if the clock is alive. The user's has itself to do the difference between 'no_clock_signal' and 'clock_signal_not_yet_available'.

- **Bits 3:0 – CLKC3:0: Clock Control Bits 3 - 0**

These bits define the command to provide to the 'Clock Switch' module. The special write procedure must be followed to change the CLKC bits.

1. Write the Clock Control Change Enable (CLKCCE) bit to one and all other bits in CLKCSR to zero.
2. Within four cycles, write the desired value to CLKCSR register while clearing CLKCCE bit.

Interrupts should be disabled when setting CLKCSR register in order not to disturb the procedure.

Table 4-3. Clock command list.

Clock command	CLKC3..0
No command	0000 _b
Disable clock source	0001 _b
Enable clock source	0010 _b
Request for clock availability	0011 _b
Clock source switch	0100 _b
Recover system clock source code	0101 _b
CKOUT command	0111 _b
No command	1xxx _b

4.2 RC oscillator

In Atmel AT90PWM81/161, typical frequency value of the RC oscillator can be changed. Two frequencies can be selected; 8 or 1MHz.

This function is achieved with CKRC81 bit of MCUCR Register (see [Table 4-4](#)).

Table 4-4. MCUCR – MCU Control Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	PUD	RSTDIS	CKRC81	IVSEL	IVCE	MCUCR
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0/1	0	0	0	

- **CKRC81- Frequency selection of the calibrated 8/1 MHz RC oscillator**

- When the CKRC81 bit is written to zero, the RC oscillator frequency is 8MHz
- When the CKRC81 bit is written to one, the RC oscillator frequency is 1MHz

The default configuration is 8MHz, which provides software compatibility.

NOTE

Can only be changed when the RC oscillator is enabled.

NOTE

When the RC oscillator is used as the PLL source, CKRC81 must not be written to 1.

NOTE

If the RC oscillator is disabled, this bit is cleared by hardware.

5 PLL

The PLL frequency of Atmel AT90PWM81/161 can be configured to 64/56/48/40 or 32MHz while the PLL frequency of Atmel AT90PWM216/316 can only be configured at 64 or 32MHz.

The PLLF bits are used to select the multiplication factor of the PLL.

If PLL is used, PLLSCR configuration must be changed in software when migrating from AT90PWM216/316 to AT90PWM81/161. Configurations versus products are detailed in [Table 5-1](#) and [Table 5-2](#).

5.1 AT90PWM216/316

In AT90PWM216/316, bit 2 (PLLF) defines the PLL factor.

Table 5-1. PLLCSR – PLL Control and Status Register.

Bit	7	6	5	4	3	2	1	0	
\$29 (\$29)	-	-	-	-	-	PLLF	PLLE	PLOCK	PLLCR
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R	
Initial value	0	0	0	1	0	0	0/1	0	

If PLLF is set, the PLL output is 64Mhz.

If PLLF is clear, the PLL output is 32Mhz.

5.2 AT90PWM81/161

In AT90PWM81/161, bits 5:2 (PLLF3/2/1/0) define the PLL factor.

Table 5-2. PLLCSR – PLL Control and Status Register.

Bit	7	6	5	4	3	2	1	0	
\$29 (\$29)	-	-	PLLF3	PLLF2	PLLF1	PLLF0	PLLE	PLOCK	PLLCR
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R	
Initial value	0	0	0	1	0	0	0/1	0	

• Bits 5:2 – PLLF: PLL Factor

The PLLF bits are used to select the multiplication factor of the PLL.

Table 5-3. PLL factors table.

PLLF3..0	N+2	PLL frequency MHz
7-F		Reserved
6	8	64
5	7	56
4	6	48
3	5	40
2	4	32
0-1		Reserved

6 Bandgap

In Atmel AT90PWM81/161 the bandgap current can be calibrated thanks to the new BGCCR and BGCRR registers described [Table 6-1](#) and [Table 6-2](#). See also section “Voltage Reference and Temperature Sensor” of the AT90PWM81/161 datasheet.

6.1 BGCCR – Bandgap Calibration Current Register

Table 6-1. BGCCR – Bandgap Calibration Current Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	BGCC3	BGCC2	BGCC1	BGCC0	BGCCR
Read/write	-	-	-	-	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	1	0	0	0	

- **Bit 3:0 – BGCC3:0: BG Calibration of PTAT Current**

These bits are used for trimming the nominal value of the bandgap reference voltage (V_{bg}). These bits are binary coded, so the lowest value for V_{bg} is reached when BGCC3:0 is 0000 and the maximum value when BGCC3:0 is 1111. The step size is approximately 5mV. Updating the BGCC bits will affect the BOD detection level. The BOD will react quickly to the new detection level.

6.2 BGCRR – Bandgap Calibration Resistor Register

Table 6-2. BGCRR – Bandgap Calibration Resistor Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	BGCR3	BGCR2	BGCR1	BGCR0	BGCRR
Read/write	-	-	-	-	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	1	0	0	0	

- **Bit 3:0 – BGCR3:0: BG Calibration of Resistor ladder**

These bits are used for temperature gradient adjustment of the bandgap reference.

7 VREF

In Atmel AT90PWM216/316, when using internal voltage reference V_{REF} , a decoupling capacitor must be connected to pin AREF.

Atmel AT90PWM81/161 can be configured to get PE3 pin free as port. In this configuration the pin does not require an external capacitor.

These configurations are achieved with REFS1/REFS0 bits of ADMUX register.

NOTE

Configurations are not software compatible.

Table 7-1. ADMUX – ADC Multiplexer Register.

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	-	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/write	R/W	R/W	R/W	-R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7, 6 – REFS1, 0: ADC V_{REF} Selection Bits**

These two bits determine the voltage reference for the ADC and for the other analog features.

The REFS1/REFS0 tables according to the AT90PWM216/316 and AT90PWM81/161 are detailed in sections 7.1 and 7.2.

7.1 AT90PWM216/316

The different settings are shown in Table 7-2.

Table 7-2. ADC Voltage Reference Selection.

REFS1	REFS0	Description	
		Voltage reference	PE3/AREF pin
0	0	External V_{REF} (internal V_{REF} is switched off)	External voltage reference
0	1	AV_{CC}	
1	0	Reserved	
1	1	Internal 2.56V reference voltage	External capacitor for decoupling of the internal reference voltage

If these bits are changed during a conversion, the change will not take effect until this conversion is complete (it means while the ADIF bit in ADCSRA register is set).

7.2 AT90PWM81/161

The different settings are shown in [Table 7-3](#) in which the added configuration is grayed.

Table 7-3. ADC Voltage Reference Selection.

REFS1	REFS0	Description	
		Voltage reference	PE3/AREF pin
0	0	External V_{REF}	External voltage reference
0	1	AV_{CC}	
1	0	Internal 2.56V reference voltage	External capacitor for decoupling of the internal reference voltage
1	1	Internal 2.56V reference voltage	PE3 pin free as port without the requirement of an external capacitor

8 Temperature sensor

The temperature sensor is a new feature which was not present in Atmel AT90PWM216/316. Please refer to the description in the AT90PWM216/316 datasheet.

Atmel AT90PWM81/161 have only one amplifier (AMP0) and the configuration, which selected AMP1 in AT90PWM216/316, is used in AT90PWM81/161 to select the temperature sensor as ADC input.

Table 8-1. ADMUX – ADC Multiplexer Register.

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	-	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/write	R/W	R/W	R/W	-R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

8.1 AT90PWM216/316

- Bit 3, 2, 1, 0 – MUX3, MUX2, MUX1, MUX0: ADC Channel Selection Bits

Table 8-2. AT90PWM216/316 ADC Channel selection bits.

MUX3	MUX2	MUX1	MUX0	Description
0	0	0	0	ADC0
0	0	0	1	ADC1
0	0	1	0	ADC2
0	0	1	1	ADC3
0	1	0	0	ADC4
0	1	0	1	ADC5
0	1	1	0	ADC6
0	1	1	1	ADC7
1	0	0	0	ADC8
1	0	0	1	ADC9
1	0	1	0	ADC10
1	0	1	1	AMP0
1	1	0	0	AMP1 (- is ADC8, + is ADC9)
1	1	0	1	Reserved
1	1	1	0	Bandgap (Vbg)
1	1	1	1	GND

In AT90PWM216/316: 1100 selects AMP1.

8.2 AT90PWM81/161

Table 8-3. AT90PWM81/161 ADC Channel selection bits.

MUX3	MUX2	MUX1	MUX0	Description
0	0	0	0	ADC0
0	0	0	1	ADC1
0	0	1	0	ADC2
0	0	1	1	ADC3
0	1	0	0	ADC4
0	1	0	1	ADC5
0	1	1	0	ADC6
0	1	1	1	ADC7
1	0	0	0	ADC8
1	0	0	1	ADC9
1	0	1	0	ADC10
1	0	1	1	AMP0
1	1	0	0	Temperature sensor (V_{TEMP})
1	1	0	1	VCC/4
1	1	1	0	Bandgap (V_{bg})
1	1	1	1	GND

In Atmel AT90PWM81/161: 1100 selects the temperature sensor (V_{TEMP}).

9 PortC

Atmel AT90PWM81/161 do not provide Port C and therefore PORTC, DDRC and PINC registers are no more present in AT90PWM81/161.

10 EEPROM

- First, the EEPROM memory of Atmel AT90PWM81/161 can be accessed per page and per byte while Atmel AT90PWM216/316 can only be accessed per byte. This function allows for instance a faster context saving during power fail sequence.
This control is achieved with new Bit 6 (EEPAGE) of EECR register (see [Table 10-1](#))
- Secondly a status bit has been added in AT90PWM81/161 to indicate that non-volatile memory (FLASH, EEPROM, Lock-bits) is busy.
This control is achieved with new Bit 7 (NVMBYS) of EECR register (see [Table 10-1](#))

Table 10-1. EECR – EEPROM Control Register.

Bit	7	6	5	4	3	2	1	0	
	NVMBYS	EEPAGE	EEPM1	EEPM0	EERIE	EEMWE	EEWE	EERE	EECR
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	0	0	X	0	

- Bit 7 – NVMBYS: Non-volatile memory busy**

The NVMBYS bit is a status bit that indicates the NVM memory (FLASH, EEPROM, Lock-bits) is busy programming. Once a program operation is started, the bit is set and it remains set until the program operation is completed.

- Bit 6 – EEPAGE: EEPROM page access (multiple bytes access mode)**

Writing EEPAGE to one enables the multiple bytes access mode. That means that several bytes can be programmed simultaneously into the EEPROM. When the EEPAGE bit has been written to one, the EEPAGE bit remains set until an EEPROM program operation is completed. Alternatively the bit is cleared when the temporary EEPROM buffer is flushed in software (see EEPMn bits description). Any write to EEPAGE, while EEPE is one, is ignored. See EEPROM section of the AT90PWM81/161 datasheet for details on how to load data into the temporary EEPROM page and the usage of the EEPAGE bit.

11 INT3

Atmel AT90PWM81/161 have no INT3 input and the External Interrupt 3 is not present.

So software compatibility must be checked when migrating from Atmel AT90PWM216/316.

The following bits are not declared in AT90PWM81/161:

- Bit 3 – INT3: External Interrupt Request 3 Enable of EIMSK register
- Bit 3 – INTF3: External Interrupt Flag 3 of EIFR register
- Bits 7/6 – ISC31/30: External Interrupt 3 Sense Control Bits of EICRA register

12 Timers

Atmel AT90PWM81/161 have only one timer (Timer1) and has only one input capture (ICP1). So the GTCCR – General Timer/Counter Control Register (see [Table 12-1](#)), which was used in Atmel AT90PWM216/316, is no longer present in AT90PWM81/161.

Table 12-1. GTCCR – General Timer/Counter Control Register.

Bit	7	6	5	4	3	2	1	0	
	TSM	ICPSEL1	-	-	-	-	-	PSRSYNC	GTCCR
Read/write	R/W	R/W	R	R	R	R	R	R/W	
Initial value	0	0	0	0	0	0	0	0	

Functions in AT90PWM216/316:

- **Bit 7 – TSM: Timer/Counter Synchronization Mode:**

Writing the TSM bit to one activates the Timer/Counter Synchronization mode. In this mode, the value that is written to the PSRSYNC bit is kept, hence keeping the corresponding prescaler reset signals asserted. This ensures that the corresponding timer/counters are halted and can be configured to the same value without the risk of one of them running during configuration. When the TSM bit is written to zero, the PSRSYNC bit is cleared by hardware, and the timer/counters start counting simultaneously.

- **Bit6 – ICPSEL1: Timer 1 Input Capture selection**

Timer 1 capture function has two possible inputs ICP1A (PD4) and ICP1B (PB6). The selection is made thanks to ICPSEL1 bit as described in the following table:

Table 12-2. ICPSEL1.

ICPSEL1	Description
0	Select ICP1A as trigger for timer 1 input capture
1	Select ICP1B as trigger for timer 1 input capture

- **Bit 0 – PSRSYNC: Prescaler Reset**

When this bit is one, Timer/Counter1 and Timer/Counter0 prescaler will be reset. This bit is normally cleared immediately by hardware, except if the TSM bit is set.

NOTE

Timer/Counter1 and Timer/Counter0 share the same prescaler and a reset of this prescaler will affect both timers.

12.1 Timer0

The Timer0 is not included in AT90PWM81/161 features. So the following registers are not declared:

- TIFR0
- TCNT0
- TCCR0B
- TCCR0A
- OCR0B
- OCR0A
- TIMSK0

- Bit 6 – PRTIM0: Power Reduction Timer/Counter0 of PRR register

12.2 Timer1

The Timer1 of Atmel AT90PWM81/161 is a simplified 16-bits timer with auto reloads of TOP value.

Output compare functions of Timer 1 are also reduced on AT90PWM81/161:

The following registers are not present in AT90PWM81/161:

- TCCR1C
- TCCR1A
- OCR1BH
- OCR1BL
- OCR1AH
- OCR1AL
- Bit 6 – ICPSEL1: Timer 1 Input Capture selection of GTCCR register
- Bit 3 – WGM12: Waveform Generation Mode of TCCR1B register
- Bit 2 – OCIE1B: Timer/Counter1, Output Compare B Match Interrupt Enable of TIMSK1 register
- Bit 1 – OCIE1A: Timer/Counter1, Output Compare A Match Interrupt Enable of TIMSK1 register

13 SPI

Atmel AT90PWM81/161 have not alternate SPI outputs while Atmel AT90PWM216/316 had this alternate SPI.

13.1 AT90PWM216/316

Table 13-1. MCUCR – MCU Control Register.

Bit	7	6	5	4	3	2	1	0	
	SPIPS	-	-	PUD	-	-	IVSEL	IVCE	MCUCR
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0/1	0	0	0	

- **Bit 7– SPIPS: SPI Pin Redirection**

Thanks to SPIPS (SPI Pin Select) in MCUCR Sfr, SPI pins can be redirected.

- On 32-pins packages, SPIPS has the following action:
 - When the SPIPS bit is written to zero, the SPI signals are directed on pins MISO, MOSI, SCK and SS
 - When the SPIPS bit is written to one, the SPI signals are directed on alternate SPI pins, MISO_A, MOSI_A, SCK_A and SS_A
- On 24-pins package, SPIPS has the following action:
 - When the SPIPS bit is written to zero, the SPI signals are directed on alternate SPI pins, MISO_A, MOSI_A, SCK_A and SS_A
 - When the SPIPS bit is written to one, the SPI signals are directed on pins MISO, MOSI, SCK and SS

NOTE

Programming port is always located on alternate SPI port.

13.2 AT90PWM81/161

The Bit 7 – SPIPS: SPI Pin Redirection of MCUCR is not used in AT90PWM81/161.

Table 13-2. MCUCR – MCU Control Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	PUD	RSTDIS	CKRC81	IVSEL	IVCE	MCUCR
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0/1	0	0	0	

14 USART

The USART feature is not present in Atmel AT90PWM81/161. So the following registers/bits will not provide any action:

- EUDR
- MUBRRH
- MUBRRL
- EUCSRC
- EUCSR
- EUCSRB
- EUCSRA
- UDR
- UBRRH
- UBRRL
- UCSRC
- UCSRB
- UCSRA
- Bit 6 – PRUSART: Power Reduction USART of PRR register

15 PSC0 / PSCR

The PSC0 of Atmel AT90PWM216/316 has been simplified for low cost PFC function with 12-bit accuracy. It is renamed as PSCR Block.

The main functional difference between the two PSCR is the PSC0 Synchro Error Interrupt Enable, which is not available in Atmel AT90PWM81/161.

15.1 AT90PWM216/316

This control bit was the Bit 5 – PSEIE0: PSC0 Synchro Error Interrupt Enable of PIM0 register in PSCR block.

Table 15-1. PIM0 – PSC0 Interrupt Mask Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	PSEIE0	PEVE0B	PEVE0A	-	-	PEOPE0	PIM0
Read/write	R	R	R/W	R/W	R/W	R	R	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 5 – PSEIE0: PSC 0 Synchro Error Interrupt Enable**

When this bit is set, the PSEIE0 bit (when set) generates an interrupt.

15.2 AT90PWM81/161

Table 15-2. PIM0 – PSC0 Interrupt Mask Register.

Bit	7	6	5	4	3	2	1	0	
	-	-	-	PEVE0B	PEVE0A	-	PEOEPE0	PEOPE0	PIM0
Read/write	R	R	R	R/W	R/W	R	R	R/W	
Initial value	0	0	0	0	0	0	0	0	

16 PSC1

Atmel AT90PWM81/161 have two PSCs; PSCR and PSC2. So PSC1 is not present and the following registers are not present in AT90PWM81/161:

- PIM1
- PIFR1
- PCTL1
- PCNF1
- PSOC1
- Bit 6 – PRPSC1: Power Reduction PSC1 of PRR register

17 PSC2

17.1 Analog synchronization

The PSC2 of Atmel AT90PWM81/161 provides the way to configure a delay to the analog synchronization output and to select an input blanking. This function is useful to control with more accuracy the capture of analog inputs.

This can be achieved with bits Bit 7, 6, 5 – PASDLK_n(2:0) of the new PCNFE2 register.

Table 17-1. PCNFE2 – PSC2 Extended Configuration Register.

Bit	7	6	5	4	3	2	1	0	
	PASDLK _n 2	PASDLK _n 1	PASDLK _n 0	PBFM _n 1	PELEV _n A1	PELEV _n B1	PISEL _n A1	PISEL _n B1	PCNFE2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7, 6, 5 – PASDLK_n(2:0): Analog Synchronization Output Delay or Input Blanking select**

Defines the modes for analog signal synchronization delay or input blanking.

Table 17-2. Analog signal synchronization or input blanking mode selection.

PASDLK _n 2	PASDLK _n 1	PASDLK _n 0	Description
0	0	0	No analog signal synchronization delay, no input blanking
0	0	1	No analog signal synchronization delay, input blanking using PSC clock, started on PSC end of cycle
0	1	0	No analog signal synchronization delay, input blanking using PSC clock, started on OCR SA event
0	1	1	No analog signal synchronization delay, input blanking using PSC clock, started on OCR SB event
1	0	0	Analog signal synchronization delay with PSC clock, no input blanking
1	0	1	Analog signal synchronization delay with PSC clock /2, no input blanking
1	1	0	Analog signal synchronization delay with PSC clock /4, no input blanking
1	1	1	Analog signal synchronization delay with PSC clock /8, no input blanking

17.2 Balance flank width modulation

AT90PWM81/161 provides additional balance flank width modulation control for lighting applications. This is achieved with Bits 4:0 of PCNFE2 register (see [Table 17-3](#)).

Table 17-3. PCNFE2 – PSC2 Extended Configuration Register.

Bit	7	6	5	4	3	2	1	0	
	PASDLK _n 2	PASDLK _n 1	PASDLK _n 0	PBFM _n 1	PELEV _n A1	PELEV _n B1	PISEL _n A1	PISEL _n B1	PCNFE2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 4 – PBFM_n1: Balance Flank Width Modulation, bit 1**

Defines the flank width modulation, together with PBFM_n0 bit in PCTL_n register.

Table 17-4. Balance Flank Width Modulation Configuration bits.

PBFMn1	PBFMn0	Description
0	0	Flank width modulation operates on RB (On-Time 1 only)
0	1	Flank width modulation operates on RB + RA (On-Time 0 and On-Time 1)
1	0	Flank width modulation operates on SB (Dead-Time 1 only)

18 ADC

18.1 ADC I/O

In Atmel AT90PWM81/161, the GPIO PE3 which has the AREF/ADC6 toggle alternate functions can only be used as a digital output pin. ADC6 has no digital input function while it was on Atmel AT90PWM216/316.

See the differences between the DIDR0 - Digital Input Disable Register 0 and DIDR1 - Digital Input Disable Register 1 described in Chapter 21.

18.2 Number of amplifiers

As already described in Chapter 7, AT90PWM81/161 has only one amplifier; AMP0.

So the AMP1CSR register of Atmel AT90PWM216/316 will have no action in AT90PWM81/161.

In AT90PWM216/316, the configuration 1100 of Bits 3, 2, 1, 0 – MUX3, MUX2, MUX1, and MUX0: ADC Channel Selection Bits of ADMUX Register selected the AMP1 as ADC input.

In AT90PWM81/161, which has not the AMP1, this configuration has been reused to select the temperature sensor.

Table 18-1. ADMUX – ADC Multiplexer Register.

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	-	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/write	R/W	R/W	R/W	-R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 3, 2, 1, 0 – MUX3, MUX2, MUX1, MUX0: ADC Channel Selection Bits**

In AT90PWM216/316: 1100 selects AMP1.

In AT90PWM81/161: 1100 selects the temperature sensor (V_{TEMP}).

18.3 Amplifier configuration

An improvement has been added in AT90PWM81/161 amplifier:

An internal connection of negative input to ground can be configured.

If done, the AMP0- input is open and PD5/AMP0- pin is free for another use. At the same time the negative input of the amplifier is internally grounded.

This function is achieved with control of Bit 3: APMP0GS of AMP0CSR register.

Amplifier 0 Control and Status register – AMP0CSR.

Table 18-2. AMP0CSR – Amplifier 0 Control and Status Register.

Bit	7	6	5	4	3	2	1	0	
	AMP0EN	AMP0IS	AMP0G1	AMP0G0	AMP0GS	-	AMP0TS1	AMP0TS0	AMP0CSR
Read/write	R/W	R/W	R/W	R/W			R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

19 Analog comparators

19.1 Analog comparator numbers and clock divider

- In Atmel AT90PWM81/161 the name of the three comparators registers have been modified:
In Atmel AT90PWM216/316, the analog comparators are named: AC2CON – AC1CON – AC0CON, while they are respectively: AC3CON - AC2CON – AC1CON in AT90PWM81/161

The only change is the address of the registers.

- Analog comparator of AT90PWM81/161 has been improved and clock divider is no more mandatory for a 16MHz clock

The result of these two changes is detailed in sections [19.1.1](#) and [19.1.2](#).

19.1.1 AT90PWM216/316

In AT90PWM216/316, the ACCKDIV clock divider bit was in ACSR register. It is no more present in AT90PWM81/161.

Table 19-1. ACSR – Analog Comparator Status Register.

Bit	7	6	5	4	3	2	1	0	
	ACCKDIV	AC2IF	AC1IF	AC0IF	-	AC2O	AC1O	AC0O	ACSR
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

• Bit 7 – ACCKDIV: Analog Comparator Clock Divider

The analog comparators can work with a clock up to 8MHz@3V and 16MHz@5V.

Set this bit in case the clock frequency of the microcontroller is higher than 8MHz to insert a divider by two between the clock of the microcontroller and the clock of the analog comparators.

Clear this bit to have the same clock frequency for the microcontroller and the analog comparators.

19.1.2 AT90PWM81/161

User must take care that the ACnIF (Analog Comparator Interrupt Flag) and ACnO (Analog Comparator outputs) have been shifted (and renamed) one position on the left.

Table 19-2. ACSR – Analog Comparator Status Register.

Bit	7	6	5	4	3	2	1	0	
	AC3IF	AC2IF	AC1IF	-	AC3O	AC2O	AC1O		ACSR
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Bits 7/6/5: AC3IF/AC2IF/AC1IF were bits 6/5/4: AC2IF/AC1IF/AC0IF of AT90PWM216/316.

The Bits 3/2/1: AC3O/AC2O/AC1O were bits 2/1/0: AC2O/AC1O/AC0O of AT90PWM216/316.

The Bit 7: ACCKDIV of AT90PWM216/316 is not present in AT90PWM81/161 and is replaced with AC3IF bit.



19.2 Analog comparator hysteresis

Analog comparators of Atmel AT90PWM81/161 have been improved to provide a configuration of the hysteresis level:

Three hysteresis values (0, $\pm 10\text{mV}$, $\pm 25\text{mV}$) can be selected thanks to the Bits 2, 1, 0— ACnH2, ACnH1, ACnH0: Analog Comparator Hysteresis select bits of the new AC3ECON/AC2ECON/AC1ECON registers.

Table 19-3. ACnECON – Analog Comparator n Extended Control Register.

Bit	7	6	5	4	3	2	1	0	
			ACnOI	ACnOE	AC1ICE	ACnH2	ACnH1	ACnH0	ACnECON
Read/write			R/W	R/W	R/W	R/W	R/W	R/W	
Initial value			0	0	0	0	0	0	

19.3 Analog comparator output

In AT90PWM81/161 the analog comparator output can be enabled/disabled, and can also be inverted while these configurations could not be changed in Atmel AT90PWM216/316.

In AT90PWM81/161, the ACnECON registers have been added:

Table 19-4. ACnECON – Analog Comparator n Extended Control Register.

Bit	7	6	5	4	3	2	1	0	
			ACnOI	ACnOE	AC1ICE	ACnH2	ACnH1	ACnH0	ACnECON
Read/write			R/W	R/W	R/W	R/W	R/W	R/W	

- **Bit 5 – AC1OI: Analog Comparator n Output Invert**

Set this bit to invert the analog comparator n output.

Clear this bit to keep the analog comparator n output.

- **Bit 4 – AC1OE: Analog Comparator n Output Enable**

Set this bit to enable the analog comparator n output pin.

19.4 Timer/Counter1 capture on analog comparator event

In AT90PWM216/316, bit AC1ICE: Analog Comparator 1 Interrupt Capture Enable bit was Bit 3 of AC1CON.

In AT90PWM81/161, bit AC1ICE: Analog Comparator 1 Interrupt Capture Enable bit has been moved to Bit 3 of AC1ECON (see [Table 19-5](#)).

Table 19-5. ACnECON – Analog Comparator n Extended Control Register.

Bit	7	6	5	4	3	2	1	0	
			ACnOI	ACnOE	AC1ICE	ACnH2	ACnH1	ACnH0	ACnECON
Read/write			R/W	R/W	R/W	R/W	R/W	R/W	

20 DAC

The DAC output of Atmel AT90PWM81/161 cannot be enabled/disabled. So DAC value of AT90PWM81/161 cannot be output on an I/O pin while it was possible for Atmel AT90PWM216/316.

20.1 AT90PWM216/316

Table 20-1. DACON – Digital to Analog Conversion Control Register.

Bit	7	6	5	4	3	2	1	0	
	DAATE	DATS2	DATS1	DATS0	-	DALA	DAOE	DAEN	DACON
Read/write	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 1 – DAOE: Digital to Analog Output Enable bit**

Set this bit to output the conversion result on D2A output.

Clear it to use the DAC internally.

20.2 AT90PWM81/161

Table 20-2. DACON – Digital to Analog Conversion Control Register.

Bit	7	6	5	4	3	2	1	0	
	DAATE	DATS2	DATS1	DATS0	-	DALA	-	DAEN	DACON
Read/write	R/W	R/W	R/W	R/W	-	R/W	-	R/W	
Initial value	0	0	0	0	0	0	0	0	

The BIT 1: DAOE of DACON Register is no more present in AT90PWM81/161.

21 I/O registers

21.1 DIDR0/DIDR1 registers

The bits locations in DIDR0 and DIDR1 have been changed between the two products. See the following tables.

Table 21-1. Digital Input Disable Register 0/1 – DIDR0/1 versus AT90PWM216/316 and AT90PWM81/161.

DIDR0 – AT90PWM216/316

Bit	7	6	5	4	3	2	1	0	
	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D ACMPM	ADC2D ACMP2D	ADC1D	ADC0D	DIDR0

DIDR0 – AT90PWM81/161

Bit	7	6	5	4	3	2	1	0	
	ADC8D AMP3D	ADC7D AMP0-D	ADC5D ACMP2D	ADC4D ACMP3D	ADC3D ACMPMD	ADC2D ACMP2MD	ADC1D	ADC0D ACMP1D	DIDR0

DIDR1 – AT90PWM216/316

Bit	7	6	5	4	3	2	1	0	
			ACMP0D	AMP0PD	AMP0ND	ADC10D ACMP1D	ADC9D AMP1PD	ADC8D AMP1ND	DIDR1

DIDR1 – AT90PWM81/161

Bit	7	6	5	4	3	2	1	0	
					ACMP1MD	AMP0+D	ADC10D	ADC9D	DIDR1

21.2 Analog input functions of DIDR0/DIDR1 bits

Table 21-2. Analog input configurations versus AT90PWM216/316 and AT90PWM81/161.

	AT90PWM216/316	AT90PWM81/161
ADC0	DIDR0.0	DIDR0.0
ADC1	DIDR0.1	DIDR0.1
ADC2	DIDR0.2	DIDR0.2
ADC3	DIDR0.3	DIDR0.3
ADC4	DIDR0.4	DIDR0.4
ADC5	DIDR0.5	DIDR0.5
ADC6	DIDR0.6	See Section 17.1
ADC7	DIDR0.7	DIDR0.6
ADC8	DIDR1.0	DIDR0.7
ADC9	DIDR1.1	DIDR1.0
ADC10	DIDR1.2	DIDR1.1

21.3 Analog comparator input functions of DIDR0/DIDR1 bits

Table 21-3. Analog comparator input configurations versus AT90PWM216/316 and AT90PWM81/161.

		AT90PWM216/316			AT90PWM81/161
Analog comp.2	Pos. input	DIDR0.2	Analog comp.3	Pos. input	DIDR0.7
				Neg. input	DIDR0.4
Analog comp.1	Pos. input	DIDR1.2	Analog comp.2	Pos. input	DIDR0.5
				Neg. input	DIDR0.2
Analog comp.0	Pos. input	DIDR1.5	Analog comp.1	Pos. input	DIDR0.0
				Neg. input	DIDR1.3
Analog comp. common	Common neg. input	DIDR0.3		Common neg. input	DIDR0.3

21.4 Analog amplifier input functions of DIDR0/DIDR1 bits

Table 21-4. Analog amplifiers input configurations versus AT90PWM216/316 and AT90PWM81/161.

		AT90PWM216/316			AT90PWM81/161
AMP0	Pos. input	DIDR1.4	AMP0	Pos. input	DIDR1.2
	Neg. input	DIDR1.3		Neg. input	DIDR0.6
AMP1	Pos. input	DIDR1.1	AMP1	Pos. input	N/A
	Neg. input	DIDR1.0		Neg. input	N/A



22 Table of contents

Features	1
1 Introduction	2
2 Reset	4
3 Interrupt vectors	5
4 Clock	6
4.1 Clock sources	6
4.1.1 CLKSELR – Clock Selection Register	6
4.1.2 CLKCSR – Clock Control and Status Register	7
4.2 RC oscillator	8
5 PLL	9
5.1 AT90PWM216/316	9
5.2 AT90PWM81/161	9
6 Bandgap.....	10
6.1 BGCCR – Bandgap Calibration Current Register	10
6.2 BGCRR – Bandgap Calibration Resistor Register	10
7 VREF	11
7.1 AT90PWM216/316	11
7.2 AT90PWM81/161	12
8 Temperature sensor	13
8.1 AT90PWM216/316	13
8.2 AT90PWM81/161	14
9 PortC	15
10 EEPROM	16
11 INT3	17
12 Timers	18
12.1 Timer0	18
12.2 Timer1	19
13 SPI	20
13.1 AT90PWM216/316	20
13.2 AT90PWM81/161	20
14 USART.....	21
15 PSC0 / PSCR.....	22
15.1 AT90PWM216/316	22
15.2 AT90PWM81/161	22
16 PSC1	23

17 PSC2	24
17.1 Analog synchronization	24
17.2 Balance flank width modulation	24
18 ADC	26
18.1 ADC I/O	26
18.2 Number of amplifiers	26
18.3 Amplifier configuration	26
19 Analog comparators	27
19.1 Analog comparator numbers and clock divider	27
19.1.1 AT90PWM216/316	27
19.1.2 AT90PWM81/161	27
19.2 Analog comparator hysteresis	28
19.3 Analog comparator output	28
19.4 Timer/Counter1 capture on analog comparator event	28
20 DAC	29
20.1 AT90PWM216/316	29
20.2 AT90PWM81/161	29
21 I/O registers	30
21.1 DIDR0/DIDR1 registers	30
21.2 Analog input functions of DIDR0/DIDR1 bits	30
21.3 Analog comparator input functions of DIDR0/DIDR1 bits	31
21.4 Analog amplifier input functions of DIDR0/DIDR1 bits	31
22 Table of contents	32



Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parking 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
16F, Shin Osaki Kangyo Bldg.
1-6-4 Osaki Shinagawa-ku
Tokyo 104-0032
JAPAN
Tel: (+81) 3-6417-0300
Fax: (+81) 3-6417-0370

© 2012 Atmel Corporation. All rights reserved.

Atmel®, Atmel logo and combinations thereof, AVR®, and others are registered trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.