ATF15xx Product Family Conversion

Introduction

The ATF15xx Complex Programmable Logic Device (CPLD) product family offers high-density and high-performance devices. Atmel currently offers the ATF1500A, ATF1502AS, ATF1504AS and the ATF1508AS CPLDs. The ATF1500A is a 32 macrocell device and is offered in 44-lead PLCC/TQFP package. The ATF1502AS is a 32 macrocell ISP device and is offered in 44-lead PLCC/TQFP package. The ATF1504AS is a 64 macrocell ISP device and is offered in 44-lead TQFP/PLCC, 68-lead PLCC, 84-lead PLCC and 100-lead TQFP/PQFP packages. The ATF1508AS is a 128 macrocell ISP device and is offered in 84-lead PLCC, 100-lead TQFP/PQFP, 160-lead PQFP packages.

ATMEL also offers low-power and low-voltage devices in the ATF15xx family as shown in Table 1.

This application note acts as a guide to use the Atmel POF2JED software utility. This utility converts a programming output file (.POF file) to the Atmel programming file (.JED) without any functionality or performance loss. It is available on the Atmel BBS and website.

Table 1. Atmel's ATF15xx Family

Atmel Device	ISP Capability	Description
ATF1500A	No	5V Standard Power Device
ATF1500AL	No	5V Low-power Device
ATF1500ABV	No	3.3V Standard Power Device
ATF1502AS ATF1504AS ATF1508AS	Yes	5V Standard Power Device
ATF1502ASL ATF1504ASL ATF1508ASL	Yes	5V Low-power Device
ATF1502ASV ATF1504ASV ATF1508ASV	Yes	3.3V Standard Power Device
ATF1502ASVL ATF1504ASVL ATF1508ASVL	Yes	3.3V Low-power Device

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Application Note

Rev. 0916C–03/01

Target Devices

Table 2 lists the competitor devices that can be converted over to their Atmel equivalents. The earliest version of POF2JED software that can do any accurate conversion for the equivalent competitor device is also listed. The information is subject to change as new devices are added. Contact Atmel PLD Applications or your local Atmel sales offices for the latest information.

Table 2. List of Target Devices

Competitor	Atmel	POF2JED Version
7032LC44	1500A-J44	3.30
7032TC44	1500A-A44	3.30
7032VLC44	1500ABV-J44	3.30
7032VTC44	1500ABV-A44	3.30
7032SLC44	1502AS-J44	4.20
7032STC44	1502AS-A44	4.20
7032AELC44	1502ASV-J44	4.20
7032AETC44	1502ASV-A44	4.20
3032ALC44	1502ASV-J44	4.41(1)
3032ATC44	1502ASV-A44	4.41(1)
7064LC44	1504AS-J44	3.30
7064TC44	1504AS-A44	3.30
7064LC68	1504AS-J68	3.30
7064LC84	1504AS-J84	3.30
7064QC100	1504AS-Q100	3.30
7064TC100	1504AS-A100	3.30
7064SLC44	1504AS-J44	3.30
7064STC44	1504AS-A44	3.30
7064SLC84	1504AS-J84	3.30
7064SQC100	1504AS-Q100	3.30
7064STC100	1504AS-A100	3.30
7064AETC44	1504ASV-A44	4.20
7064AELC44	1504ASV-J44	4.20
7064AETC100	1504ASV-A100	4.20
3064ATC44	1504ASV-A44	4.41(1)
3064ALC44	1504ASV-J44	4.41(1)
3064ATC100	1504ASV-A100	4.41(1)
7128ELC84	1508AS-J84	3.30
7128LC84	1508AS-J84	3.30
7128SLC84	1508AS-J84	3.30

Table 2. List of Target Devices (Continued)

Competitor	Atmel	POF2JED Version
7128EQC100	1508AS-Q100	3.30
7128QC100	1508AS-Q100	3.30
7128SQC100	1508AS-Q100	3.30
7128EQC160	1508AS-Q160	3.30
7128QC160	1508AS-Q160	3.30
7128SQC160	1508AS-Q160	3.30
7128STC100	1508AS-A100	3.30
7128ALC84	1508ASV-J84	4.20
7128ATC100	1508ASV-A100	4.42
7128AELC84	1508ASV-J84	4.20
7128AETC100	1508ASV-A100	4.41(1)
3128ATC100	1508ASV-A100	4.41(1)

Note: 1. POF2JED Version 4.41 also supports setting the I/O drivers on the ground pins to Tri-state.

How to Use POF2JED?

POF2JED utility is executed at the DOS prompt. The program does conversion automatically taking into consideration the proper device and package.

```
Command: POF2JED filename.POF
```

The output is a JEDEC (.JED) file that is used to program the Atmel CPLD. A report that shows the results of the conversion is also generated (.TXT file).

Note: A UNIX version is available. Please contact Atmel PLD Applications for more information.

To list command line options type:

POF2JED [device option]

Select one of the following device options:

-1500A
-1502AS
-1504AS
-1508AS
-1502ASV
-1504ASV
-1508ASV

A JEDEC file generated for the 5V/3V standard power device type can be used to program the 5V/3V low-power device type. For example, a JEDEC file generated for the ATF1502AS device can be used to program the ATF1502ASL device. For example,

```
POF2JED filename.pof -device 1502asv -secure -
race_cover_off
```

This will secure the device and will not add race condition coverage when converting “filename.pof” to generate “filename.jed” for an ATF1502ASV part.

Standard Command Line Options

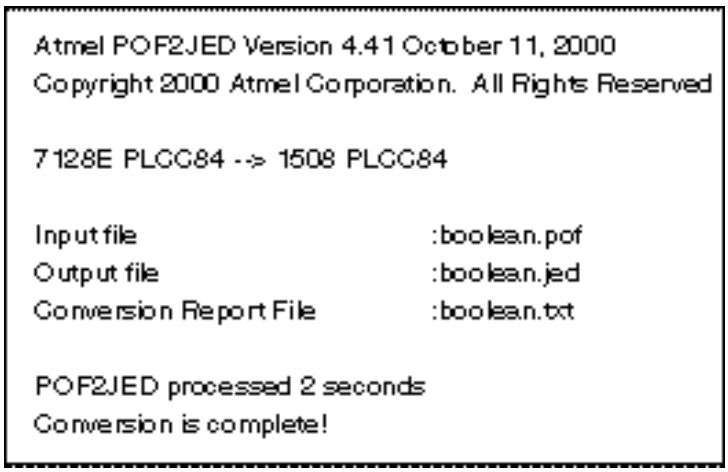
-i	Specify the input file name (.POF).	
-o	Specify the output filename (.JED).	
-device	Specify the target device (1500A, 1502AS, 1504AS, 1508AS, 1502ASV, 1504ASV, 1508ASV).	
	1500A	Use this device type to generate a JEDEC file for the ATF1500A/ABV device. This is only applicable for 7032/7032V POF files. Note: The ATF1500A device replaced the ATF1500 device (-1500), which is a discontinued device.
	1502AS	Use this device type to generate a JEDEC file for the ATF1502AS/ASL, when the original POF file is for the 7032/7032V device which otherwise will generate a JEDEC file for the ATF1500A/ABV device (by default).
	1502ASV 1508ASV 1504ASV	When the ASV device option is specified, the screen will display that the target device is a low-voltage device and power-reset hysteresis will default to “LARGE”. POF2JED will now create the same JEDEC file as it did for the 5V parts and the (.TXT) file documenting the conversion will show an ASV part.
-PD1	Enables the Power-down mode on pin PD1 for ATF15XX family of devices (defaults to Disabled).	
-PD2	Enables the Power-down mode on pin PD2 for ATF15XX family of devices (defaults to Disabled). Either PD1 or PD2 pins or both can be used to power-down the part. This option can also be selected in the design source file. A logic high on these pins brings the device into the Power-down mode. Any time the pin is asserted, the device will switch into a standby power mode and ignore all inputs. All pin transitions are ignored until the PD pin is brought to a logic low. Note: The translator may override this option setting if you enable this mode, but the Design is using the PD pin for Design Logic.	
-powerdown	Enables the Power-down mode (ATF1500, ATF1500A only – defaults to Disabled).	
-pinclk	Uses pin clock wherever applicable. Global clock will be used for Product term Clock. This helps to improve performance of the design (defaults to Disabled).	
-race_cover_off	Turns off race coverage option (defaults to on). This conversion will be the same as implemented in the POF output file. However, if turned on, it will detect any potential hazards and accordingly allocate additional resources available to correct the hazards. If the hazards cannot be corrected a warning will appear in the report file.	
-secure	Sets security bit on (defaults to off). A JEDEC file with the security bit enabled will be generated. When this JEDEC file is programmed into the devices it will be secured. When the device is secured it cannot be read and will perform normally in the design.	
-slew [fast|slow|auto]	Sets slew rate for all outputs (7000/7000E – defaults to fast; 7000S/7000A/7000AE/3000A – defaults to auto).	
	fast	Sets output slew rate to fast. A faster slew rate provides high-speed transitions and may introduce more noise transients.
	slow	Sets output slew rate to slow and thereby reduces system noise. However, it does introduce a nominal delay.
	auto	Follows settings from POF file. Depending on the device type the outputs would either be fast or slow.
-pin_keep	Enables pin-keeper circuits (defaults to Disabled). The pin-keeper circuits eliminate the need for external pull up resistors and eliminate their DC power consumption.	

Advanced Command Line Options Applicable to ATF15xx Family (1502AS/1504AS/1508AS)

-mc_power [on|off|auto]	Sets Reduced Power mode for all Macrocells (MCs)[2] (defaults to auto).	
	on	Turns on Reduced Power mode for all MCs.
	off	Turns off Reduced Power mode for all MCs.
	auto	Follows settings from POF file.
	When this feature is turned on, power consumption is reduced. All MCs draw approximately one-half the power in the reduced power mode compared to the standard power mode. There is a speed penalty when this option is enabled. Consult the device datasheet for details.	
-power_reset	Sets device power-up reset hysteresis to large. This feature allows the device to reset only when V_{CC} turns off. This feature must be enabled if the power-down mode is enabled (-PD1 and/or -PD2 option) – (defaults to Disabled). Please refer to a Technical Bulletin "Choosing ATMEL ATF150XASV(L) POR options" for additional description. This bulletin is available on our website.	
-GCLK1_ ITD	Disables ITD (Input Transition Detection circuitry) fuse on GCLK1 – (defaults to enabled).	
-GCLK2_ ITD	Disables ITD (Input Transition Detection circuitry) fuse on GCLK2 – (defaults to enabled).	
-GCLK3_ ITD	Disables ITD fuse on GCLK3 (defaults to enabled). The ITD feature allows the user to save power by controlling whether the device will wake up on each clock edge even if no inputs are transitioning. When the feature is disabled, the devices will not wake up on each transition of the selected pin clock input. When enabled the pin clock transition will wake up the part. Note: The POF2JED will automatically enable/disable this feature depending on the type of design that is being converted. If any of the GCLK[1:3] pin goes to the Universal Interconnect Matrix, the ITD circuitry is always enabled, overriding the user setting. This only applies to "L/Z" devices.	
-open_out [on|off|auto]	Sets all MC output types. (7000/7000E: defaults to off; 7000S/7000A/7000AE/3000A – defaults to auto).	
	on	Sets Open Collector mode. Here the outputs are of open collector type for each I/O pin. This enables the device to provide control signals that can be asserted by one of several inputs.
	off	Sets to Normal mode
	auto	Follows settings from POF file.
-JTAG [on|auto]	Sets JTAG mode. (7000/7000E: defaults to off; 7000S/7000A/7000AE/3000A – defaults to auto). When this option is turned on, the four JTAG port pins are disabled for use as I/O pins. When a JEDEC file with the JTAG bit "on" is programmed into an ATMEL ISP device, the JTAG port will automatically be enabled. (The ATF15xx family of devices are shipped to customers in the erased state thereby enabling the JTAG port by default).	
	on	Enables JTAG mode.
	auto	Follows settings from POF file.
-TDI_PULLUP	Enables pull-up (10 KΩ) on TDI pin for 7000S/7000A/7000AE/3000A only (defaults to Disabled).[1]	
-TMS_PULLUP	Enables pull-up (10 KΩ) on TMS pin for 7000S/7000A/7000AE/3000A only (defaults to Disabled).[1]	

Notes: 1. JTAG bit is enabled automatically.
2. MC stands for Macrocell.

A screen snapshot of a conversion will look as follows:



Listing of Common Warning Messages

The following table has a listing of typical messages that appear in the DOS window in the process of running a POF2JED conversion.

Warning Message	Meaning
GCLK2 ITD setting override (ignore user request to disable) GCLK2 pin is used as a logic input so ITD wake-up enable is forced on.	This message appears if the user tries to use the -GCLK2_ITD option when running a POF2JED conversion. This means that the GCLK2_ITD option is enabled but the design is using the GCLK2 pin as input. Note: This will not affect the current consumption or behavior of a Standard power(5V/3V) device.
JTAG on: Error! Some or all four JTAG pins are used in your logic function. JTAG mode cannot be enabled.	This message appears if you try to turn on the JTAG port using the -JTAG ON option and the design is using the JTAG pins for logic I/O.
If Conversion is for a low voltage device, please use the -power_reset option.	This message appears if the conversion is for an EPM7000/7000E/7000S POF file. If the target device is a 3.3V device then the user can either: • Use -power_reset option • Use -device 150XASV which will automatically set power_reset bit thereby enabling large hysteresis.

Enhanced Architecture Conversion Issues Specific to ATF15xx Family (1502AS/1504AS/1508AS)

How to Reduce Power Consumption and attain µA standby current with "Z" devices

- In order to reduce power consumption, use "L/Z" devices.
- Disable the ITD on the Global Clock pins (GCLK[1:3]. If any of the GCLK[1:3] pin goes to the Universal Interconnect Matrix, the ITD circuitry is enabled. The ITD feature allows the user to save power by controlling whether the device will wake up on each clock edge even if no inputs are transitioning. When the feature is disabled, the devices will not wake up on each transition of the selected pin clock input thus conserving power.
- Turn on when applicable the reduced power option (mc_power). This will put all macrocells into the reduced power mode.

Note: There is a speed penalty when using this option.

- Enable Pin-keeper circuits (-pin_keep).
- Set Slew option to slow and thereby reduce dynamic I_{CC} (-slew slow).
- Ensure that in "L/Z" designs there is a large decoupling capacitor. The "L/Z" device requires a large transient current from V_{CC} when waking-up the device from standby to active mode. This transient current can be supplied by using decoupling capacitors. A 0.22 µF ceramic capacitor is recommended for typical applications. You may also refer to the applications note, "Selecting Decoupling Capacitors for Atmel PLDs", available on Atmel's Website.
- Use the Power_Reset option to put the device into the large hysteresis mode. This reduces the standby I_{CC} by approximately 1mA

Pin-keeper Issues

- All members of the ATF15xx product family have active Pin-keeper circuits. Ensure that I/O or input pull-up/pull-down resistors do not contend with Pin-keeper circuits. Pin-keeper circuits have a 40 µA drive. These circuits ensure that a signal holds its previous state after the pin has been tristated.
- Problems can occur when you have 100 KΩ pull-up or 30 KΩ pull-down resistors on the I/O pins. These resistors will contend with the pin-keeper circuits. If a design uses pull-up on the inputs or outputs of an ATF1508AS, a 10 KΩ is recommended. For pull-down, a 5K resistor is recommended.
- POF2JED automatically disables Pin-keeper circuits for ATF15xx family of devices (by default).

Power-on Reset Issue

- Use the -Power_Reset feature if you are unsure about power regulation on circuit board or if the V_{CC}/GND pins are noisy.
- When you use one of the power-down pins (PD1 or PD2) to power-down the device, the Power_Reset option must be turned ON. This puts the device in dual-point reset mode and ensures that the device is not reset unless the V_{CC} is turned off.

JTAG Conversion Issues

When converting from a 7128S or any 7000 series part with JTAG capability, the POF2JED will automatically enable JTAG In-System Programming (ISP) mode of the Atmel ISP device. Refer to the TXT file generated by the POF2JED converter to determine if the JTAG port is enabled. If it is enabled, then the device can be re-programmed through ISP. Otherwise you will need to manually enable it by setting the JTAG ON option in the POF2JED converter. The translator will check if the design is using the JTAG port pins. If it is, an error will be generated and the Atmel ISP device can still be programmed once in the ISP mode. However, it will have to be re-programmed on an external programmer.

The Atmel ISP device also has an optional feature to enable the pull-ups for the JTAG pins TDI and TMS (-TMS_pull-up and -TDI_pull-up). If these internal pull-ups are enabled, then no external pull-ups are needed for these JTAG pins.

Low-voltage Device Support (ASV)

When the ASV device option is specified, POF2JED will still create the same JEDEC file as it did for the 5V parts but the (.TXT) file documenting the conversion will show an ASV part. It will also show up on the screen when the customer runs the POF2JED conversion.

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