PolarFire SoC FPGA Video Kit Picture-In-Picture Application Note

AN4723

Introduction (Ask a Question)

This application note describes the method to run the imaging and video demo using the PolarFire® SoC video kit, a dual camera sensor module, and an HDMI monitor. This solution is developed on Microchip's PolarFire SoC video kit, which features an MPFS250TS PolarFire SoC device.

This demo demonstrates the following features:

- MIPI CSI-2 RX to read the Full HD dual-camera input
- Color Filter Array (CFA) to Red, Green, Blue (RGB) conversion
- Display Controller
- Picture-in-Picture (PIP)
- Full HD video output through HDMI 2.0 TX port
- Edge detection
- Histogram
- Image enhancements such as contrast, brightness, color balance, and gamma correction

Important: The solution includes a user-friendly video control Graphical User Interface (GUI) to control the preceding image and video settings.

PolarFire SoC video kit enables prototyping of Video and Imaging solutions. It supports the following key features among others:

- MPFS250TS PolarFire SoC device
- MIPI CSI-2 interface
- FPGA Mezzanine Card (FMC) connector
- SD and eMMC card, LPDDR4, and DDR4 memories
- HDMI, Ethernet, PCIe, and other interfaces

For more information about the PolarFire SoC video kit, see MPFS250-VIDEO-KIT.

Table of Contents

1. Demo Requirements (Ask a Question)

The following table lists the hardware and software required for running the demo.

Table 1-1. Demo Requirements

Requirement	Description
Hardware and Accessories	
PolarFire® SoC Video kit	MPFS250-VIDEO-KIT Kit Contents: • PolarFire SoC Video kit board with MPFS250TS-1FCG1152I device • Dual Camera Sensor board – VIDEO-DC-DUALCAM • HDMI cable • Micro B USB cable – 2 • RJ45 Ethernet cable • 12V AC adapter/power cord
Image Sensor module	LI-IMX334-MIPI-MICRO v1.0
USB A to Micro-USB B cable	Required for: • FPGA programming • UART interface with the Video Control GUI
HDMI Monitor	To display the processed resultant video data for a full HD resolution (1920 x 1080).
Host PC with USB port	PC with Windows® 11/10
Software	
`.exe`	This software is used to program the FPGA.
Design Files	Link to design files: www.microchip.com/en-us/application-notes/AN4723
`mpfs_an4723_v2024p2_jb`	`.job` file to test on PolarFire SoC Video kit
Microchip FPGA_GUI_Pack	This pack includes the necessary runtime engine and drivers for the operation of the Microchip FPGA Demo GUIs.

2. Demo Prerequisites (Ask a Question)

Before you begin, ensure the following components are in place:

1. Download and install the Libero® SoC Design Suite from Libero SoC Software Downloads.
2. Download and install the Microchip FPGA_GUI_Pack from Microchip FPGA_GUI_Pack.

2.1. Libero License (Ask a Question)

The demo design supports Libero® v2024.2 and above. To get a silver license, see www.microchipdirect.com/fpga-software-products

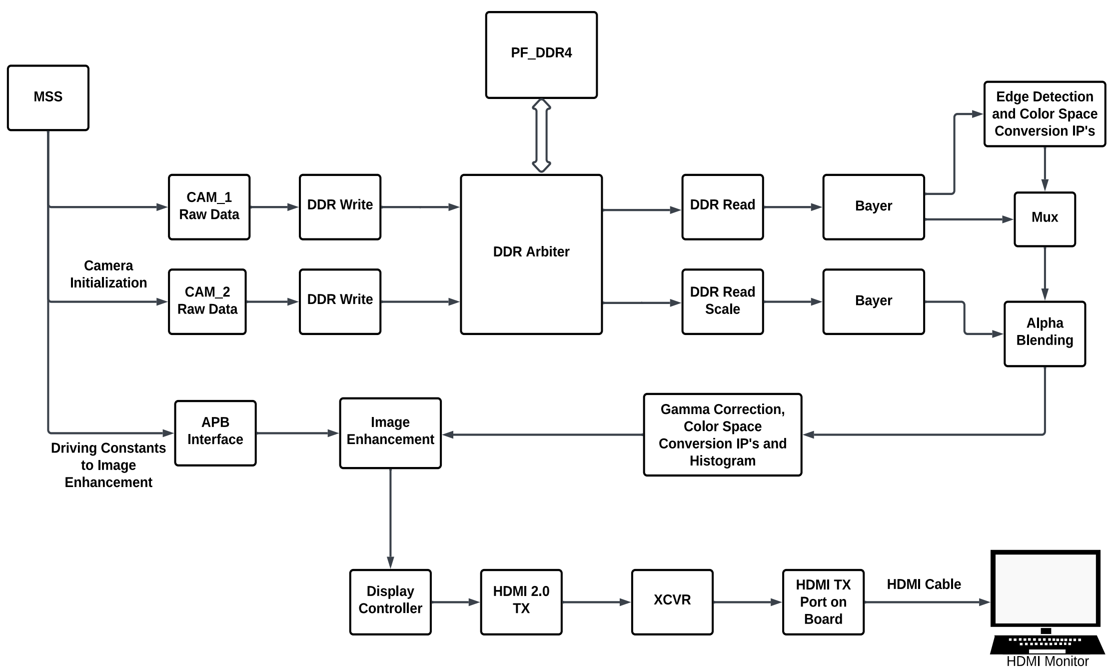
3. Design Overview (Ask a Question)

The following figure illustrates the top-level block diagram of the reference design. The system captures raw data from a dual-camera sensor module and writes it to the fabric DDR4 memory. The captured data is processed through an image processing pipeline, which includes various IP cores such as:

- Bayer Conversion
- RGB to YCbCr Transformation
- YCbCr to RGB Transformation
- Edge Detection
- Image Enhancement

Once processed, the data from both camera modules is blended using an alpha blending IP before being displayed on an HDMI-compliant device. The Microprocessor Sub-System (MSS) executes firmware that configures both camera sensor modules through I^2C channels. Additionally, a Video Control GUI enables real-time adjustments to video features such as brightness and contrast. This GUI communicates with the design on the board through a UART interface.

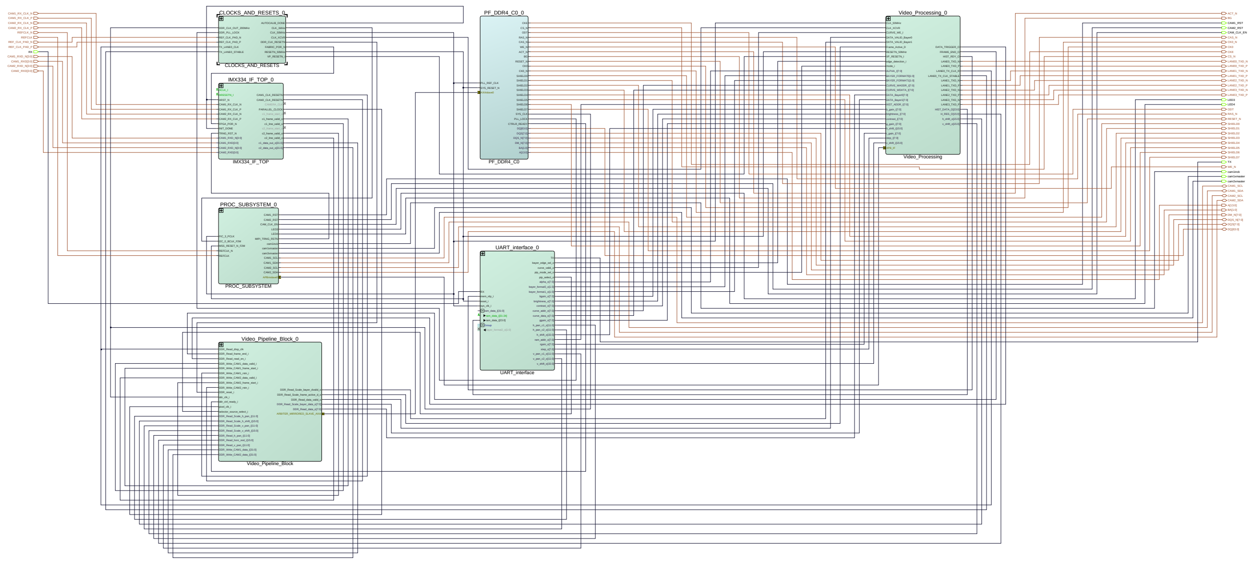
Figure 3-1. Top-Level Block Diagram



3.1. Hardware Implementation (Ask a Question)

The following figure shows the Libero SoC implementation of the top-level SmartDesign.

Figure 3-2. Top-Level SmartDesign



3.2. MSS Configuration (Ask a Question)

The following table lists the configuration of MSS clock, peripherals, and memory.

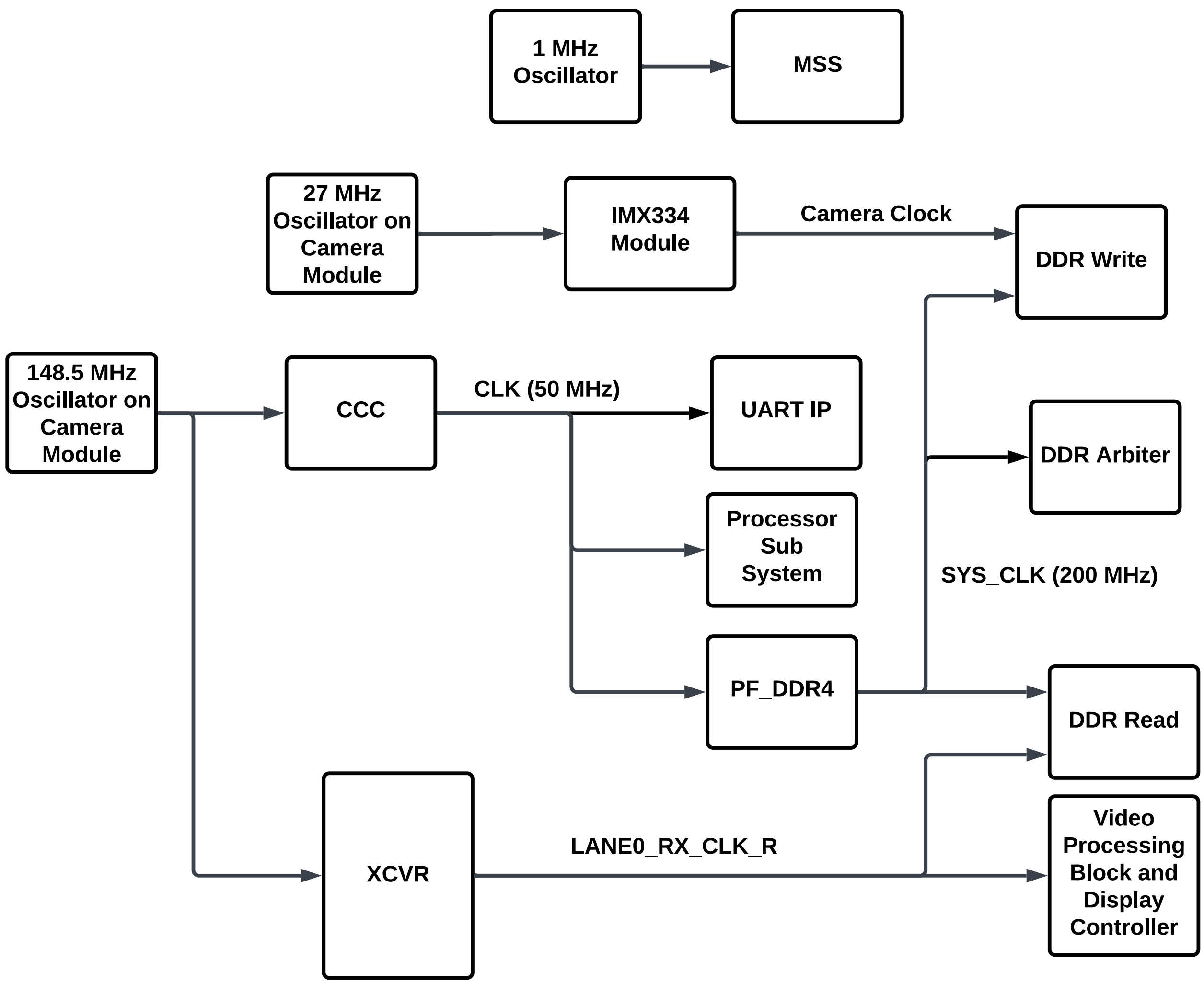
Table 3-1. MSS Configuration

MSS Block	Description
MSS Clocks	MSS PLL reference clock source: 125 MHz MSS CPU clock frequency: 600 MHz
Peripherals	I^{2}C: Used for initializing the camera
Fabric Interface Controller (FIC)	FIC3_APB_Master: Accessing camera control registers through APB interface
Low Power DDR4 (LPDDR4) memory	Low Power DDR4 memory is unused in this Picture-in-Picture design
Memory Partitioning	Since LPDDR4 is unused, memory partitioning is not used in the current design

3.3. Clocking Structure (Ask a Question)

The following figure shows the clocking structure of the design. PF_CCC_C0 generates the 50 MHz fabric clocks from the REF_CLK generated by PF_XCVR_REF_CLK. This clock drives the APB3 bus interface and provides the reference clock for the PLL inside the PF_DDR4 Controller. The on-board 148.5 MHz on-board oscillator provides a reference clock to generate clocks used in the design.

Figure 3-3. Clocking Structure

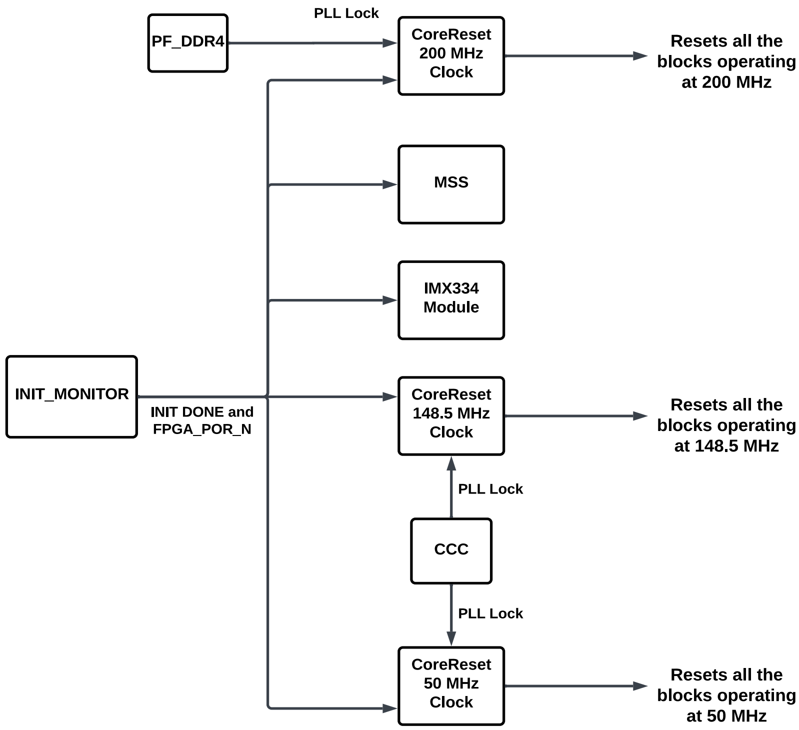


3.4. Reset Structure (Ask a Question)

The following figure shows the reset structure of the design. The INIT_MONITOR IP asserts the following signals:

- FABRIC_POR_N: Asserted after the initialization of the fabric. FABRIC_POR_N is used to reset MSS.
- DEVICE_INIT_DONE: Asserted after the initialization of the PolarFire SoC device.

Figure 3-4. Reset Structure



4. Installing the Video Control GUI (Ask a Question)

To install the Video Control GUI, perform the following steps:

1. Extract the contents of the `mpfs_an4723_v2024p2_gui.zip` file.
2. To install the demo GUI, run the `setup.exe` file from `mpfs_an4723_v2024p2_gui` with admin rights and follow the on-screen instructions.

The **Video Control GUI** is now ready for use.
Notes:

- At the end of the installation, you may be prompted to download and install the FPGA_GUI_Pack, if it is not already available on your system.
- For any queries encountered while running the installer, contact the Technical Support team.

5. Setting Up the Demo (Ask a Question)

Setting up the demo involves the following steps:

- Setting up the Hardware
- Setting up the Serial Terminal
- Programming the Device

5.1. Setting Up the Hardware (Ask a Question)

Setting up the hardware involves interfacing the camera sensor module and the HDMI monitor with the PolarFire SoC video kit.

To set up the hardware, perform the following steps:

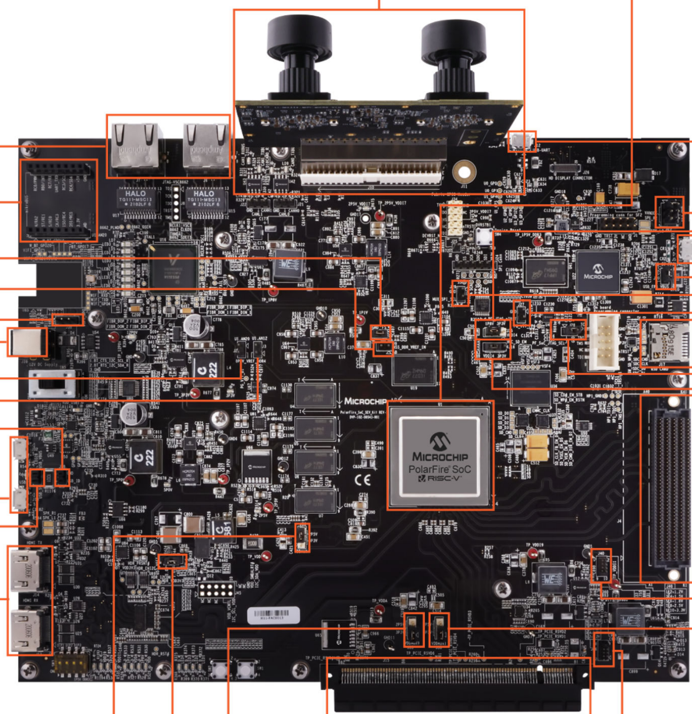
1. Connect the camera sensor module at **J10** on the video kit.
2. Connect the HDMI monitor at **J14** on the video kit using the HDMI cable.
3. Ensure that the jumpers are set correctly on the video kit, as listed in the following table.
   For more information about the default jumper settings, see the "Jumper Settings" section in PolarFire SoC FPGA Video Kit User Guide.

Table 5-1. Jumper Settings

Jumper	Default Position	Functionality
J46	9 and 10	Bank 1 voltage for UART communication
J40	9 and 10	Bank 9 voltage
J2 and J3	Open	DDR4 ref voltage
J20	1 and 2	VBUS for FlashPro 6
J23	1 and 2	Backlight LED driver VANODE
J29	Open	External on-board SPI Flash
J27	Open	JTAG TRSTB
J39	12V Input	12V input to Board
J28	1 and 2	embedded Flash Programmer 6 (eFP6)
J41	1 and 2	MSS reference 125 MHz clock
J9	Open	MSS DDR Vref
J33	1 and 2	VDDAUX9 3.3V
J30	1 and 2	VDDAUX1 3.3V
J18	Open	USB ID
J57	Open	USB VBUS
J44	1 and 2	Core voltage 1.05V

The following figure shows the jumpers on the PolarFire SoC video kit.

Figure 5-1. Board Callout



5.2. Setting Up the Serial Terminal (Ask a Question)

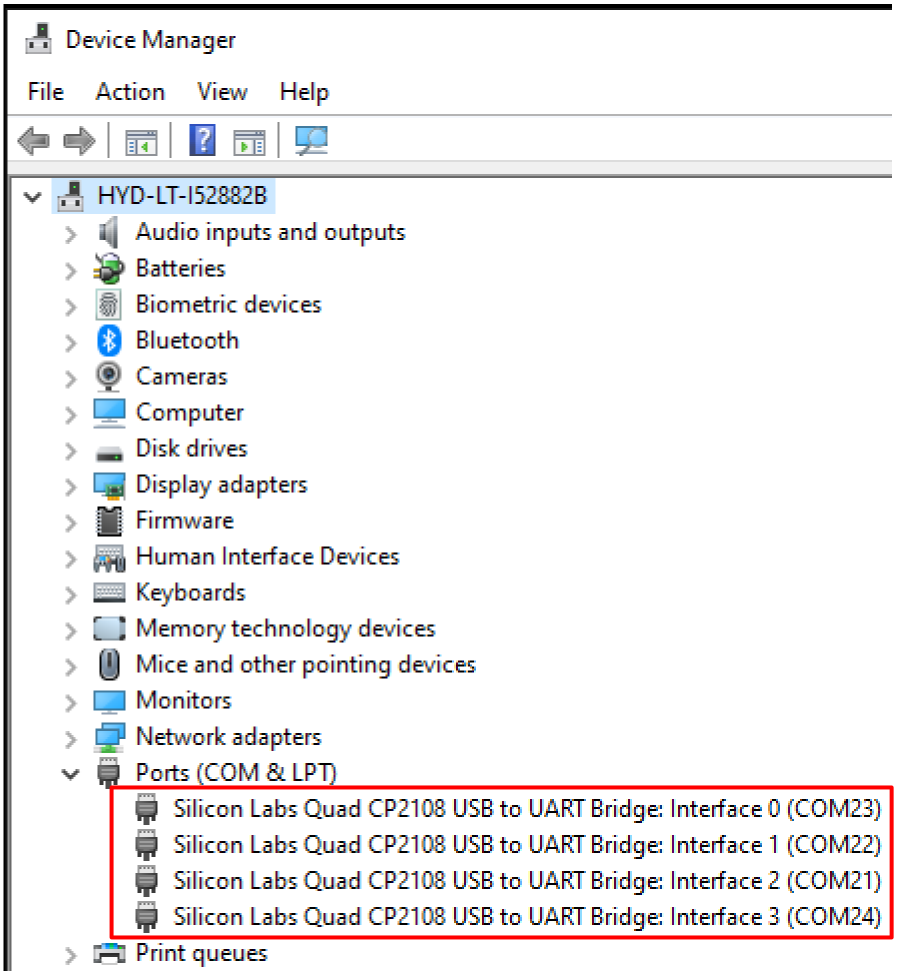
PolarFire SoC video kit includes CP2108 USB to establish communication between the video kit and host PC. Before you start, ensure these components are in place:

- Download and install CP210x Universal Windows Driver.
- Unzip and see the *CP210x_Universal_Windows_Driver_ReleaseNotes*.

After installing the driver, perform the following steps:

1. Connect USB cable at **J12** port on PolarFire SoC video kit board to the host PC.
2. After connecting power adapter to the board at **J39**, switch ON the power supply using the **SW5** switch. This must detect the USB UART chip on the board at the host PC. You can confirm this at the host PC device manager, as shown in the following figure.

Figure 5-2. Device Manager



The Interface 0 COM port (COM23) is used to connect the Video Control GUI. The interface 0 might be on a different COM port number other than the ports shown in the preceding figure.

5.3. Programming the Device (Ask a Question)

This section describes how to program the PolarFire SoC device, with the `.job` file, using FlashPro Express.

To program the device, perform the following steps:

1. Connect a micro USB to **J5** from the host PC and launch the FlashPro Express software from its installation directory.
2. To create a new job project on the **Project** menu, click **New** or **New Job Project from FlashPro Express Job**.
3. In the **New Job Project** dialog box, perform the following steps:
   – **Programming job file**: Click **Browse**, navigate to the location where the `.job` file is located, and select the file. The default location is: <download_folder\mpfs_an4723_v2024p2_jb\mpfs_an4723_v2024p2_df.
   – **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears. Verify that a programmer number (for example,

79DE6C53) appears in the **Programmer** field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

5. To program the device, click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed.
6. To close FlashPro Express, click **Project** > **Exit**.
7. Power cycle the board using the **SW5** switch.

6. Running the Demo (Ask a Question)

The demo showcases the reception of MIPI Rx data from two cameras, each supporting Full HD (FHD) resolution (1920 × 1080). The captured frames from the cameras are stored in DDR4 memory and subsequently transferred to the display in accordance with the display controller's timing parameters. On the display side, the image processing pipeline applies a series of enhancements to the raw image, including:

- Bayer Interpolation
- Gamma Correction
- Histogram Processing
- Edge Detection
- Image Enhancement

Additionally, the demo features automatic camera exposure control, which dynamically adjusts based on the surrounding lighting conditions. The display controller is responsible for generating FHD video synchronization signals, ensuring smooth and accurate video output.

The Full HD (FHD) output in the demo design supports the following advanced features:

- Picture-in-Picture (PIP)
- Edge Detection
- Image Enhancements including:
  - Contrast Adjustment
  - Brightness Control
  - Color Balance
  - Alpha Blending

A Video Control GUI is provided for image enhancements, offering a unified interface for both video outputs. This GUI enables real-time adjustments and ensures seamless control over video processing parameters.

To run the demo, perform the following steps:

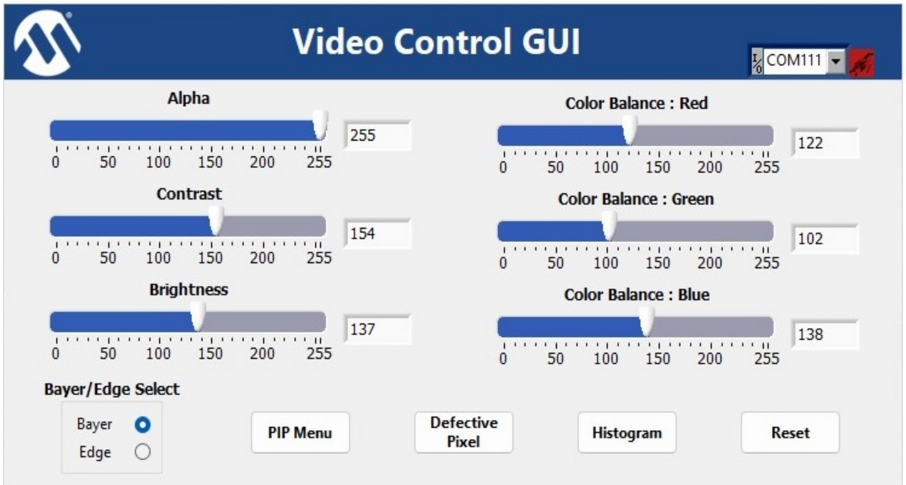
1. Verify Imaging and Video Settings – To configure and adjust imaging parameters such as brightness, contrast, color balance, and other enhancements, use the Video Control GUI.
2. Observe the Output – To confirm the applied settings and real-time adjustments, view the processed video output on an HDMI monitor.

This process ensures that the video pipeline functions correctly and the desired enhancements are applied effectively.

To use the demo GUI, perform the following steps:

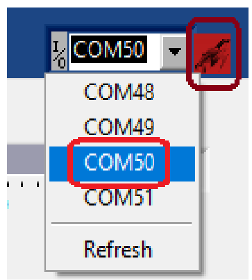
1. Launch the **Video Control GUI** from the installation directory. The GUI is displayed, as shown in the following figure.

Figure 6-1. Video Control GUI



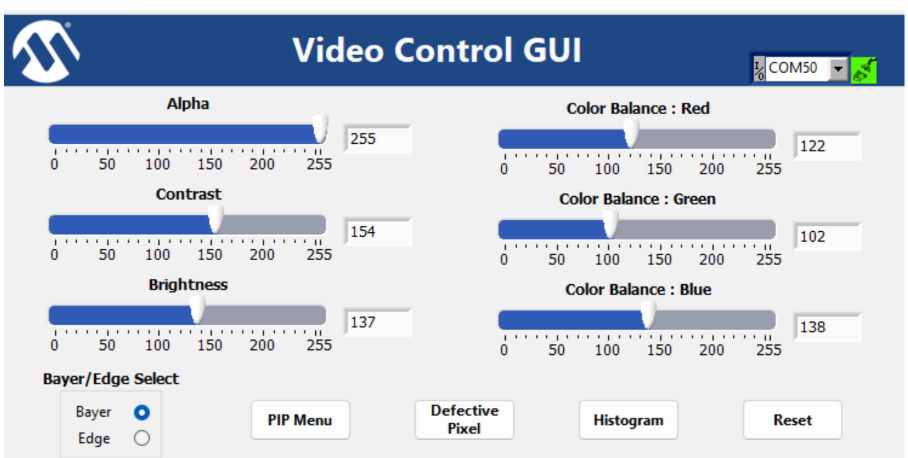
2. Select the Interface 0 (**COM23**) port, as described in Setting Up the Serial Terminal, and then click the **Connect** button.

Figure 6-2. Connecting the GUI and Video Kit



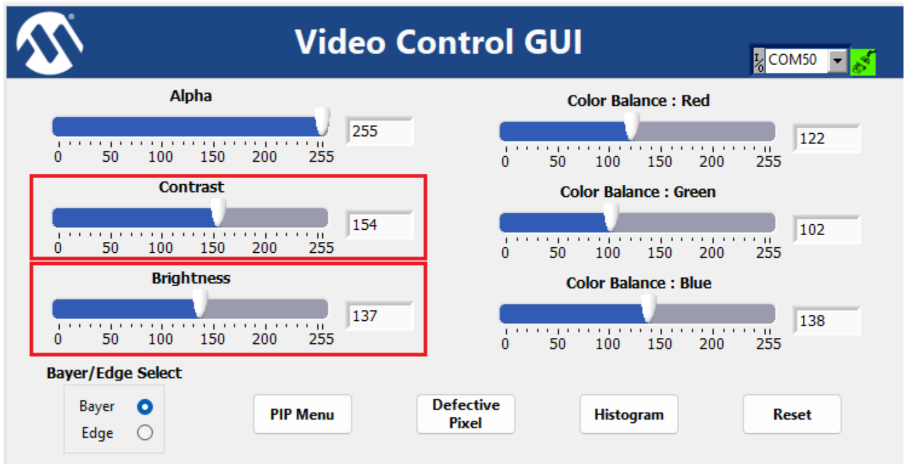
The **Connect** button turns green indicating a successful connection, as shown in the following figure.

Figure 6-3. Connection Successful



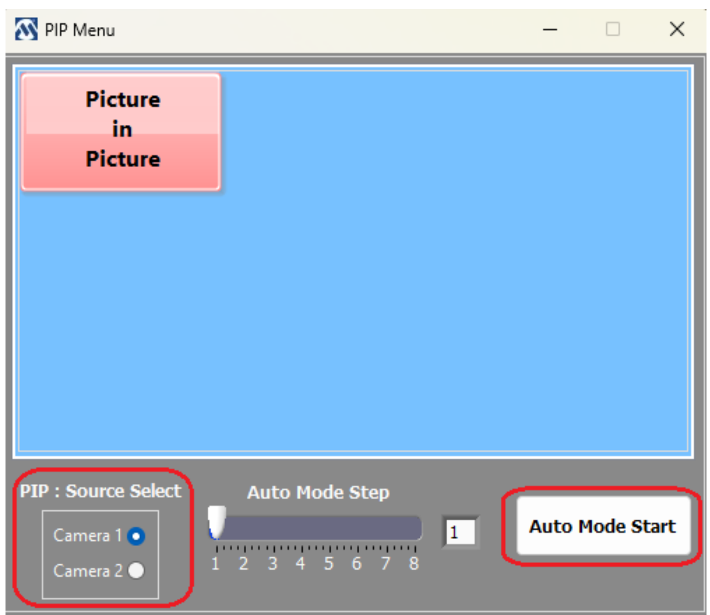
3. To adjust the contrast and brightness, and observe the change on the HDMI monitor, move the **Contrast** and **Brightness** sliders appropriately. The sliders are highlighted in the following figure.

Figure 6-4. Adjusting Contrast and Brightness



4. To adjust the color balance of the image, move the sliders using the color balance sliders.
5. To change the PIP settings, select the **PIP Menu**.
6. Select the source of the PIP window between Camera 1 and Camera 2 using **PIP: Source Select**. The position of the PIP window can be moved anywhere within the screen by dragging the pink **Picture In Picture** box. The **Auto Mode Start** option moves the PIP window automatically. The speed of this movement is controlled using the **Auto Mode Step** slider.

Figure 6-5. PIP Menu



7. Close the **PIP Menu** window.
8. To enable or disable the defective pixel functionality, navigate to the **Defective Pixel Menu**, as shown in the following figure, and select the threshold values as listed:
   - **Threshold 1**: The first detection threshold establishes the minimum absolute difference between pixels and their adjacent pixels of the same color.
   - **Threshold 2**: The second detection threshold determines how the difference in pixels compares to the differences in pixels of other colors.

Important: The defective pixel correction feature, when enabled and configured with specified thresholds, adjusts the output video to reduce the impact of dead or stuck pixels on the screen. Each pixel is compared to established threshold values. If the pixel's value falls below the threshold, it is identified as a dead pixel and eliminated.

Figure 6-6. Defective Pixel Menu

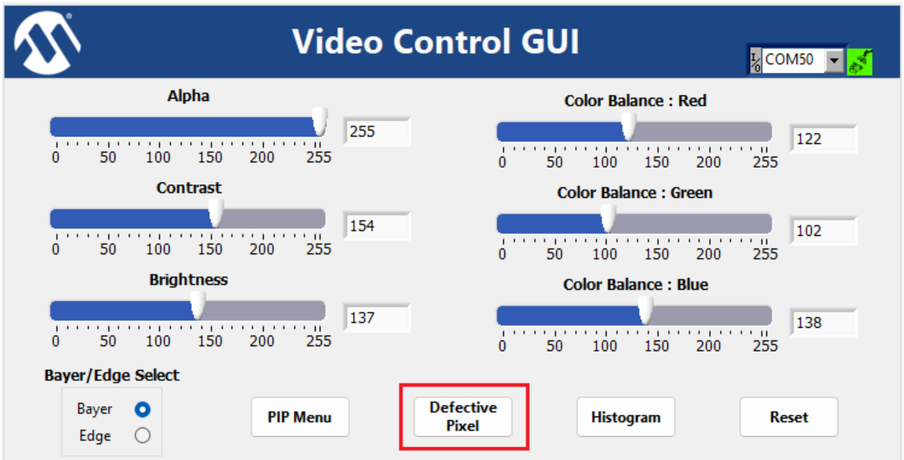
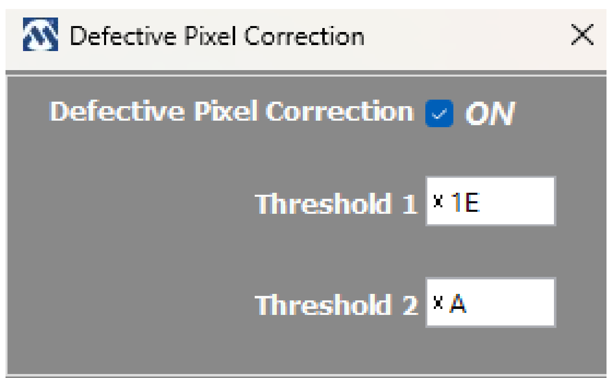
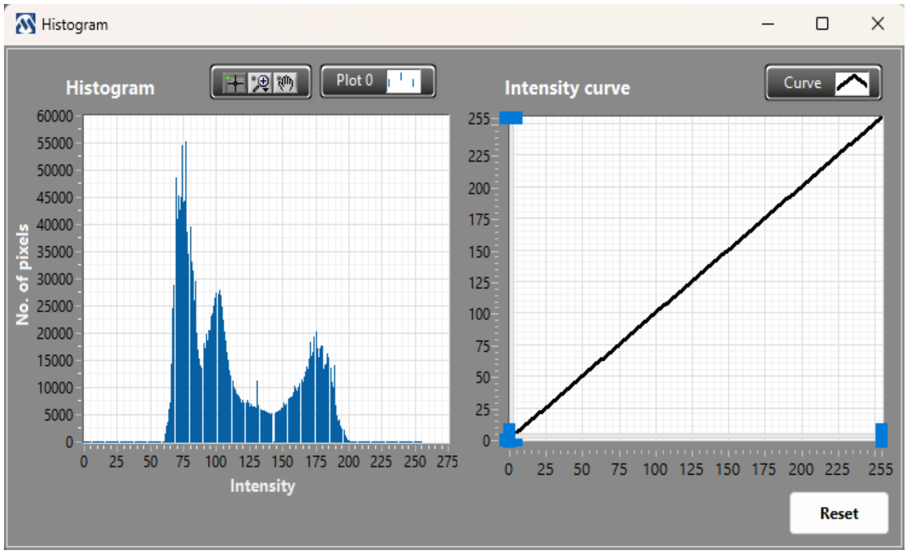


Figure 6-7. Defective Pixel Correction



9. To view the histogram plot of the live video, navigate to the main video control GUI window and select **Histogram** option.
   The following histogram bar graph shows the number of pixels with a particular intensity level. For example, a y-axis value of 500000 at x-axis 100 indicates that there are 500000 pixels with an intensity of 100 (range is 0–255). The Intensity curve on the right side can be used to remap the intensity levels to a new value. The advantage of using intensity curve is that the pixel intensities can be remapped, independently. For example, the pixels below an intensity range of 50 can be modified, independently. The curve can also be used to adjust the black levels of the video frames.

Figure 6-8. Histogram



10. To return to the main GUI, close the **Histogram** window.
11. To exit from the demo, close the GUI.

This concludes the demo.

7. Appendix: Running the Tcl Script (Ask a Question)

Tcl scripts are provided in the www.microchip.com/en-us/application-notes/an4723.

To run Tcl, perform the following steps:

1. Launch the Libero software.
2. From the menu bar, click **Project** > **Execute Script**.
3. In the downloaded directory `mpfs_an4723_v2024p2_df`, locate and select the `script.tcl` file.
4. To execute the selected Tcl script, click **Run**.

After a successful execution of the Tcl script, the Libero project is created within the top directory of `mpfs_an4723_v2024p2_df`. You can verify the process by reviewing the log file, see `mpf_an4723_v2024p2_df_log`.

For more details about the folder structure and details of the Tcl scripts and commands, see the `TCL_Scripts_readme.txt` file and the Tcl Commands Reference Guide. Contact Technical Support team, for any queries about running the Tcl script.

8. Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
C	04/2025	The following is the list of changes in revision C of the document: • Updated the `.job` filepath and TCL script filepath throughout the document. • Updated Table 1-1 in the Demo Requirements section. • Added Microchip_FPGA_GUI_Pack weblink in the Demo Prerequisites section. • Updated Figure 3-1 in the Design Overview section. • Updated Figure 3-2 in the Hardware Implementation section. • Updated Figure 3-3 in the Clocking Structure section. • Updated Figure 3-4 in the Reset Structure section. • Updated Running the Demo section.
B	03/2023	The following is the list of changes in revision B of the document: • Replaced "SEV kit" with "video kit" throughout the document. • Updated for Libero SoC v2022.3 release.
A	08/2022	Initial Revision

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