

Board Debug Checklist for ZL30151, ZL30169 and ZL3025x Devices

Introduction

This application note provides board debug guidelines to customers using ZL30151, ZL30169, and ZL3025x series devices. It is intended to be used mainly during the lab validation stage of new products but it can also be used as reference to debug issues on existing, mature products.

The application note is based on the assumption that the schematic symbol and the PCB footprint used to implement the design are correct.

Prerequisites

There are different issues that can occur in a design involving ZL30151, ZL30169, and ZL3025x series devices; some are common to all designs and some are specific to a design based on how the timing device is used. Under this section are placed the common tests required to be performed in all cases before performing design specific tests.

Visual Inspection

- Check if the timing device populated on the board is the right part number and has the right orientation (pin 1 location).

Power Supply

- Check the power supply voltage levels. For the pins connected directly, check the voltage on the main 1.8V and 3.3V power supply rails. For the pins supplied through isolated islands check the voltage level on the island to identify any missing or interrupted ferrite bead. The measured voltages should be within the operating range specified in the datasheet.
- Check if the power supply sequencing requirement is met. The 1.8V power supply voltage should not be higher than the 3.3V power supply voltage by more than 0.6V during the power-up/down.

Local Reference

- If the local reference is provided by an oscillator, check the amplitude and the frequency of the signal provided by the oscillator; probe the signal at destination (the input pin of the timing device) to identify any missing or broken source series termination on the oscillator output. The amplitude of the signal should be 3.3V LVCMOS.
- Check if the frequency generated by the crystal or the oscillator populated on the board is correct. (it should be the same frequency used to create the configuration file for the timing device)

- If a crystal is used, check the signal on XA and XB pins using a scope; a clock signal should be present on both pins with higher amplitude on XB. If there is no clock signal on XA and XB pins, the timing device is not configured at all or the crystal is defective. If there is no clock signal on XB and there is small amplitude signal (~0.5V) on XA, the timing device is configured to use an external oscillator.

Reset

- Check if the reset signal is asserted only after both 3.3V and 1.8V supply voltages reach nominal value and its duration is at least 100ns.
- If the timing device is configured by a host processor, check if there is at least 100us delay between the moment when the reset is de-asserted and the moment when the processor starts initializing the timing device.

Test Pin

- Check if the TEST pin is asserted low and is stable at the rising edge of reset.

Design Specific Tests

Configuration from External EEPROM is not Working

- Check if the device populated on the board supports configuration from external EEPROM.
- Check if the external EEPROM is populated on the board, has the right orientation and the right part number.
- Check if IF[1:0]=11 and AC[1:0] are 01, 10 or 11 at the rising edge of reset. Also check if the levels on these pins are stable when sampled by the reset rising edge.
- Check if the external EEPROM used for auto configuration contains the right configuration data.
- If a local host uP/uC is connected to the SPI interface of the timing device, check if it is not driving the bus after reset when the timing device is acting as a bus master downloading its configuration from the external EEPROM. The host processor should take control of the SPI bus only after the configuration of the timing device from external EEPROM is completed.

Configuration from Internal EEPROM is not Working

- Check if the timing device populated on the board has internal EEPROM.
- Check if the internal EEPROM used for auto configuration contains the right configuration data.
- Check if during reset the AC1 and AC0 pins are stable, asserted high/low as required to select the proper configuration section from the EEPROM.

Configuration from a Host Processor is not Working

- Check if during reset the IF1 and IF0 pins are stable, asserted high/low as required to enable the interface mode that is actually implemented in hardware. The interface implemented on the board, SPI or I2C, should match the host interface mode selected during reset.
- If the host interface is I2C, check the presence of the pull-up resistors on SDA and SCL and if these signals meet the DC and AC specifications from the datasheet.
- Check if the I2C address assigned during reset based on the status of AC[1,0] pins is the same with the I2C address used by the software to access the timing device; also check if there are no other devices using this address.
- If the host interface is SPI, check if the signals belonging to this interface meet the DC and AC specification from the datasheet.
- Consider reducing the host interface speed as a way to debug timing violations and signal integrity related issues.

High Jitter on the Outputs

- Review the timing device configuration in order to determine if the high jitter is configuration related. Use the same configuration on an evaluation board and compare the jitter numbers; this should reveal if the jitter is hardware dependent or not. If similar numbers are obtained in both cases review the configuration and optimize it based on recommendations in ZLAN-497 app note: Configuring the ZL30151/ZL30169/ZL3025X for Optimum RMS Jitter Performance.
- Check the pk-pk noise on the oscillator's power supply. Optimize the power supply filtering in order to minimize the level of power supply noise. For debug purpose, consider supplying the oscillator from a clean bench top power supply to identify if the high jitter is caused by the oscillator's power supply noise.
- Check the pk-pk noise on the timing device power supply rails. Optimize the power supply filtering in order to minimize the level of power supply noise.
- Check if the timing device input reference is clean, stable, and meets the input specifications.
- Check if the timing device output signal at the receiver is clean, stable, and meets the receiver input specifications.
- For differential outputs, check if both pos. and neg. signals are toggling at the receiver to identify any missing or interrupted series components.



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