
AT13382: Migrating from SAM L21 variant A to variant B

APPLICATION NOTE

Introduction

This document summarizes the relevant differences when migrating from SAM L21 variant A (SAM L21A) to SAM L21 variant B (SAM L21B).

Variant A devices have only been available as engineering samples and have not been released to production. All devices released to production are variant B devices.

Refer to the SAM L21 datasheet for detailed information on the device. Part naming details can be found in Chapter "Ordering Information" in the datasheet.

Erratas for variant A which are fixed are not discussed in this document, as these are documented in the datasheet.

Characteristics are not discussed in this document.

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1. Changes from SAM L21A to SAM L21B

This chapter describes the functional changes in SAM L21B compared to SAM L21A.

1.1. Non-Volatile Memory Controller (NVMCTRL)

1.1.1. Reset Value of CTRLB.MANW Changed

In SAM L21B the reset value of the Manual Write bit in the Control B register of the NVM peripheral (NVM.CTRLB.MANW) has been changed from 0 to 1. This was done to avoid corrupting system flash. With automatic write, when writing to a bad pointer pointing to flash it was possible to corrupt the flash data. By default this is not possible in SAM L21B.

1.2. Supply Controller (SUPC)

1.2.1. Low-power Configuration for Regulator Added

In SAM L21B there is an added configuration bit to control the regulator during standby mode. The low-power mode Efficiency bit in the VREG register (VREG.LPEFF) can be written to 1 to optimize power consumption during standby if your device is operating in a reduced VCC range (2.5V to 3.6V).

1.3. Power Manager (PM)

1.3.1. STDBYCFG.AVREGSD replaced by STDBYCFG.VREGSMOD

In SAM L21B the former Automatic VREG Switching Disable bit in the Standby Config register (STDBYCFG.AVREGSD) is replaced by the Voltage Regulator Standby Mode bits in the same register (STDBYCFG.VREGSMOD). This allows the user to force use of the low-power regulator in standby when SleepWalking tasks are running. This mode must only be used when SleepWalking peripherals are running on a GCLK with 32kHz source.

1.3.2. PLCFG.PLDIS Added

In SAM L21B a configuration bit for disabling the automatic switching of performance levels is added. The Performance Level Disable bit in the Performance Level Configuration register (PLCFG.PLDIS) can be written to 1 to force the device to run in PL0, reducing the power consumption and the wake-up time from standby sleep mode.

1.4. External 32kHz Crystal Oscillator (XOSC32K)

1.4.1. Internal Load Capacitor Removed

In SAM L21A there was an internal load capacitor equivalent to 7pF in the External 32kHz Crystal Oscillator (XOSC32K). This capacitor has been removed in SAM L21B.

If an external crystal is used in a PCB designed with the SAM L21A, the calculation for external load capacitors needs to be redone, accounting for the removed internal load capacitance.

1.5. RTC

In SAM L21B there is an added configuration bit in the RTC, CTRLA.COUNTSYNC.

COUNTSYNC is used to enable read synchronization of the COUNT/CLOCK register. If this bit is not set the returned value when reading the COUNT/CLOCK register will always return 0. Setting the bit will enable read synchronization, and the current count value will be returned when reading the COUNT/CLOCK register.

This bit was not visible and enabled by default in SAM L21 revision A. In SAM L21 revision B it has a reset value of zero, and thus needs to be written to 1 to get the same behavior as in SAM L21 revision A.

1.6. High-speed Bus Matrix (HMATRIX)

1.6.1. Low Latency Mode Added

In SAM L21B there is a new configuration option in the HMATRIX to make a choice between low latency/high performance connection to a peripheral bus or a higher latency connection with a lower power consumption. Refer to Chapter "Features" in the SAM L21 datasheet for details on use of this feature. The default reset value gives the higher latency/lower power option, which is the same behavior as in SAM L21A.

2. Pinout Changes

In variant B of the SAM L21 there has been changes done in the 32- and 48-pin packages relating to the number and placement of the Peripheral Touch Controller (PTC) Y lines. The 32-pin packages have a reduced number of Y lines from 10 down to 7, and the 48-pin package has been reduced from 12 to 10 Y lines. In addition the Y2, Y3, and Y14 has been moved on all packages. In addition OPAMP pins OA_OUT[1] and OA_NEG[2] has swapped position.

Table 2-1. PTC pinout changes

PTC Y Line	Variant A pin	Variant B pin	SAML21E (32-pin)	SAML21G (48-pin)	SAML21J (64-pin)
Y[0]	PA02	PA02			
Y[1]	PA03	PA03			
Y[2]	PA04	PB10	removed		
Y[3]	PA05	PB11	removed		
Y[4]	PA06	PA06			
Y[5]	PA07	PB12	removed	removed	
Y[6]	PA08	PA08			
Y[7]	PA09	PA09			
Y[8]	PA10	PA10			
Y[9]	PA11	PA11			
Y[10]	PB04	PB04			
Y[11]	PB05	PB05			
Y[12]	PB06	PB06			
Y[13]	PB07	PB07			
Y[14]	PB08	PB13		removed	
Y[15]	PB09	PB09			

Bold pins in the variant B column have changed positions from variant A to variant B. Pins marked as removed were available in variant A but are no longer available in variant B.

Table 2-2. OPAMP pinout changes

PIN	Variant A OPAMP pinout	Variant B OPAMP pinout
PB06	OA_NEG[2]	OA_OUT[1]
PB08	OA_OUT[1]	OA_NEG[2]

3. Revision History

Doc. Rev.	Date	Comments
42512B	03/2016	RTC chapter added. OPAMP pinout changes to pinout changes chapter added.
42512A	08/2015	Initial document release.



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