
Migrating from ATmega48A/88A/168A to ATmega48PB/ 88PB/168PB

Features

The ATmega48PB/88PB/168PB introduces several new features:

- picoPower® features
- Four extra GPIO pins
 - One pair of GND and VCC removed and replaced with two extra GPIO pins
 - Two pins that previously only had ADC input channels are now multiplexed with GPIO
- USART Start Frame Detection available in all sleep modes
- Analog Comparator output to pin added
- Serial number (Unique Device ID) added

Introduction

This application note acts as a guide to help users of ATmega48A/88A/168A migrating to the newer ATmega48PB/88PB/168PB.

ATmega48PB/88PB/168PB is functionally compatible with ATmega48A/88A/168A. This document will describe how to update the toolchain, developer tools, and IDE.

Always check the latest revision of the corresponding data sheet for the latest and correct characteristics and device details. It is recommended to review the Errata list.

The latest data sheets can be found here:

- ATmega48A/88A/168A - <http://www.microchip.com/wwwproducts/en/ATmega168a>
- ATmega48PB/88PB/168PB - <http://www.microchip.com/wwwproducts/en/ATmega168pb>

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1. Hardware Design Compatibility

1.1 Package Types

ATmega48PB/88PB/168PB can function as a drop-in replacement for the 32-pin TQFP package, and the 32-pin VFQFN with the 32-pin MLF package, but there are conditions to follow. See chapter [Added/Modified Pin Functionality](#). For other package types, expect to change the PCB layout when migrating from ATmega48A/88A/168A to ATmega48PB/88PB/168PB. The data sheet includes dimensions and physical drawings of the footprint for each device under "Packaging Information". Below are the different package types compared to the different devices.

ATmega48A/88A/168A is available in the following package types:

- 32-pin TQFP
- 32-pin MLF
- 32-pin UFBGA
- 28-pin VQFN
- 28-pin PDIP

ATmega48PB/88PB/168PB is available in two package types:

- 32-pin TQFP
- 32-pin VFQFN

1.2 Added/Modified Pin Functionality

There are two package types that are compatible with ATmega48A/88A/168A and ATmega48PB/88PB/168PB. This section will compare the pin-out of the TQFP package type. For the other compatible package type, MLF/VFQFN, refer to the data sheet chapters "Ordering Information" and "Packaging Information".

ATmega48PB/88PB/168PB introduces four additional GPIO pins; PORTE [3:0]. The different pins are described in [Table 1-1](#) and the pin-out for each device are shown in [Figure 1-1](#) and [Figure 1-2](#).

The 32-pin MLF/VQFN pin-out can be found in the Pin Configurations section in the ATmega48PB/88PB/168PB data sheet.

Figure 1-1. ATmega48A/88A/168A - 32-Pin TQFP

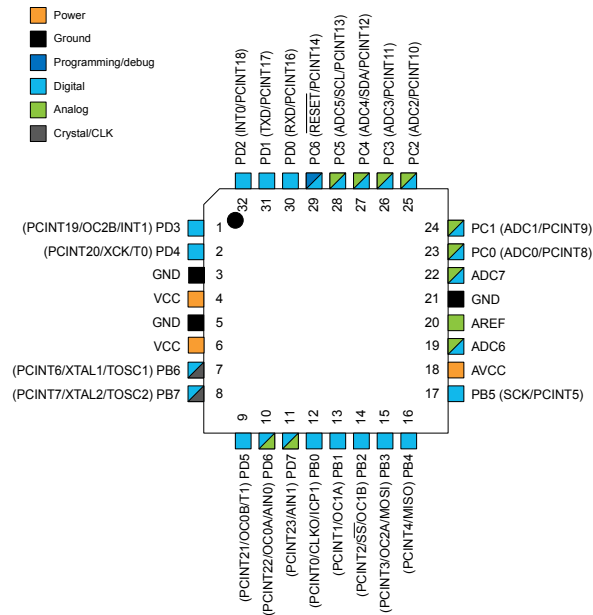
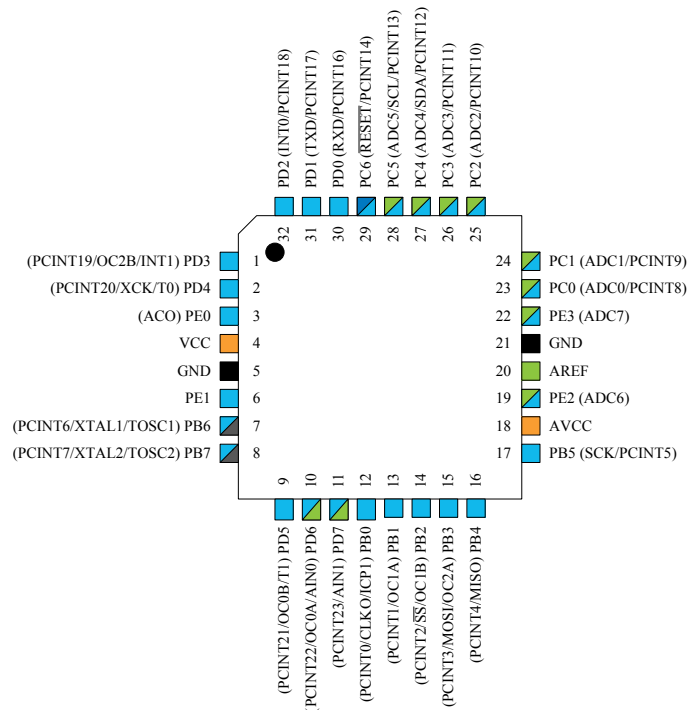


Figure 1-2. ATmega48PB/88PB/168PB - 32-Pin TQFP



GPIO pins PE2 and PE3 are added to Pin19 and Pin22. PE2 and PE3 are multiplexed with ADC6 and ADC7.

Pin3 (GND) and Pin6 (VCC) are replaced by PE0 and PE1 respectively. PE0 is multiplexed with ACO.

Table 1-1. Pin Functionality Difference

32-Pin TQFP Package	ATmega48A/88A/168A	ATmega48PB/88PB/168PB
Pin3	GND	PE0/ACO
Pin6	VCC	PE1
Pin19	ADC6	ADC6/PE2
Pin22	ADC7	ADC7/PE3



To use the ATmega48PB/88PB/168PB device as a drop-in replacement for the ATmega48A/88A/168A the following conditions must meet:

- Pin 3 - If connected to GND, the pin must not be actively driven or ACO must not be enabled.
- Pin 6 - If connected to VCC, the pin must not be actively driven.

1.3 Alternate Pin Configuration

The alternate pin configurations are:

- **ADC7– Port E, Bit 3**
PE3 can also be used as ADC input channel 7. ADC input channel 7 uses analog power AVCC.
- **ADC6 – Port E, Bit 2**
PE2 can also be used as ADC input channel 6. ADC input channel 6 uses analog power AVCC.
- **None – Port E, Bit 1**
No alternate function.
- **ACO – Port E, Bit 0**
ACO Analog Compare Output pin is multiplexed with PE0.

2. Code Compatibility

ATmega48A/88A/168A is code compatible with ATmega48PB/88PB/168PB.

To ensure that code designed for ATmega48A/88A/168A executes on the ATmega48PB/88PB/168PB the user must remember to change the device and recompile the code.

A general rule of thumb is that reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2.1 Writing Reserved Registers

If code should by accident write to a reserved register, Microchip can not guarantee the behavior of the application.

This chapter describes what to be aware of when using code designed for the ATmega48A/88A/168A on the ATmega48PB/88PB/168PB. If by mistake, the code accesses reserved registers or bit locations, the previous device might still operate as expected. On the newer devices these registers or bits might have specific functions, hence unexpected behavior can be observed.

On the ATmega48A/88A/168A register location 0x4F is reserved as shown in figure [Figure 2-1](#).

Figure 2-1. Extract From the ATmega48A/88A/168A Data Sheet

0x4E	SPDR0	7:0	SPID[7:0]							
0x4F	Reserved									
0x50	ACSR	7:0	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0

On the ATmega48PB/88PB/168PB register location 0x4F is the ACSR0 register. This register contains one bit that controls the analog comparator output to Pin 3, ACOE - Analog Comparator Output Enable, as shown in figure [Figure 2-2](#).

Figure 2-2. Extract From the ATmega48PB/88PB/168PB Data Sheet

0x4E	SPDR	7:0	SPID[7:0]							
0x4F	ACSR0	7:0								ACOE
0x50	ACSR	7:0	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS [1:0]	

If the ACO is enabled by accident, and ATmega48PB/88PB/168PB is used as a drop-in replacement for ATmega48A/88A/168A, the ACO can potentially try to drive a pin which is connected to GND, and this can lead to unexpected behavior.

2.2 Device Part Pack

To ensure full device support for ATmega48PB/88PB/168PB the latest part pack must be installed. Up-to-date part packs are included in the latest version of Atmel Studio 7.0, or can be manually downloaded if needed:

- In the Atmel Studio 7.0 toolbar, click *Tools -> Device Pack Manager*. In the Device Pack Manager window click and select the latest version under *ATmega_DFP*, then click Install -> Install Selected Packs.
- [Alternative] Go to <http://packs.download.atmel.com/> and download the latest *Atmel ATmega Series Device Support*. Install the downloaded file.

3. Ecosystem

The ecosystem for AVR[®] products includes Atmel Studio 7 Integrated Development Environment, Toolchains for AVR, Programmers, Debuggers, and Starter Kits.

3.1 Integrated Development Environment

3.1.1 Atmel Studio 7

ATmega48PB/88PB/168PB is supported in the latest version of Atmel Studio 7 - a Free IDE for development of C/C++ and assembler code for Atmel microcontrollers.

Studio 4 does not support ATmega48PB/88PB/168PB.

Go to <http://www.microchip.com/development-tools/atmel-studio-7> for the latest installer and user guide, and other relevant information.

3.1.2 IAR

ATmega48PB/88PB/168PB is supported in IAR Embedded Workbench[®] for Atmel AVR[®] - a commercial C/C++ compiler that is available for 8-bit AVR. Users of IAR[™] must ensure their current installed version supports ATmega48PB/88PB/168PB.

There is a 30-day evaluation version as well as a 4 KB code size limited kick-start version available from their website: <https://www.iar.com/iar-embedded-workbench/partners/atmel/>

3.2 Development Tools

The following developer tool is recommended for ATmega48PB/88PB/168PB:

- Atmel-ICE

Other legacy tools that also support ATmega48PB/88PB/168PB:

- AVR Dragon
- AVR One!
- AVRISP mkII
- JTAGICE mkII
- JTAGICE3
- Power Debugger
- QT600
- STK500
- STK600
- Simulator
- mEDBG

To update the desired tool in Atmel Studio 7: Click Tools → Device Programming in the Atmel Studio 7 Toolbar. When device programming has opened, choose the desired tool, device and interface, and then click Apply. If the tool has an older firmware version, Atmel Studio will prompt you to update the tool firmware version.

Another method: In the Atmel Studio toolbar, click View → Available Atmel Tools. In the Available Atmel Tools window right-click on your Tool and choose Upgrade... in the drop-down menu.

4. New Features

This chapter summarizes the enhancements or added features in ATmega48PB/88PB/168PB compared with ATmega48A/88A/168A.

- USART Start Frame Detection is available in all sleep modes
- Analog Comparator output is available on a pin. (This pin is multiplexed with PE0.)
- Serial Number (Unique Device ID)
- picoPower

4.1 USART

The USART Start Frame Detector can wake up ATmega48PB/88PB/168PB from all sleep modes when it detects a start bit.

When a high-to-low transition is detected on RxDn, the internal 8 MHz oscillator is powered up and the USART clock is enabled. After start-up, the rest of the data frame can be received, provided that the baud rate is slow enough in relation to the internal 8 MHz oscillator start-up time. Start-up time of the internal 8 MHz oscillator varies with supply voltage and temperature.

The USART start frame detection works in both asynchronous and synchronous modes. It is enabled by writing the Start Frame Detection Enable bit (SFDE). If the USART Start Interrupt Enable (RXSIE) bit is set, the USART Receive Start Interrupt is generated immediately when start is detected.

When using the feature without start interrupt, the start detection logic activates the internal 8 MHz oscillator and the USART clock while the frame is being received, only. Other clocks remain stopped until the Receive Complete Interrupt wakes up the MCU.

The maximum baud rate in synchronous mode depends on the sleep mode the device is woken up from:

- Idle sleep mode: system clock frequency divided by four
- Standby or Power-down: 500 kbps

The maximum baud rate in asynchronous mode depends on the sleep mode the device is woken up from:

- Idle sleep mode: the same as in active mode

Table 4-1. Maximum Total Baud Rate Error in Normal Speed Mode

Baud Rate	Frame Size					
	5	6	7	8	9	10
0 - 28.8 kbps	+6.67 -5.88	+5.79 -5.08	+5.11 -4.48	+4.58 -4.00	+4.14 -3.61	+3.78 -3.30
38.4 kbps	+6.63 -5.88	+5.75 -5.08	+5.08 -4.48	+4.55 -4.00	+4.12 -3.61	+3.76 -3.30
57.6 kbps	+6.10 -5.88	+5.30 -5.08	+4.69 -4.48	+4.20 -4.00	+3.80 -3.61	+3.47 -3.30

Baud Rate	Frame Size					
	5	6	7	8	9	10
76.8 kbps	+5.59	+4.85	+4.29	+3.85	+3.48	+3.18
	-5.88	-5.08	-4.48	-4.00	-3.61	-3.30
115.2 kbps	+4.57	+3.97	+3.51	+3.15	+2.86	+2.61
	-5.88	-5.08	-4.48	-4.00	-3.61	-3.30

Table 4-2. Maximum Total Baud Rate Error in Double Speed Mode

Baud Rate	Frame Size					
	5	6	7	8	9	10
0 - 57.6 kbps	+5.66	+4.92	+4.35	+3.90	+3.53	+3.23
	-4.00	-3.45	-3.03	-2.70	-2.44	-2.22
76.8 kbps	+5.59	+4.85	+4.29	+3.85	+3.48	+3.18
	-4.00	-3.45	-3.03	-2.70	-2.44	-2.22
115.2 kbps	+4.57	+3.97	+3.51	+3.15	+2.86	+2.61
	-4.00	-3.45	-3.03	-2.70	-2.44	-2.22

4.2 Analog Comparator

The Analog Comparator Output (ACO) can be connected to PE0 if the Analog Comparator Output Enable (ACOE) is written with "1" in the Analog Comparator Control and Status Register C (ACSR0).

4.3 Serial Number

Each ATmega48PB/88PB/168PB has an integrated serial number (also called unique device ID) that can be used to uniquely identify each part.

There are two approaches to get the serial number information.

One way is to read the Signature Row from software. For detailed information, refer to section "Reading the Signature Row from Software" in the latest data sheet.

Table 4-3. Signature Row Addressing

Signature Byte	Z-Pointer Address
Device Signature Byte 1	0x0000
Device Signature Byte 2	0x0002
Device Signature Byte 3	0x0004
RC Oscillator Calibration Byte	0x0001
Serial Number Byte 1	0x000E
Serial Number Byte 0	0x000F
Serial Number Byte 3	0x0010

Signature Byte	Z-Pointer Address
Serial Number Byte 2	0x0011
Serial Number Byte 5	0x0012
Serial Number Byte 4	0x0013
Serial Number Byte 6	0x0015
Serial Number Byte 7	0x0016
Serial Number Byte 8	0x0017

Note:

If the serial number feature is used across several device families the device signature bytes should also be included in the serial number. Extending the serial number to a 12-byte number.

Another way is to read I/O address 0xF0 - 0xF8, as the ATmega48PB/88PB/168PB serial number can be accessed through I/O registers SNOBRx. The serial number is made from concatenating the nine bytes read out from these read-only registers. See sub-chapter [SNOBRx - Serial Number Byte 8 to 0](#) for more detail.

An example of how to read out the serial number is given below:

C Code Example

```
uint8_t serial_num[9] = {0};

for(uint8_t i = 0; i < 9; i++){
    serial_num[i] = *((uint8_t *) &DEVID0+i);
}
```

4.3.1 SNOBRx - Serial Number Byte 8 to 0

	7	6	5	4	3	2	1	0	
(0xF8)	Serial Number Byte 5								SNOBR5
(0xF7)	Serial Number Byte 4								SNOBR4
(0xF6)	Serial Number Byte 3								SNOBR3
(0xF5)	Serial Number Byte 2								SNOBR2
(0xF4)	Serial Number Byte 1								SNOBR1
(0xF3)	Serial Number Byte 0								SNOBR0
(0xF2)	Serial Number Byte 6								SNOBR6
(0xF1)	Serial Number Byte 7								SNOBR7
(0xF0)	Serial Number Byte 8								SNOBR8
Read/Write	R	R	R	R	R	R	R	R	
Initial Value									Serial Number Byte Value

4.4 picoPower/Power Management and Sleep Modes

The essence of an AVR[®] picoPower device goes beyond merely the various picoPower features included. The design methodology, the process geometry, and even the types of transistors used are all essential power-saving parts of a picoPower device. All picoPower devices are designed from the ground up for low power consumption utilizing AVR's proprietary low leakage processes and libraries to provide industry leading low power consumption in active and all sleep modes.

The white paper "[Innovative Techniques for Extremely Low Power Consumption with 8-bit Microcontrollers](#)" and the application note "[AVR4013-picoPower Basics](#)" give a more in-depth look at the picoPower features.

4.4.1 BOD Disable

When the Brown-out Detector (BOD) is enabled by BODLEVEL fuses, the BOD is actively monitoring the power supply voltage during a sleep period. To save power, it is possible to disable the BOD by use of software for some of the sleep modes. The sleep mode power consumption will then be at the same level as when BOD is globally disabled by fuses. If BOD is disabled in software, the BOD function is turned off immediately after entering the sleep mode. Upon wake-up from sleep, BOD is automatically enabled again. This ensures safe operation in case the V_{CC} level has dropped during the sleep period.

When the BOD has been disabled, the wake-up time from sleep mode will be approximately 60 μ s to ensure that the BOD is working correctly before the MCU continues executing code.

BOD disable is controlled by the BOD Sleep bit in the MCU Control Register (MCUCR.BODS). Writing this bit to '1' turns off the BOD in relevant sleep modes, while a zero in this bit keeps BOD active. The default setting, BODS=0, keeps BOD active.

Note: Writing to the BODS bit is controlled by a timed sequence and an enable bit.

5. Updated Features

5.1 Signature Bytes

All AVR microcontrollers have a three-byte signature code, which identifies the device. This code can be read in both serial and parallel mode, also when the device is locked. The three bytes reside in a separate address space. For the device signature bytes, there are differences between ATmega48A/88A/168A and ATmega48PB/88PB/168PB, see the table below for more detail.

Table 5-1. Device ID

Part	Signature Bytes Address		
	0x000	0x001	0x002
ATmega48A	0x1E	0x92	0x05
ATmega48PB	0x1E	0x92	0x10
ATmega88A	0x1E	0x93	0x0A
ATmega88PB	0x1E	0x93	0x16
ATmega168A	0x1E	0x94	0x06
ATmega168PB	0x1E	0x94	0x15

5.2 Full Swing Oscillator

The ATmega48A/88A/168A device includes a full swing crystal oscillator as a clock source option, which can be selected by configuring the flash fuse. In the new ATmega48PB/88PB/168PB, the full swing crystal oscillator is removed. Refer to the "Clock Sources" chapter in the device data sheet.

Table 5-2. Full Swing Oscillator Removed from ATmega48PB/88PB/168PB

Device Function	ATmega48A/88A/168A	ATmega48PB/88PB/168PB
Full swing crystal oscillator	Yes	No

5.3 Characteristics

This chapter will compare the biggest changes in electrical- and typical characteristics. For the most up-to-date- and other numbers refer to the latest data sheet of the device.

The latest data sheets can be found here:

- ATmega48PB/88PB/168PB - <http://www.microchip.com/wwwproducts/en/ATmega168pb>
- ATmega48A/88A/168A - <http://www.microchip.com/wwwproducts/en/ATmega168a>

Table 5-3. Typical Wait Delay Before Writing the Next Flash or EEPROM Location

Symbol	ATmega48A/88A/168A	ATmega48PB/88PB/168PB	Units
t _{WD_FLASH}	4.5	2.6	ms
t _{WD_EEPROM}	3.6	3.6	ms

Symbol	ATmega48A/88A/168A	ATmega48PB/88PB/168PB	Units
t_{WD_ERASE}	9.0	10.5	ms
t_{WD_FUSE}	-	4.5	ms

6. Additional reading and related documents

- [AVR095: Migrating between ATmega48, ATmega88 and ATmega168](#)
- [AVR512: Migration from ATmega48/88/168 to ATmega48P/88P/168P](#)
- [AVR528: Migrating from ATmega48P/88P/168P to ATmega48PA/88P/168PA](#)
- [AVR532: Migrating from ATmega48/88/168 to ATmega48A/88A/168A](#)
- [AN2519: AVR Microcontroller Hardware Design Considerations](#)
- [AT12615: Getting Started with ATmega48PB/88PB/ 168PB](#)
- [AVR040: EMC Design Considerations](#)
- [AVR053: Calibration of the internal RC oscillator](#)
- [AVR140: ATmega48/88/168 family run-time calibration of the Internal RC oscillator for LIN applications](#)
- [AVR910: In-System Programming](#)
- [AVR4013: picoPower Basics](#)
- [AVR4100: Selecting and testing 32kHz crystal oscillators for AVR microcontrollers](#)
- [AVR42787: AVR Software User Guide](#)

Additional documents can be found here: <http://www.microchip.com/wwwproducts/en/ATmega168pb>

Or our webpage at www.microchip.com

7. Revision History

Doc. Rev.	Date	Comments
A	12/2017	Initial document release

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