

## Introduction

Author: Mihai Alexandru Ricanu, Microchip Technology Inc.

The Analog to Digital Converter (ADC) is an indispensable peripheral in analog data collection and processing applications such as sensor nodes, board voltages and currents monitoring, functional safety, layered conditional triggering, and notification. A wide range of applications make use of ADC peripherals. However - if a small signal measurement is required, additional input signal conditioning is necessary, especially in noisy environments. The usage of external filters and amplifiers is usually required to make the sensor output suitable for ADC processing. However, this approach increases the Bill of Materials (BOM) and the total solution cost. The AVR® EB family of microcontrollers (MCUs) has two specific ADC hardware enhancements that intent to solve or alleviate these issues: the internal Programmable Gain Amplifier (PGA) with up to 16x gain and the Burst Accumulation mode with up to 1024 consecutive measurements mean.

The main advantage of the internal PGA over dedicated operational amplifier peripherals on other devices is the input multiplexing. Although these dedicated peripherals feature user-defined feedback and allow for higher gain, they require additional external circuitry, and the limited number of dedicated amplification pins greatly reduces the range of possible applications. The ADC peripheral on the AVR EB features an internal PGA that is available for all ADC channels (24 I/O pins for the AVR16EB32), allowing for a wide range of applications.

By implementing an accumulation and averaging process, the measured signal accuracy improves. This is especially useful if the ADC operates in noisy environments. This method is equivalent to a low-pass filter and has the advantage of attenuating signal fluctuation or noise. The ADC peripheral on the AVR® EB features a Burst Accumulation mode that performs this process in hardware without core interaction.

This document showcases the hardware enhancements of the 12-bit ADC peripheral on the AVR® EB MCU by developing an application where a low-voltage signal is measured. Specific to such applications, the necessary information is provided by slight voltage variations and is usually greatly affected by noise, as the input signal is in the range of a few millivolts. This is a measurement-limiting environment dominated by 24-bit ADCs, where the usage of a simple 12-bit ADC would be unsuitable. The applications taking advantage of the AVR® EB ADC hardware enhancements should consider low dynamic range signals to allow burst accumulations, such as variations of temperature, weight, humidity, and velocity. To demonstrate these features, a strain gauge load cell is used to develop a weight scale application.

The application uses the MPLAB® Code Configurator (MCC) for initial device and peripherals setup. Also, it has a corresponding web page on the Microchip MPLAB Discover website, providing a comprehensive description of the hardware and software requirements.



[Click to view code examples on MPLAB DISCOVER](#)

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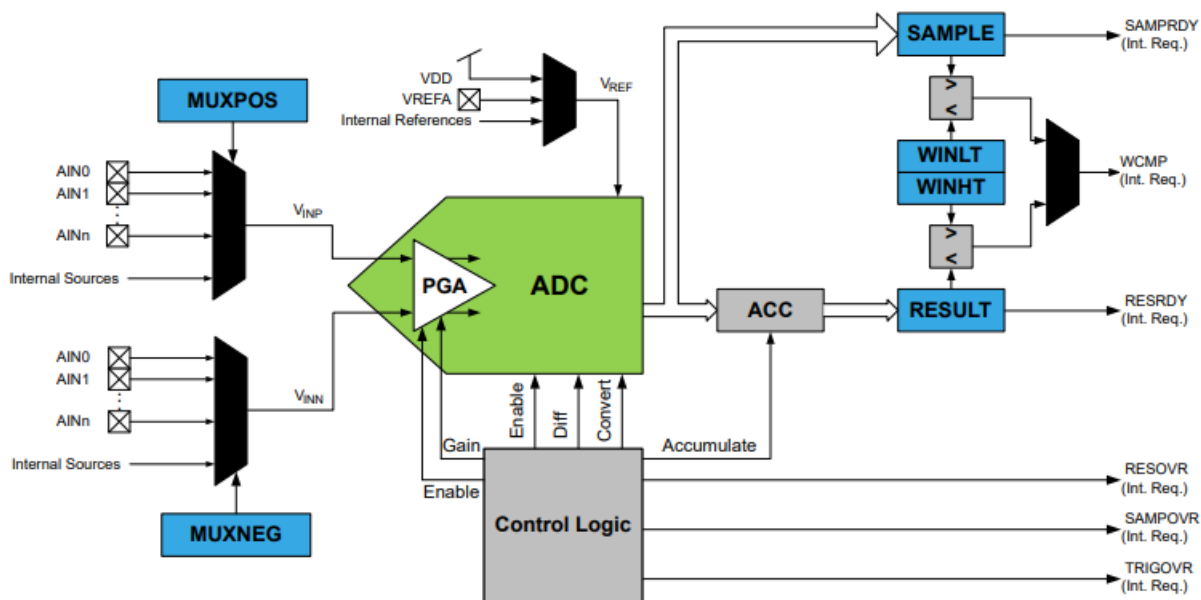
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## 1. Peripheral Overview: Analog-to-Digital Converter with Programmable Gain Amplifier

The ADC peripheral on the AVR EB family of microcontrollers features the following characteristics:

- 12-Bit Resolution
  - Up to 17 bits with oversampling
- Conversion Rate Up to 300 ksps at 12-Bit Resolution
- Up to 24 Inputs
- Differential and Single-Ended Conversion
- Programmable Gain Amplifier from 1x to 16x
- Input Voltage Range from -100 mV to  $V_{DD}+100$  mV
- Multiple Internal ADC Reference Voltages
  - $V_{DD}$
  - 1.024V
  - 2.048V
  - 2.500V
  - 4.096V
- External Reference Input
- Single and Free-Running Conversions
- Series and Burst Accumulation Modes
- Accumulation of Up to 1024 Conversions
- Left or Right Adjusted Result
- Interrupts on Conversion Complete
- Optional Event Triggered Conversion
- Configurable Window Comparator

Figure 1-1. ADC Block Diagram



The ADC supports six different operation modes, with differential and single-ended conversions possible for each mode:

- Single mode – Single conversion per trigger, with 8- or 12-bit conversion output
- Series Accumulation mode – One conversion per trigger, with an accumulation of n samples
- Burst Accumulation mode – A burst of n samples accumulated as fast as possible after a single trigger

In Series and Burst modes, the SAMPNUM bit field in the Control F register controls how many samples to accumulate. This hardware accumulation feature acts as a noise filter, allowing for more accurate sampling of the input signal. The noise reduction comes at the expense of total conversion time, which the application must take into consideration.

An ADC conversion is started by one of the following triggers, depending on the configuration of the START bit field in the Command register:

- Writing the IMMEDIATE value to the START bit field
- Receiving an event input
- Writing to one of the input multiplexer registers

The Result Ready interrupt flag in the Interrupt Flags register shows if a conversion or accumulation has finished. This flag also triggers the corresponding interrupt if enabled in the Interrupt Control register.

In the default configuration, the PGA is disabled, and the input signals are sampled directly into the conversion state without internal amplification. Depending on the input signal properties, it can be desirable to configure the internal PGA stage to amplify the signal. In comparison to external amplifiers, the internal PGA has several desirable properties:

- Small bill of materials
- Low number of pins required
- Firmware selectable gain with input multiplexing for flexible and feature-rich applications
- Non-inverting amplification maintains signs/logic structure in firmware when the application requires to operate with PGA turned on and off

The user must consider the following effects when using the PGA:

- The input signal is amplified with the natural side effects of an additional amplification stage (input noise, offset and gain error) and possible saturation
- The maximum conversion rate is slower because the ADC needs to sample the PGA
- Power consumption is slightly increased
- Depending on the sampling mode, the relative timing of the conversions is altered

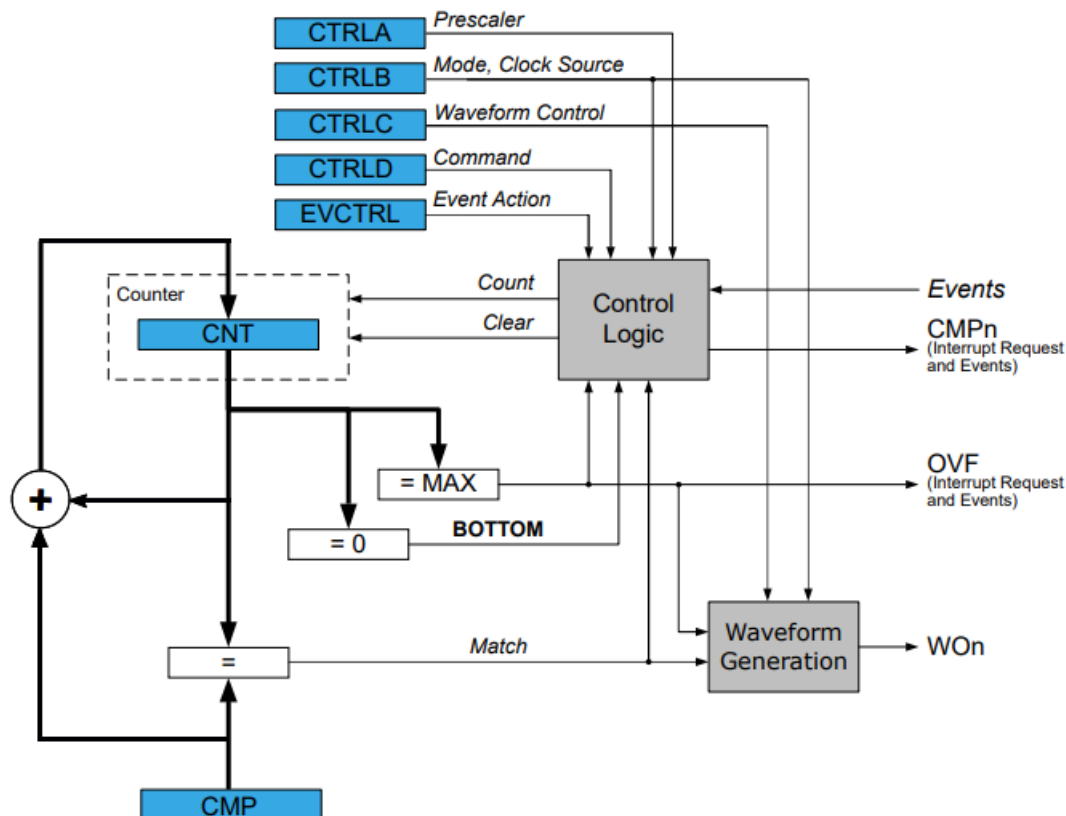
The PGA is enabled by setting the PGAEN bit and configuring the GAIN bit field in the PGA Control register. The VIA bit fields in the Positive and Negative Input Multiplexer registers determine whether the input signal is connected via the PGA or is fed straight to the conversion stage. The VIA bits are shared, so a value written to the VIA bit field in any Input Multiplexer register updates both.

## 2. Peripheral Overview: Timer/Counter Type F

The Timer/Counter type F capabilities include frequency and waveform generation. The TCF consists of a base counter and a control logic, which can be set in different modes, each providing unique functionality. A selectable clock source with optional prescaling clocks the base counter. The TCF features the following characteristics:

- 24-Bit Timer/Counter
- Operation Modes:
  - Frequency Generation
  - Numerically Controlled Oscillator (NCO)
    - Pulse-Frequency
    - Fixed Duty Cycle
  - 8-Bit Pulse-Width-Modulation (PWM)
- 7-Bit Prescaler
- Timer Overflow and Two Compare Match Events/Interrupts
- Event Generation as Pulse or Waveform Output
- Multiple Clock Sources

Figure 2-1. TCF Block Diagram



Depending on the operation mode, the peripheral's registers functionality might be different. In the context of this technical brief, the focus is on the Frequency Waveform Generation mode.

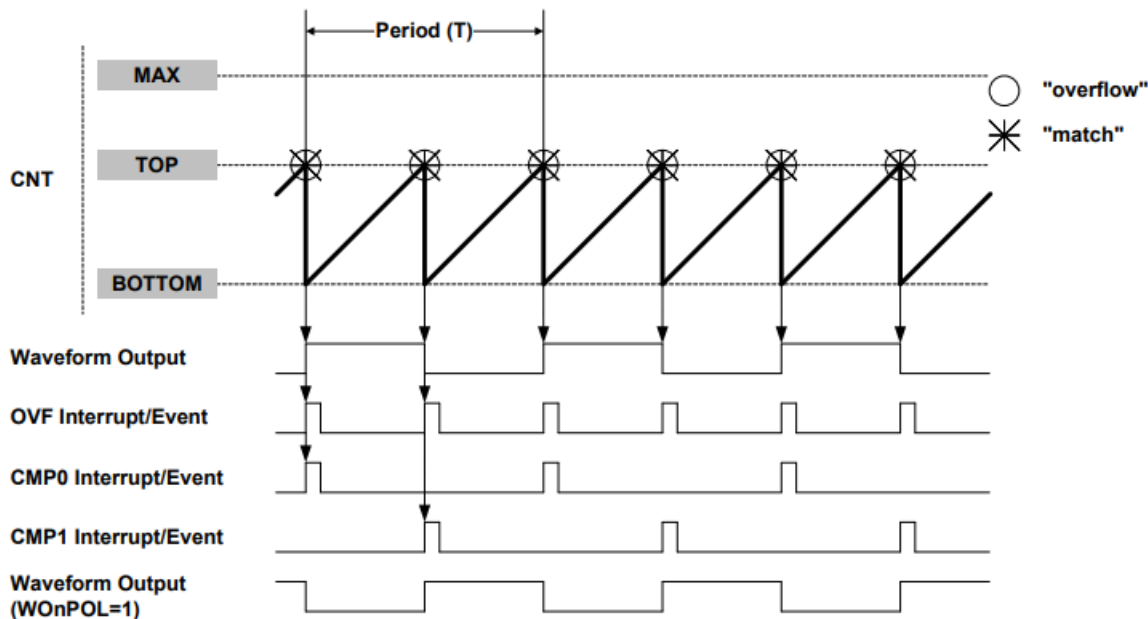
In Frequency Waveform Generation mode, the TCFn.CMP register controls the period time. The corresponding waveform generator output is toggled on each compare match between the TCFn.CNT and TCFn.CMP registers. The following equation defines the waveform frequency:

$$f_{FRQ} = f_{CLK\_TCF} / 2N(CMP+1)$$

where N represents the prescaler divider, and  $f_{CLK\_TCF}$  is the TCF clock frequency.

The OVF interrupt/event is generated on every overflow, while the CMP0 and CMP1 interrupts/events are generated on alternating overflows. When using the Event System, the OVF and CMPn events can be configured to trigger actions in other peripherals, without using the CPU.

**Figure 2-2.** TCF Frequency Waveform Generation

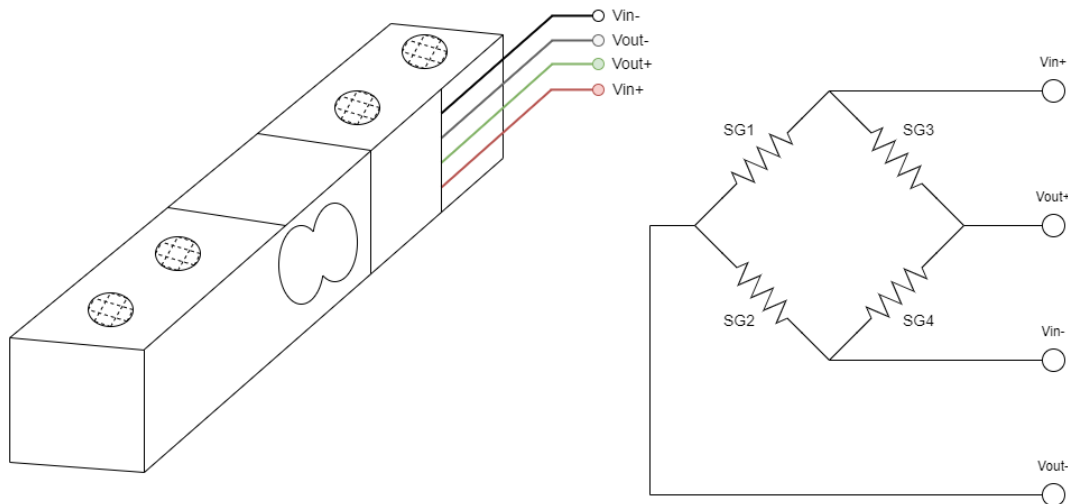


The application developed in the context of this technical brief uses the TCF and the Event System to trigger ADC conversions periodically, without software interaction. The TCF is configured in Frequency Waveform Generation mode, and the period of the generated signal is set to 20 ms, ensuring that a new ADC conversion or burst accumulation is triggered every 10 ms, depending on the operation mode.

### 3. Application Setup

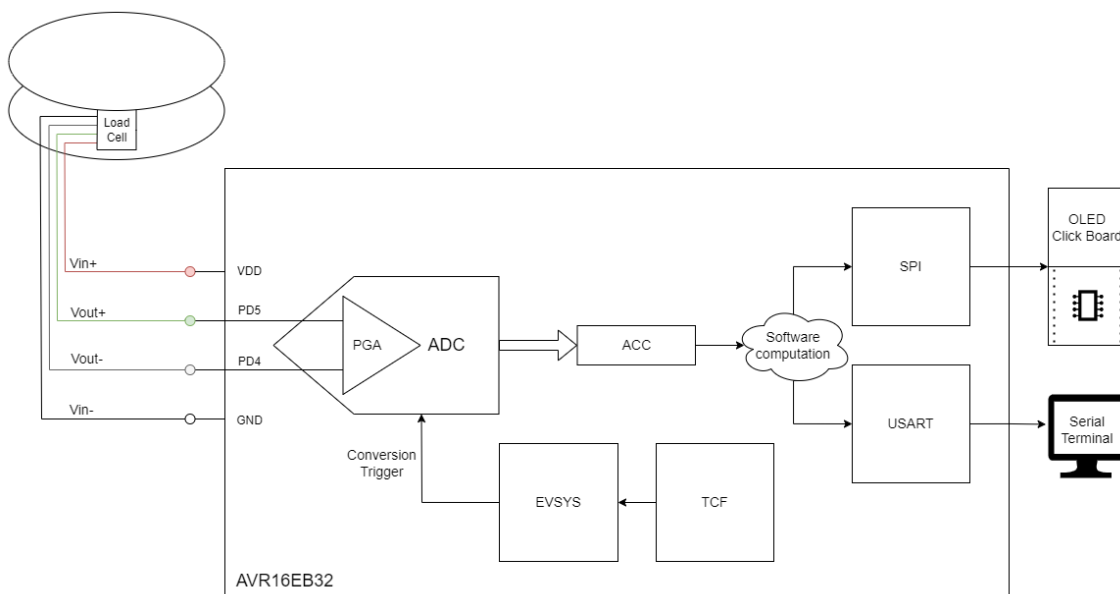
A load cell is an electromechanical sensor used to measure force or weight. Through a mechanical arrangement, the sensed force deforms a strain gauge. The strain gauge measures the deformation as a change in electrical resistance. A load cell usually consists of four strain gauges in a Wheatstone bridge configuration. The electrical signal output is typically in the order of a few millivolts and requires amplification before it can be measured. The load cell is used in various applications, including weight scales.

**Figure 3-1.** Strain Gauge Load Cell and Wheatstone Bridge Configuration



The weight scale application is developed around the AVR16EB32 microcontroller and uses the Event System, the Timer/Counter type F (TCF) and the ADC peripherals to periodically sample the output signal of a strain gauge load cell. The resulting values are converted to weight and displayed on a Mikroe® OLED Click board and in the serial terminal window or the Data Visualizer (DV) interface.

**Figure 3-2.** Weight Scale Block Diagram



## 4. Measurement Results

The output signal of the load cell is sampled using three different configurations to demonstrate the advantages of the PGA and Burst Accumulation mode. A fourth setup combines the hardware capabilities of the ADC with additional software computation to further improve the accuracy of the measured signal.

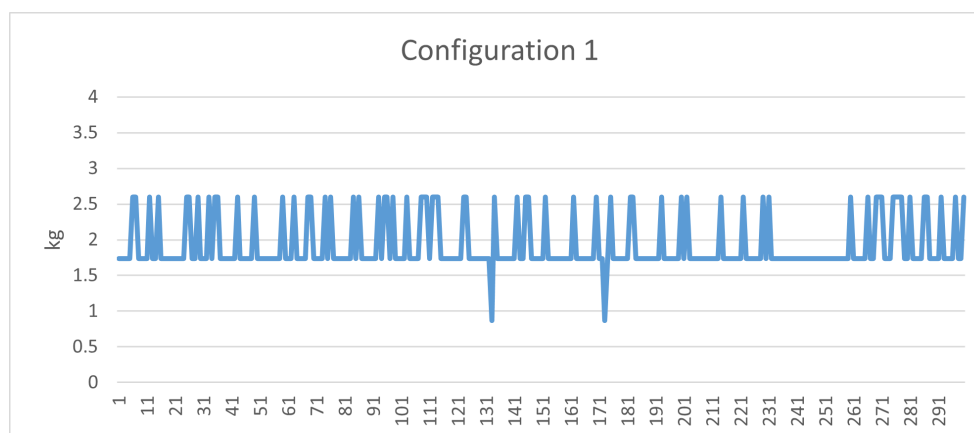
### 4.1 Configuration 1: Single Conversion without PGA Usage

In the first configuration, the ADC operates in Single Conversion mode with the PGA disabled. An object weighing 2.003 kg is placed on the scale, and 300 ADC samples are recorded and analyzed.

**Table 4-1.** Configuration 1 Results

Weight on load cell:	2.003 kg
Maximum weight measured:	2.599 kg
Minimum weight measured:	0.866 kg
Max - Min:	1.733 kg

**Figure 4-1.** Configuration 1 Chart



As observed in the above chart, the input signal is not usable without prior conditioning. According to the load cell's data sheet its capacity and output are rated at 5 kg and 1.0±0.15 mV/V, respectively. The load cell outputs 3.3 mV at maximum capacity when supplied by 3.3V. Performing ADC conversions on signals of this scale without prior amplification proves unsuitable as the LSB voltage is in the range of 0.5 mV when the ADC is operating in differential mode, and the voltage reference is 1.024V. In this case, as the resolution is inappropriate, minor variations of the ADC output translate into considerable changes in the computed weight. It is, therefore, impossible to detect any minor input signal variations. Taking into account these observations, the internal PGA proves instrumental in the development of the weight scale application featured in this document.

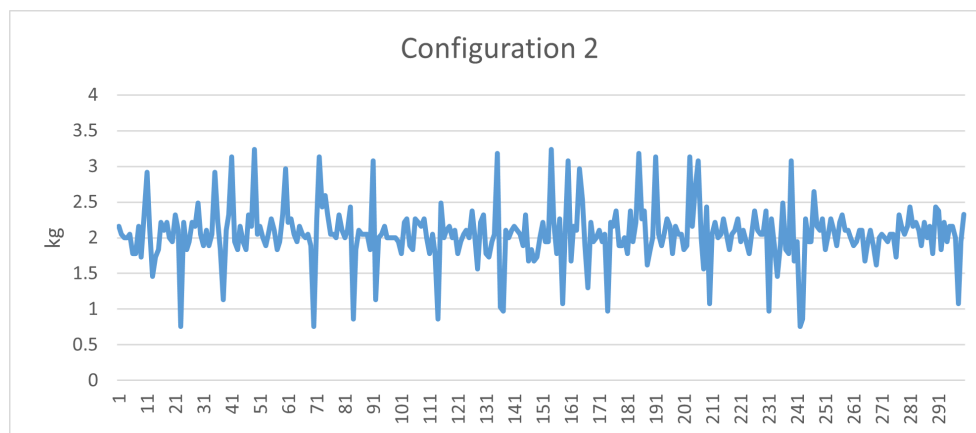
### 4.2 Configuration 2: Single Conversion with 16x Gain

The second configuration features the ADC operating in Single Conversion mode, with the PGA enabled and the gain set to 16x. The same object weighing 2.003 kg is placed on the scale, and 300 ADC samples are recorded and analyzed.

**Table 4-2.** Configuration 2 Results

Weight on load cell:	2.003 kg
Maximum weight measured:	3.238 kg
Minimum weight measured:	0.756 kg
Max - Min:	2.482 kg

Figure 4-2. Configuration 2 Chart



As observed in **Table 4-2**, the weight of the object placed on the scale and the peak-to-peak error determined from the sampled data are in the same order of magnitude. Additional noise filtering is required to obtain an accurate weight measurement. The simplest and most convenient way to achieve this is to accumulate and average multiple ADC samples, which can be done in hardware, by operating the ADC in Burst Accumulation mode or in software by repeatedly accumulating single conversion results. The most notable advantage of the Burst Accumulation mode over software accumulation is the non-blocking aspect of it, as the ADC hardware peripheral performs the accumulation core independently.

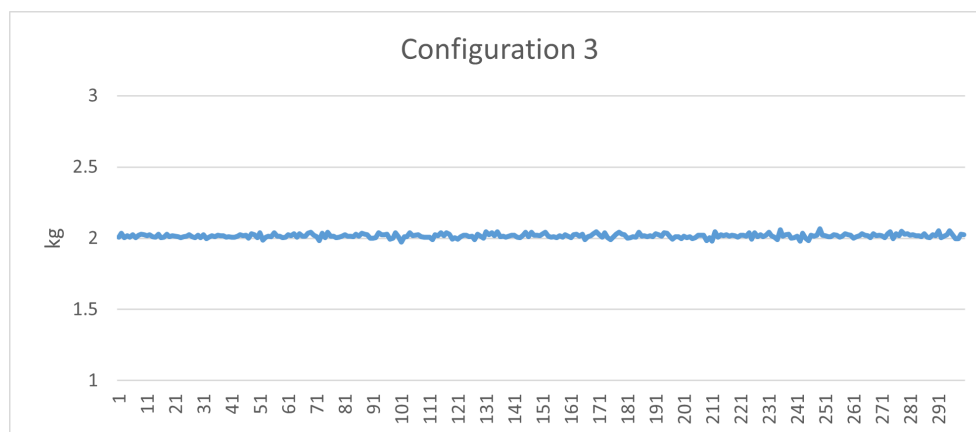
### 4.3 Configuration 3: Burst Conversion with 16x Gain

The third configuration features the ADC operating in Burst Conversion mode with 1024 accumulation samples. The PGA is enabled, and the gain is set to 16x. The same object used in the previous configurations is placed on the scale, and 300 burst conversion results are recorded and analyzed.

Table 4-3. Configuration 3 Results

Weight on load cell:	2.003 kg
Maximum weight measured:	2.065 kg
Minimum weight measured:	1.973 kg
Max - Min:	0.092 kg

Figure 4-3. Configuration 3 Chart



Operating the ADC in Burst Accumulation mode makes a significant improvement in the accuracy of the measurement compared to the second configuration. The hardware accumulation and averaging process improves the noise reduction, as seen in the previous chart. When compared to the Single Conversion mode, the drawback of the Burst Accumulation mode is the longer conversion time, which depends on the configured number of accumulation samples.

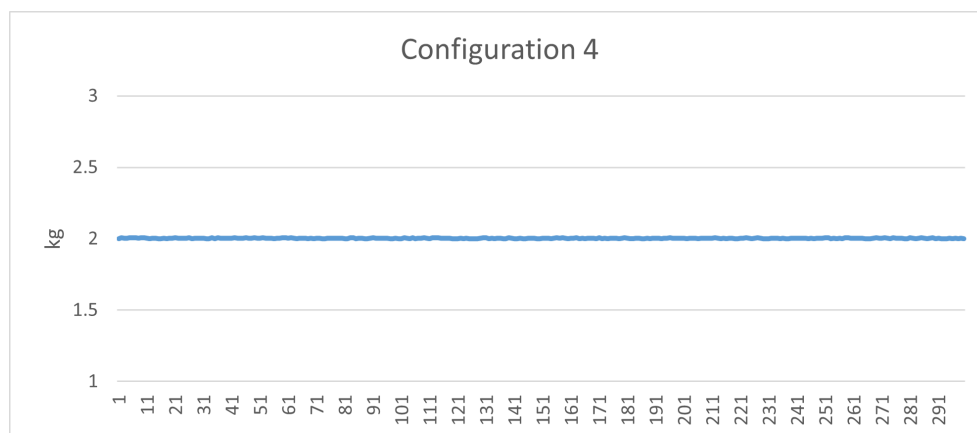
#### 4.4 Configuration 4: Burst Conversion with 16x Gain and Software Accumulation

If the conversion time is not a restraint, in addition to the settings specified for Configuration 3, software accumulation and averaging can be implemented to achieve even greater accuracy. By accumulating 128 burst conversion results in software (each conversion represents the sum of 1024 samples), the following measurements were obtained:

**Table 4-4.** Configuration 4 Results

Weight on load cell:	2.003 kg
Maximum weight measured:	2.007 kg
Minimum weight measured:	2.000 kg
Max - Min:	0.007 kg

**Figure 4-4.** Configuration 4 Chart



Combining the effects of hardware and software accumulation offers impressive results. As a drawback, the additional accuracy comes at the price of considerably long conversion times, as the total number of accumulated samples is equal to the product of the set hardware and software sample numbers. Additionally, the software implemented accumulation is core dependent.

## 5. Demonstration

Pictures of the hardware setup and screenshots of the DV interface were taken for demonstration purposes. For improved measurement accuracy, the weight scale application is running in Configuration 4. Data from Configuration 3 and 4 were plotted in the DV interface to demonstrate the conversion time versus accuracy tradeoff.

Figure 5-1. Configuration 3 - DV Plot

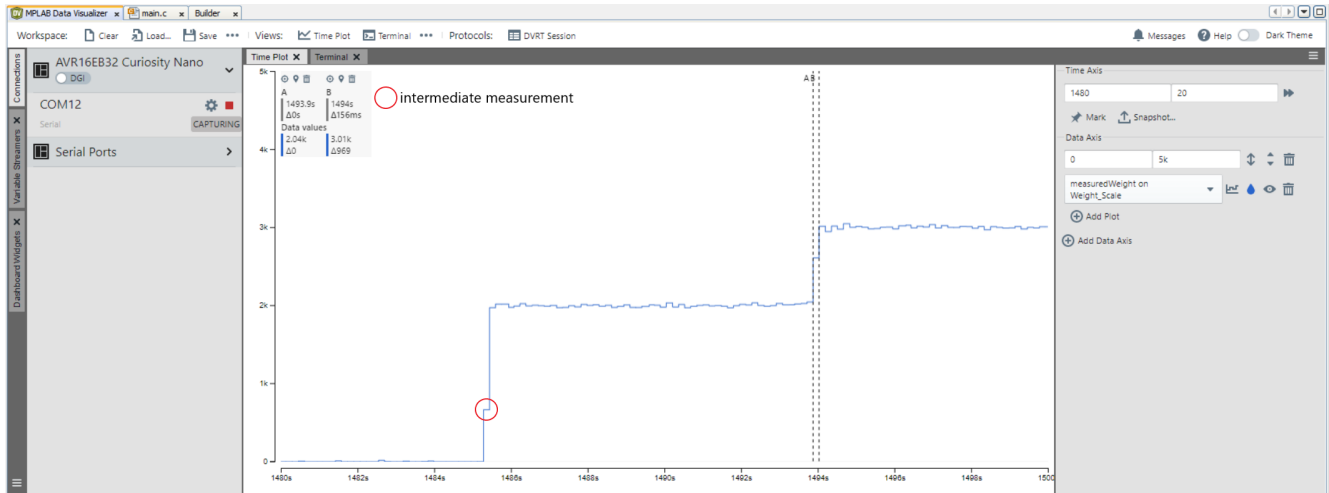
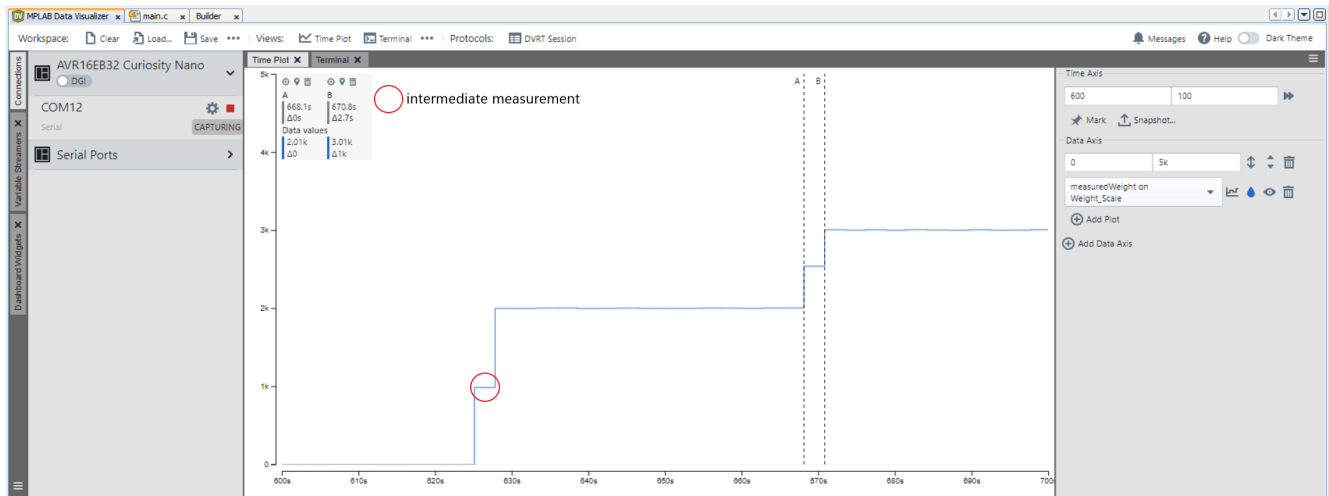


Figure 5-2. Configuration 4 - DV Plot



Two objects (respectively two and one kilogram) are placed on the weight scale. The influence of the additional software accumulation and averaging is clearly noticeable when comparing the plotted results. The accuracy improvement comes at the cost of conversion time. Although more accurate, in Configuration 4, the conversion result is plotted every 2.7 seconds, while in Configuration 3, the result is plotted every 156 ms.

Figure 5-3. Configuration 4 - Demo Setup with 1 kg Object on the Weight Scale



Figure 5-4. Configuration 4 - Measurement Results of the 1 kg Object, Displayed in the DV Serial Terminal Window

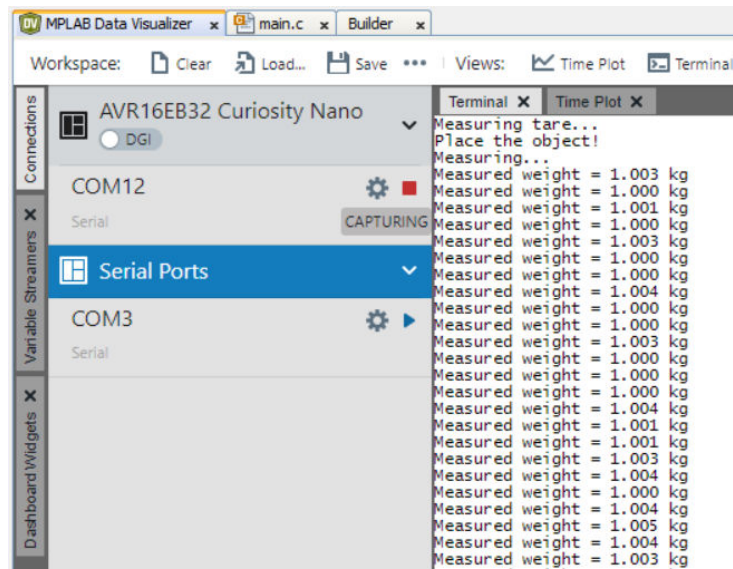
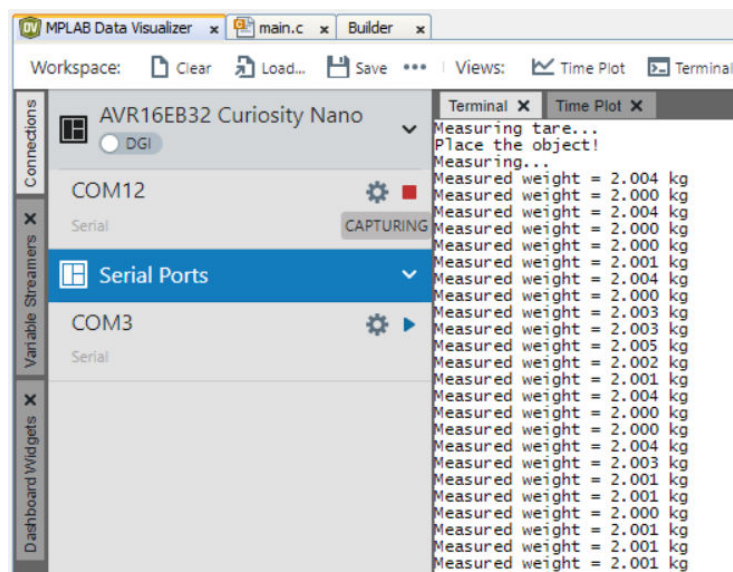


Figure 5-5. Configuration 4 - Demo Setup with 2 kg Object on the Weight Scale



Figure 5-6. Configuration 4 - Measurement Results of the 2 kg Object, Displayed in the DV Serial Terminal Window



## 6. Conclusion

To conclude the analysis performed in this document, the development of the showcased weight scale or similar applications that require low-voltage signal measurement would not be possible without using an amplification stage before sampling. The ADC peripheral with integrated PGA provides an effective and low-cost solution compared to external amplifiers. Among other advantages, the PGA firmware selectable gain and input multiplexing allow for the development of a wide variety of applications, including multiple channels data acquisition systems, as the usually limited number of dedicated amplification pins is no longer a constraint. If additional noise reduction is required, Burst Accumulation mode can be used to improve the accuracy of the measurement.

## 7. References

- *"AVR16EB14/20/28/32 Preliminary Data Sheet"* (DS40002522). Microchip Technology Inc., 2023
- *"AVR16EB32 Curiosity Nano User Guide"* (DS50003605). Microchip Technology Inc., 2023
- *"Curiosity Nano Base for Click boards™ Hardware User Guide"* (DS50002839). Microchip Technology Inc., 2021
- *"MPLAB® Code Configurator v3.xx User's Guide"* (DS40001829). Microchip Technology, Inc., 2018

## 8. Revision History

Document Revision	Date	Comments
A	02/2024	Initial document release

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