High-Speed Analog Comparator Module

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33E/PIC24E devices.

Please consult the note at the beginning of the **"High-Speed Analog Comparator"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

1.0 INTRODUCTION

The High-Speed Analog Comparator module, in Switch Mode Power Supply (SMPS) and digital power conversion devices, provides a way to monitor voltage, current and other signals in a power conversion application. The analog comparator provides the user with the ability to implement Current Mode Control (CMC) in power conversion applications.

The High-Speed Analog Comparator module contains four high-speed analog comparators, each with a dedicated 12-bit Digital-to-Analog Converter (DAC), which provide a programmable reference voltage to the negative input of the comparator.

The High-Speed Analog Comparator module consists of the following key features:

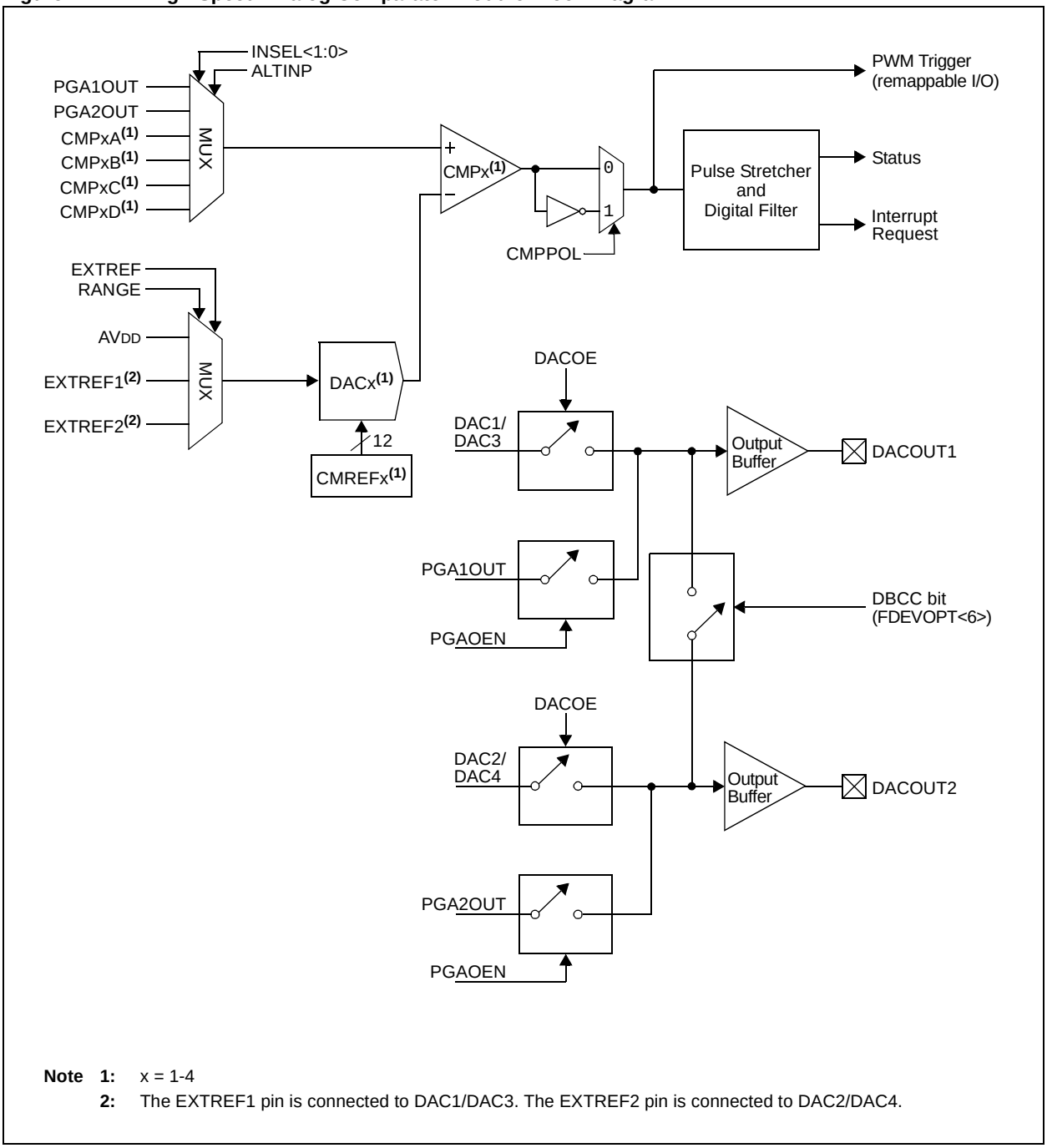
- Four Rail-to-Rail Analog Comparators
- Dedicated 12-Bit DAC for each Analog Comparator
- Up to Six Selectable Input Sources per Comparator:
  - Four external inputs
  - Two internal inputs from PGAx module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Up to Two DAC Outputs to Device Pins
- Multiple Voltage References for the DAC:
  - External references (EXTREF1/EXTREF2)
  - AV_{DD}
- Interrupt Generation Capability
- Functional Support for the High-Speed Pulse-Width Modulation (PWM) module, which includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

2.0 MODULE DESCRIPTION

The SMPS analog comparator module provides high-speed operation with a typical delay of 15 ns. The negative input of the comparator module is connected to the output of the DAC and the positive input is connected to an analog multiplexer that selects the input signal source. The internal block diagram of the High-Speed Analog Comparator module is shown in Figure 2-1.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC module and detect voltage transients with the comparator module.

Figure 2-1: High-Speed Analog Comparator Module Block Diagram



Note 1: x = 1-4

2: The EXTREF1 pin is connected to DAC1/DAC3. The EXTREF2 pin is connected to DAC2/DAC4.

3.0 CONTROL REGISTERS

The following registers are used to configure the High-Speed Analog Comparator module:

- **CMPxCON: Comparator x Control Register**

This register is used to configure the comparator, including voltage reference source, input source select pin and output polarity. There are four individual registers (CMP1CON to CMP4CON), which correspond to the respective comparator.

- **CMPxDAC: Comparator x DAC Control Register**

The contents of this register determine the threshold voltage for the comparator. There are four individual registers (CMP1DAC to CMP4DAC), which correspond to the respective comparator.

Register 3-1: CMPxCON: Comparator x Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CMPON:** Comparator Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CMPSIDL:** Comparator Stop in Idle Mode bit
1 = The comparator clocks will be stopped and the bias current will be disabled; the comparators will not recover from Idle mode
0 = No operational changes for the comparators from normal mode; the comparators will recover from Idle mode
If a device has multiple comparators, any CMPSIDL bit set to ‘1’ will disable all comparators while in Idle mode.

bit 12-11 **HYSSEL<1:0>:** Comparator Hysteresis Select bits
11 = 45 mV hysteresis
10 = 30 mV hysteresis
01 = 15 mV hysteresis
00 = No hysteresis is selected

bit 10 **FLTREN:** Digital Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 9 **FCLKSEL:** Digital Filter and Pulse Stretcher Clock Select bit
1 = Digital filter and pulse stretcher operate with the PWM clock
0 = Digital filter and pulse stretcher operate with the system clock

bit 8 **DACOE:** DAC Output Enable bit(1)
1 = DAC analog voltage is connected to the DACOUTx pin
0 = DAC analog voltage is not connected to the DACOUTx pin

Note 1: DACOUTx can only be associated with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DAC output by setting their respective DACOE bit.

Register 3-1: CMPxCON: Comparator x Control Register (Continued)

bit 7-6 **INSEL<1:0>:** Comparator Input Source Select bits

If ALTINP = 0, Select from Comparator Inputs:
11 = Select CMPxD input pin
10 = Select CMPxC input pin
01 = Select CMPxB input pin
00 = Select CMPxA input pin

If ALTINP = 1, Select from Alternate Inputs:
11 = Reserved
10 = Reserved
01 = Select PGA2 output
00 = Select PGA1 output

bit 5 **EXTREF:** External Reference Enable bit

1 = External source provides reference to the DAC (maximum DAC voltage is determined by external voltage source)
0 = Internal reference sources provide reference to the DAC (maximum DAC voltage is determined by the RANGE bit setting)

bit 4 **HYSPOL:** Comparator Hysteresis Polarity Select bit

1 = Hysteresis is applied to the falling edge of the comparator output
0 = Hysteresis is applied to the rising edge of the comparator output

bit 3 **CMPSTAT:** Comparator Status Output Including CMPPOL Selection bit

bit 2 **ALTINP:** Alternate Input Select bit

1 = INSEL<1:0> bits select alternate inputs
0 = INSEL<1:0> bits select comparator inputs

bit 1 **CMPPOL:** Comparator Output Polarity Control bit

1 = Output is inverted
0 = Output is not inverted

bit 0 **RANGE:** DAC Output Voltage Range bit

1 = Max DAC Value = AV_{DD}
0 = Unimplemented: Read as '0'

Note 1: DACOUTx can only be associated with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DAC output by setting their respective DACOE bit.

Register 3-2: CMPxDAC: Comparator x DAC Control Register

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CMREF<11:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **CMREF<11:0>:** Comparator Reference Voltage Select bits

111111111111 = [CMREFx * (AVDD)/4096] volts when AVDD is selected as the voltage reference; (CMREFx * EXTREFx/4096) if the EXTREF bit is set

•
•
•

000000000000 = 0.0V

Note 1: When using an external reference source, the output voltage of the DAC is lower than the set value due to the presence of an internal Electrostatic Discharge (ESD) protection resistor.

2: The ESD resistor has no effect when using the internal voltage reference as the DAC reference source.

4.0 CONFIGURING THE HIGH-SPEED ANALOG COMPARATOR

The High-Speed Analog Comparator module is configured using the CMPxCON register. The INSEL<1:0> (CMPxCON<7:6>) and ALTINP (CMPxCON<2>) bits are used to select the comparator input source. Each comparator has up to six input sources: four external inputs and two internal Programmable Gain Amplifier (PGA) inputs.

The EXTREF bit (CMPxCON<5>) selects between an external reference source and an internal reference source.

When the external reference source is selected, and depending on the comparator channel, either the EXTREF1 or EXTREF2 pin is selected as the external voltage reference, Comparators 1 and 3 use EXTREF1; Comparators 2 and 4 use EXTREF2.

When the EXTREF bit (CMPxCON<5>) is configured for the internal voltage reference, the AVDD is selected by setting the RANGE bit (CMPxCON<0>) to '1'. The polarity of the analog comparator is selected by configuring the CMPPOL bit (CMPxCON<1>).

4.1 12-Bit DAC

Each analog comparator in the High-Speed Analog Comparator module has a dedicated, 12-bit DAC that is used to program the comparator threshold voltage via the CMPxDAC register. Register 3-2 describes how the comparator reference voltage can be calculated based on the input voltage source. With AVDD selected as the input voltage source, the DAC voltage can be incremented/decremented in steps of ~800 µV.

Each DAC has an output enable bit in the Comparator x Control register, DACOE (CMPxCON<8>), that enables the DAC reference voltage to be routed to an external output pin (DACOUTx). The DACOUTx pins can only be associated with a single DAC or PGA output at any given time. If more than one DACOE bit is set, or the PGA Output Enable bit (PGAOEN) and the DACOE bit are set, the DACOUTx will be a combination of the signals.

For devices with a single DAC output pin, the DBCC bit in the FDEVOPT Configuration register, when enabled, interconnects the two DAC outputs. This allows the output of PGA2, DAC2 and DAC4 to be seen on the DAC output pin.

4.2 Pulse Stretcher

The analog comparator can respond to very fast transient signals. To avoid a comparator malfunction, after choosing the comparator output polarity using the CMPPOL bit (CMPxCON<1>), the signal is passed to a pulse stretching circuit.

The pulse stretching circuit waits for the comparator output to transition to a high state or a low state and then will stretch the signal for three clock cycles (PWM clock or system clock). The pulse stretcher clock is selected by configuring the FCLKSEL bit (CMPxCON<9>).

4.3 Digital Filter

In many motor and power control applications, the analog comparator input signals can be corrupted by the large electromagnetic fields generated by the associated external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. A digital output filter can minimize the effects of the input signal corruption.

The digital filter processes the comparator signal from the pulse stretcher circuit. The digital filter is enabled by the FLTREN bit (CMPxCON<10>). The digital filter operates with the clock selected by the FCLKSEL bit (CMPxCON<9>), which can either be the system clock or the PWM clock. The comparator signal must be stable, either in a high state or a low state, for at least three times the selected clock frequency for it to pass through the digital filter. Assuming the current state is '0', an input string of '001010110111' will only yield an output state of '1' at the end of the example sequence, after the three consecutive '1's. Similarly, a sequence of three consecutive '0's is required before the output will change to a '0' state.

Because of the requirement of three similar consecutive states for the filter, the selected digital filter clock period must be one-third or less than the maximum desired comparator response time.

In Sleep mode or Idle mode, the digital filter is bypassed to enable an asynchronous signal from the comparator to the interrupt controller. This asynchronous signal can be used to wake-up the processor from Sleep mode or Idle mode.

4.4 Comparator Outputs

When the digital filter is disabled, the comparator signal is made directly available to the PWM module as a current-limit and/or Fault signal. This ensures minimal latency for Current mode applications and for time-critical (safety) applications. The status signal and the interrupt request signal will be processed by the pulse stretcher circuit.

When the digital filter is enabled, the PWM trigger signal, status signal and interrupt request signal are all processed by the pulse stretcher and the digital filter logic. This will cause a delay in the current-limit/Fault limit event.

4.5 Analog Comparator Interrupt

The analog comparator interrupt can be used to service the comparator switching event and can be enabled or disabled from the interrupt controller. The analog comparator interrupt, if enabled, generates the comparator interrupt signal on the rising edge of the comparator output, following the polarity processing through the CMPPOL bit (CMPxCON<1>), and the subsequent processing by the pulse stretcher and the digital filter logic.

It is very important that the interrupt be generated only on the selected rising edge and not on the subsequent falling edge. If the CMPPOL bit is changed during operation, the CMPPOL bit change will not cause an interrupt. Only the selected edge of an actual change of the comparator output status will initiate an interrupt.

4.6 Comparator Hysteresis Control

The HYSSEL<1:0> bits (CMPxCON<12:11>) specify the amount of hysteresis for the analog comparator. The HYSPOL bit (CMPxCON<4>) specifies whether hysteresis is applied to the rising edge or falling edge of the signal.

Configuration of hysteresis (see Example 4-1) helps the comparator to avoid oscillation (i.e., toggling of the comparator output), which could be caused by noise in the positive input.

Example 4-1: Configuration of Hysteresis Control

```
// Select comparator hysteresis
CMP1CONbits.HYSSEL = 3;    // 45 mV hysteresis selected
CMP1CONbits.HYSPOL = 0;    // Hysteresis is applied to rising edge of the
                           // comparator output
```

4.7 Operation in Sleep and Idle Mode

During Sleep mode, the High-Speed Analog Comparator continues to function in a reduced manner, allowing the device to wake-up when an active signal is applied to the comparator input. To reduce power consumption when the device enters Idle mode, the comparator module can be disabled by setting the CMPSIDL bit. If a device has multiple comparators, and if any CMPSIDL bit is set, then the entire group of comparators will be disabled while in Idle mode.

5.0 APPLICATION INFORMATION

The High-Speed Analog Comparator module provides comparators that can be used in many power conversion applications. The outputs of the SMPS analog comparator module can be used to perform the following functions:

- Generate an interrupt
- Trigger an ADC sample and convert process
- Truncate the PWM signal (current-limit)
- Truncate the PWM period (Current Reset)
- Disable the PWM outputs (Fault latch)

The output of the SMPS analog comparator module can be used in multiple modes at the same time. For example, the comparator output can be used to generate an interrupt, have the ADC take a sample and convert it, and truncate the PWM output, all in response to a voltage being detected beyond its expected value.

The SMPS analog comparator module can also be used to wake-up the system from Sleep mode or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

The potential applications of the SMPS analog comparator module are numerous and varied. The following section describes a typical application in power conversion circuits.

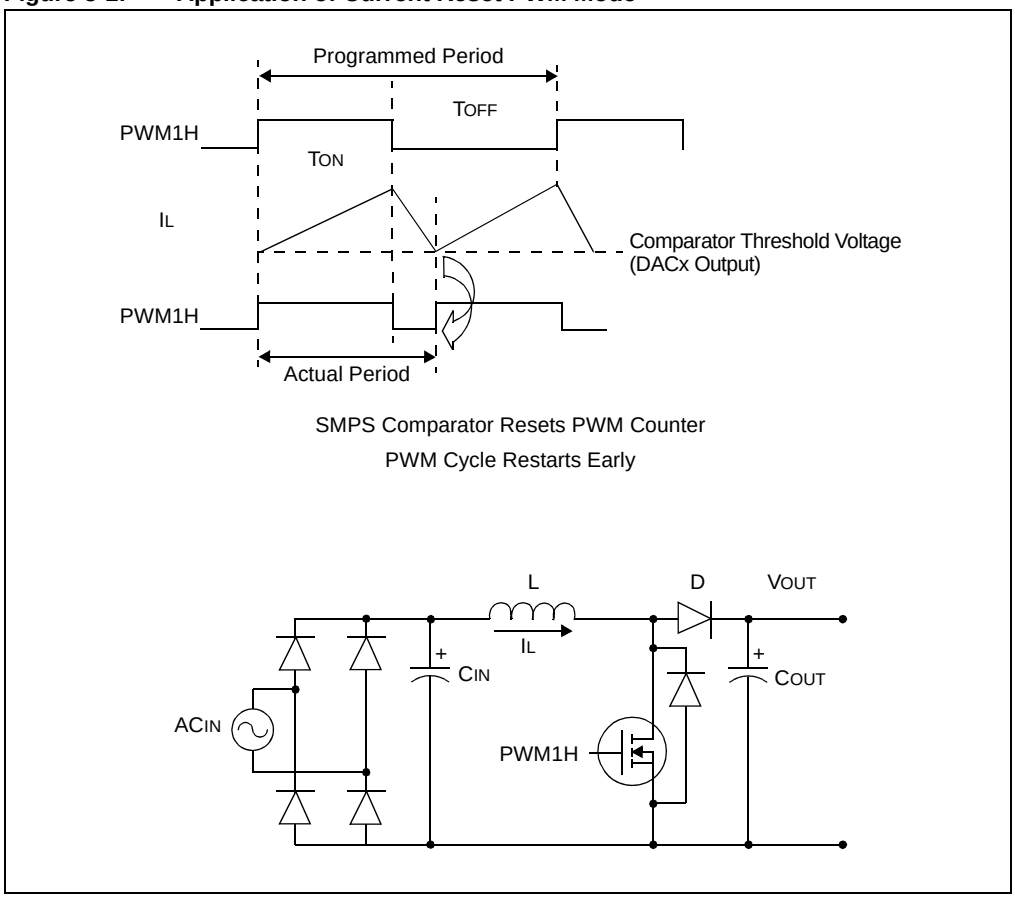
5.1 Power Factor Correction (PFC) Boost Converter: PWM Reset Using the High-Speed Analog Comparator

Analog comparators are widely used in PFC boost converter applications, as illustrated in Figure 5-1. The SMPS analog comparator module can be utilized for this application instead of adding expensive circuitry. The SMPS analog comparator is used in conjunction with the SMPS power supply PWM module to generate the Current Reset mode PWM signal.

The SMPS analog comparator is configured to reset the PWM module when the measured current through the inductor falls below the minimum acceptable current level. This minimum current level is determined by the application.

Initially, the power semiconductor switch is turned on. After a constant ON time, the switch is turned off and the PWM module waits for the current to decay below the comparator threshold. When the current falls below the threshold, the comparator resets the PWM module, turning the power semiconductor switch back on, and thereby, energizing the inductor.

Figure 5-1: Application of Current Reset PWM Mode



6.0 HIGH-SPEED ANALOG COMPARATOR LIMITATIONS

6.1 Comparator Input Range

The High-Speed Analog Comparator has a limitation for the input Common-Mode Range (CMR) to not exceed (AV_{DD} + 0.2V). This means that both inputs to the comparator (the selected CMPx input pin and the selected reference source) should be within this range. As long as one of the inputs is within the CMR, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated. If both inputs exceed the CMR, the comparator output will be indeterminate.

6.2 DAC Input Range

The maximum reference voltage input to the DAC should not exceed 3.6 V_{DC}. If the reference voltage input exceeds this value, the DAC output will be indeterminate.

6.3 EXTREF Range

If the external reference is selected as the DAC reference source, the voltage at the EXTREFx pin should not exceed 3.6 V_{DC}. If the voltage at the EXTREFx pin exceeds this value, the comparator output may become unpredictable.

7.0 REGISTER MAP

A summary of the registers associated with the High-Speed Analog Comparator module is provided in Table 7-1.

Table 7-1: Analog Comparator Control Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPxCON	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMPxDAC	—	—	—	—	CMREF<11:0>												0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

8.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33E/PIC24E device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Speed Analog Comparator module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33E/PIC24E family of devices.

9.0 REVISION HISTORY

Revision A (June 2013)

This is the initial released revision of this document.

Revision B (September 2014)

This revision incorporates the following updates:

- Sections:
  - Updated **Section 1.0 “Introduction”**, **Section 3.0 “Control Registers”** and **Section 4.0 “Configuring the High-Speed Analog Comparator”**
- Figures:
  - Updated Figure 2-1
- Registers:
  - Updated Register 3-1 and Register 3-2
- Examples:
  - Updated Example 4-1
- Tables:
  - Table 7-1
- Changes to text and formatting were incorporated throughout the document.

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