PIC16(L)F176X

PIC16(L)F176X Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F1764
- PIC16F1765
- PIC16F1768
- PIC16F1769
- PIC16LF1764
- PIC16LF1765
- PIC16LF1768
- PIC16LF1769

1.0 OVERVIEW

The device can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}$/V_{PP} pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the PIC16(L)F176X devices can be programmed using a single V_{DD} source in the operating range. The $\overline{MCLR}$/V_{PP} pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}$/V_{PP} pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1: The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}$/V_{PP} pin.

2: While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-1.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	**Pin Type**	**Pin Description**
ICSPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ICSPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{\text{MCLR}}$/VPP	Program/Verify mode	P[1]	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16L(F)1764/5 family are shown in Figure 2-1 and Figure 2-2.

The pin diagrams for the PIC16L(F)1768/9 family are shown in Figure 2-3 and Figure 2-4.

The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 14-PIN PDIP, SOIC, TSSOP

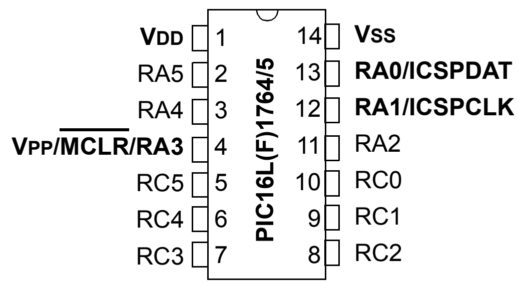


FIGURE 2-2: 16-PIN QFN

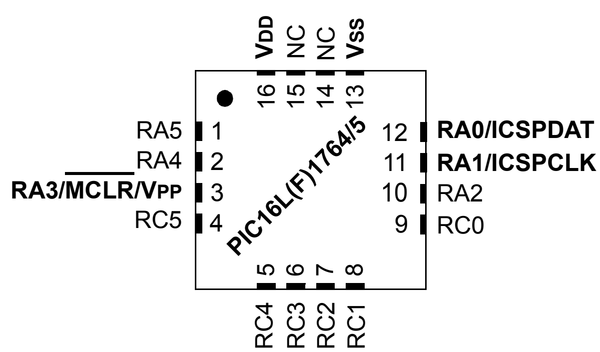


FIGURE 2-3: 20-PIN PDIP, SOIC, SSOP

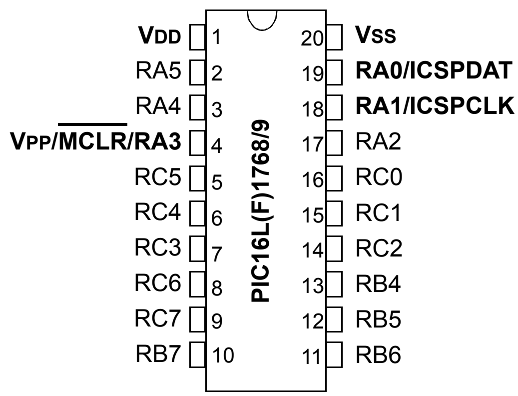
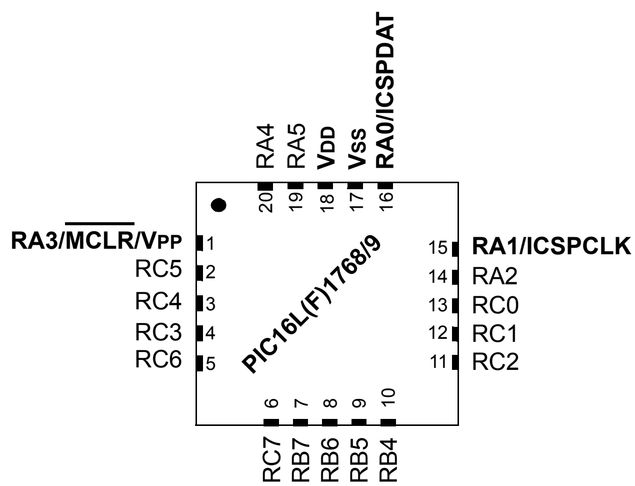


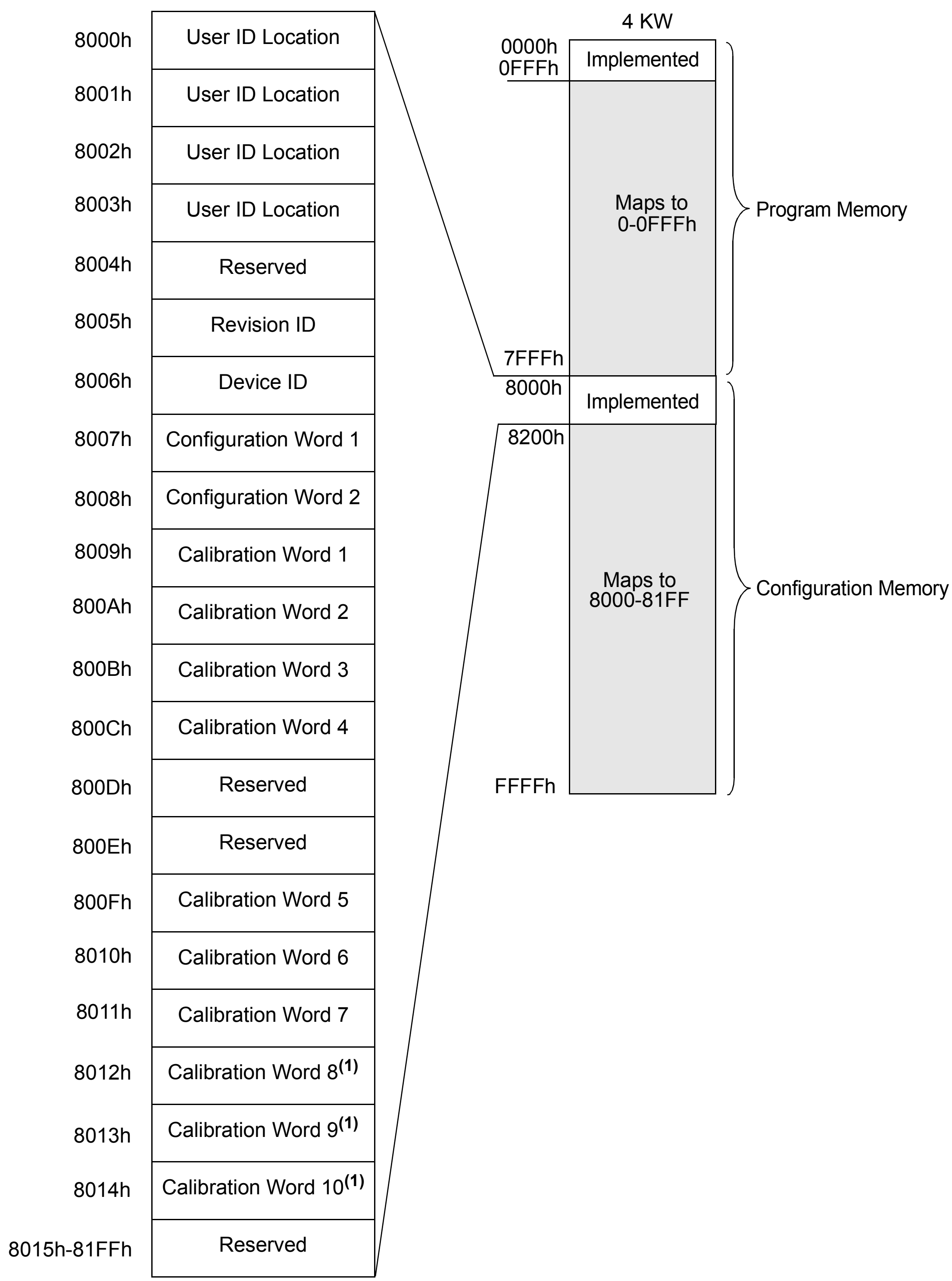
FIGURE 2-4: 20-PIN QFN (4X4)



3.0 MEMORY MAP

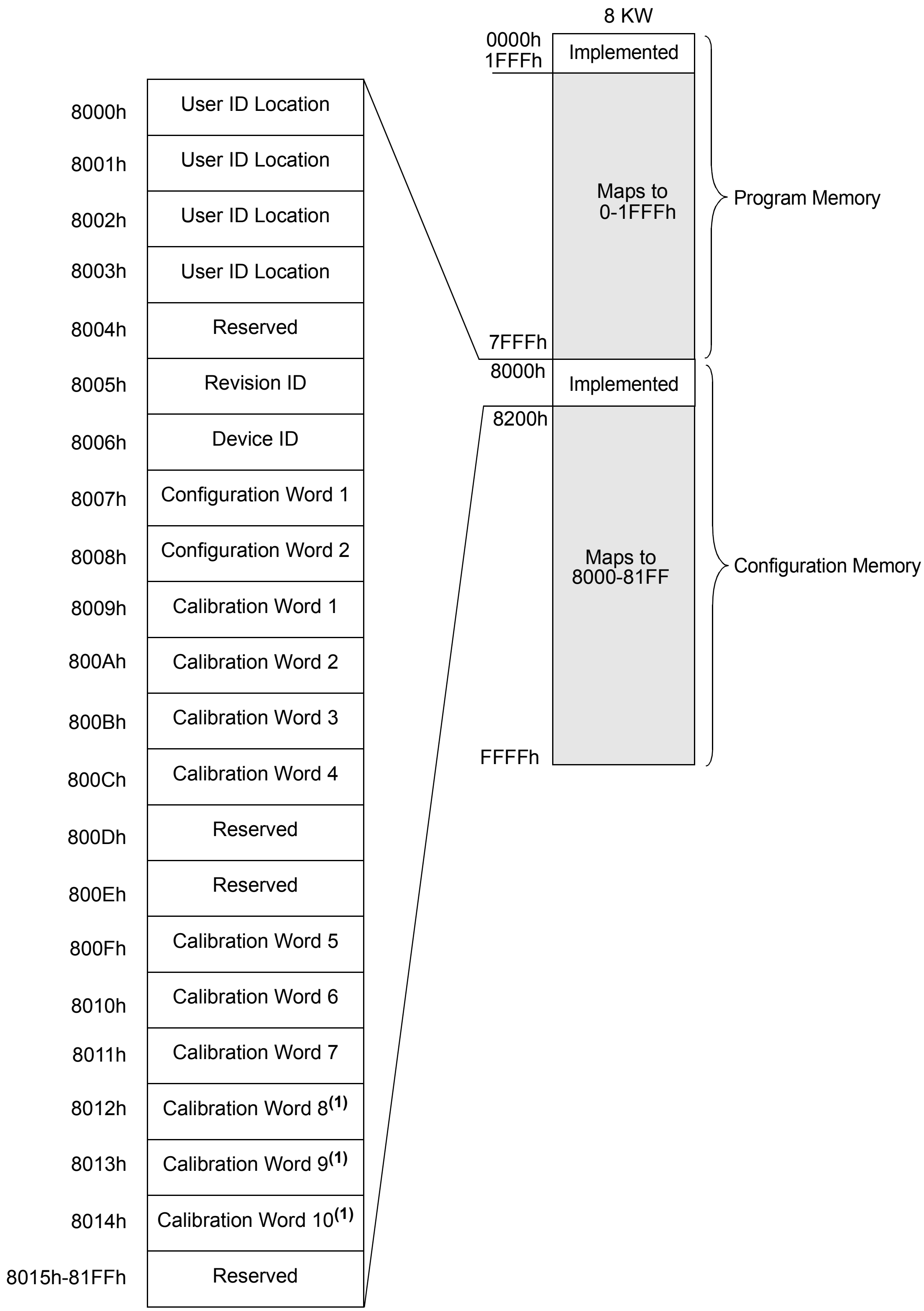
The memory is separated into two sections: program memory and configuration memory.

FIGURE 3-1: PIC16(L)F1764/8 PROGRAM MEMORY MAPPING



Note 1: These locations are reserved in the PIC16(L)F1764.

FIGURE 3-2: PIC16(L)F1765/9 PROGRAM MEMORY MAPPING



Note 1: These locations are reserved in the PIC16(L)F1765.

3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note: MPLAB® IDE only displays the seven Least Significant bits (LSb) of each user ID location; the upper bits are not read. It is recommended that only the seven LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device/Revision ID

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified.

REGISTER 3-1: DEVICEID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit		
‘0’ = Bit is cleared	‘1’ = Bit is set	x = Bit is unknown

bit 13-0 **DEV<13:0>:** Device ID bits
Refer to Table 3-1 to determine what these bits will read on which device. A value of 3FFFh is invalid.

Note 1: This location cannot be written.

REGISTER 3-2: REVISIONID: REVISION ID REGISTER(1)

R	R	R	R	R	R
REV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
REV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit		
‘0’ = Bit is cleared	‘1’ = Bit is set	x = Bit is unknown

bit 13-0 **REV<13:0>:** Revision ID bits
These bits are used to identify the device revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

Device	Device ID	Revision ID
PIC16F1764	3080h	2xxxh
PIC16LF1764	3082h	2xxxh
PIC16F1765	3081h	2xxxh
PIC16LF1765	3083h	2xxxh
PIC16F1768	3084h	2xxxh
PIC16LF1768	3086h	2xxxh
PIC16F1769	3085h	2xxxh
PIC16LF1769	3087h	2xxxh

3.3 Configuration Words

The device has two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in the Calibration Word locations. See Figure 3-1 for address information.

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-3: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
`1 = ON` Fail-Safe Clock Monitor is enabled
`0 = OFF` Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
`1 = ON` Internal/External Switchover mode is enabled
`0 = OFF` Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
`1 = OFF` CLKOUT function is disabled. I/O or oscillator function on CLKOUT
`0 = ON` CLKOUT function is enabled on CLKOUT

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.

REGISTER 3-3: CONFIGURATION WORD 1 (CONTINUED)

bit 10-9	**BOREN<1:0>:** Brown-out Reset Enable bits[1] `11 = ON` BOR enabled `10 = SLEEP` BOR enabled during operation and disabled in Sleep `01 = SBODEN` BOR controlled by SBOREN bit of the BORCON register `00 = OFF` BOR disabled
bit 8	**Unimplemented:** Read as '`1`'
bit 7	**$\overline{\text{CP}}$:** Code Protection bit[2] `1 = OFF` Program memory code protection is disabled `0 = ON` Program memory code protection is enabled
bit 6	**MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit <u>If LVP bit = `1 (ON)`:</u> This bit is ignored. <u>If LVP bit = `0 (OFF)`:</u> `1 = ON` $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled. `0 = OFF` $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of port pin's WPU control bit.
bit 5	**$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit[1] `1 = OFF` PWRT disabled `0 = ON` PWRT enabled
bit 4-3	**WDTE<1:0>:** Watchdog Timer Enable bit `11 = ON` WDT enabled `10 = SLEEP` WDT enabled while running and disabled in Sleep `01 = SWDTEN` WDT controlled by the SWDTEN bit in the WDTCON register `00 = OFF` WDT disabled
bit 2-0	**FOSC<2:0>:** Oscillator Selection bits `111 = ECH` External Clock, High-Power mode: CLKIN on OSC1/CLKIN `110 = ECM` External Clock, Medium-Power mode: CLKIN on OSC1/CLKIN `101 = ECL` External Clock, Low-Power mode: CLKIN on OSC1/CLKIN `100 = INTOSC` Internal HFINTOSC, I/O function on OSC1/CLKIN `011 = EXTRC` External RC oscillator, RC function on OSC1/CLKIN `010 = HS` High-speed crystal/resonator on OSC2/CLKOUT pin and OSC1/CLKIN `001 = XT` Crystal/resonator on OSC2/CLKOUT pin and OSC1/CLKIN `000 = LP` Low-power crystal on OSC2/CLKOUT pin and OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.

2: The entire program memory will be erased when the code protection is turned off.

REGISTER 3-4: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	PLLEN
bit 13					bit 8

R/P-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1
$\overline{\text{ZCD}}$	—	—	—	—	PPS1WAY	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
`1 = ON` Low-voltage programming enabled
`0 = OFF` $\overline{\text{MCLR}}$/VPP must be used for programming high voltage

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
`1 = OFF` In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
`0 = ON` In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power Brown-out Reset Enable bit
`1 = OFF` Low-Power Brown-out Reset is disabled
`0 = ON` Low-Power Brown-out Reset is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit(2)
`1 = LOW` Brown-out Reset voltage (VBOR), low trip point selected
`0 = HIGH` Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
`1 = ON` Stack Overflow or Underflow will cause a Reset
`0 = OFF` Stack Overflow or Underflow will not cause a Reset

bit 8 **PLLEN:** PLL Enable bit
`1 = ON` 4xPLL enabled
`0 = OFF` 4xPLL disabled

bit 7 **$\overline{\text{ZCD}}$:** Zero-Cross Detect Enable bit
`1 = OFF` Zero-cross detection is disabled on POR. Zero-cross detection can be controlled by software.
`0 = ON` Zero-cross detection is always enabled. Software cannot disable zero-cross detection.

bit 6-3 **Unimplemented:** Read as ‘1’

bit 2 **PPS1WAY:** PPSLOCK One-Way Set Enable bit
`1 = ON` The PPSLOCK bit is permanently set after the first access sequence that sets it.
`0 = OFF` The PPSLOCK bit can be set and cleared as needed by the PPSLOCK access sequence.

Note 1: The LVP bit cannot be programmed to ‘0’ when Programming mode is entered via LVP.
2: See VBOR parameter for specific trip point voltages.

REGISTER 3-4: CONFIGURATION WORD 2 (CONTINUED)

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits

4 kW Flash memory (PIC16(L)F1764/8):

- `11 = OFF` Write protection off
- `10 = BOOT` 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
- `01 = HALF` 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
- `00 = ALL` 000h to FFFh write-protected, no addresses may be modified by PMCON control

8 kW Flash memory (PIC16(L)F1765/9):

- `11 = OFF` Write protection off
- `10 = BOOT` 0000h to 03FFh write-protected, 0400h to 1FFFh may be modified by PMCON control
- `01 = HALF` 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
- `00 = ALL` 0000h to 1FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

2: See VBOR parameter for specific trip point voltages.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First Entry mode
- VDD – First Entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has $\overline{\text{MCLR}}$ disabled (MCLRE = `0`), the power-up time is disabled ($\overline{\text{PWRTE}}$ = `0`), the internal oscillator is selected (FOSC = `100`), and RA0 and RA1 are driven by the user application, the device will execute code. Since this may prevent entry, VPP-First Entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figure 8-3 and Figure 8-4.

> **Note:** In systems where the VDD and $\overline{\text{MCLR}}$/VPP signals can be controlled independently the VPP-last method of exit should be used to keep the device in Reset, thereby preventing any issues that may be caused by program execution.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F176X devices to be programmed using VDD only, without high voltage. When the LVP bit of the Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, `'0100 1101 0100 0011 0100 1000 0101 0000'` (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See Figure 8-8 and Figure 8-9.

Note:	To enter LVP mode, the LSb of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3 Program/Verify Commands

These devices implement 13 programming commands, each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay, 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data for Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data from Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

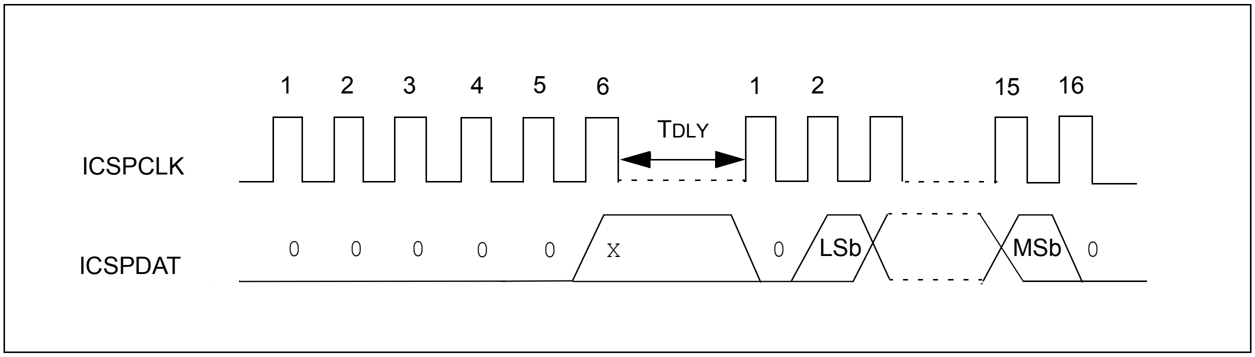
The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note:	Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

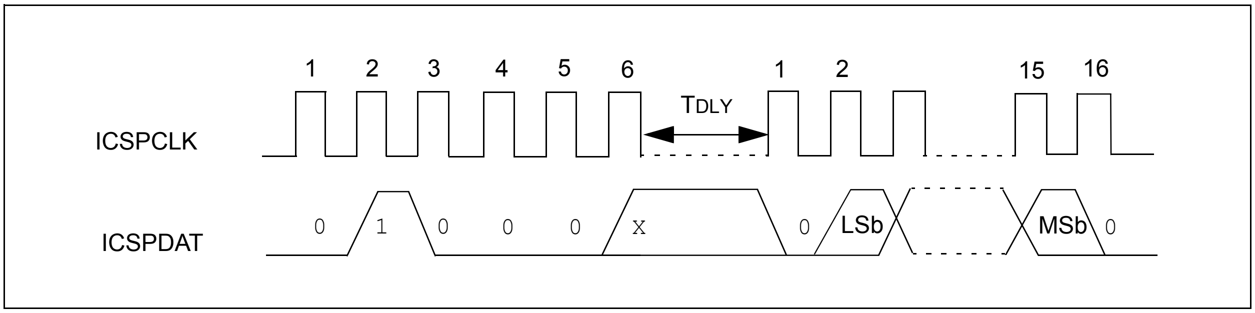
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

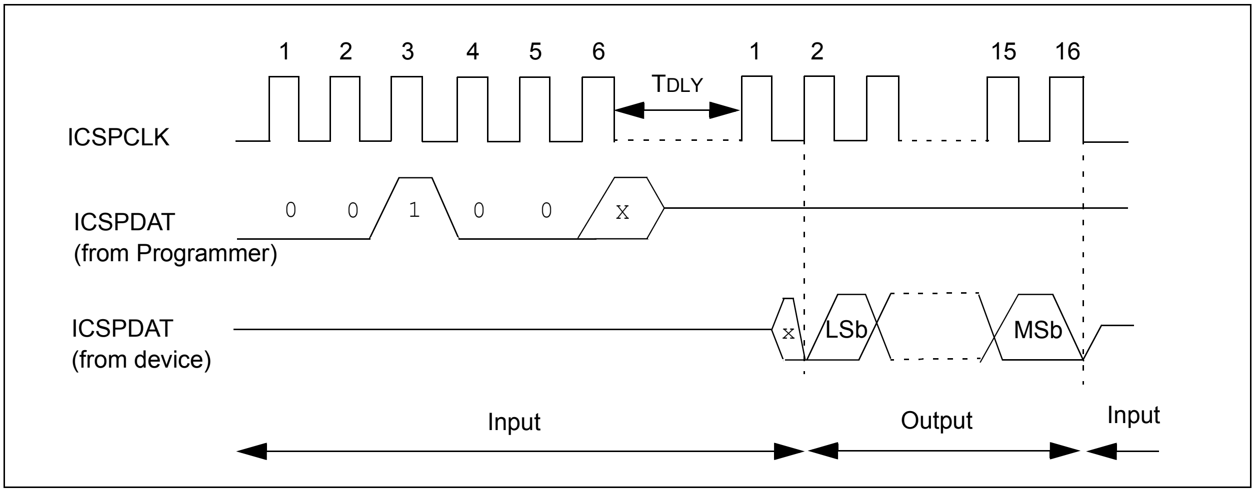
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY

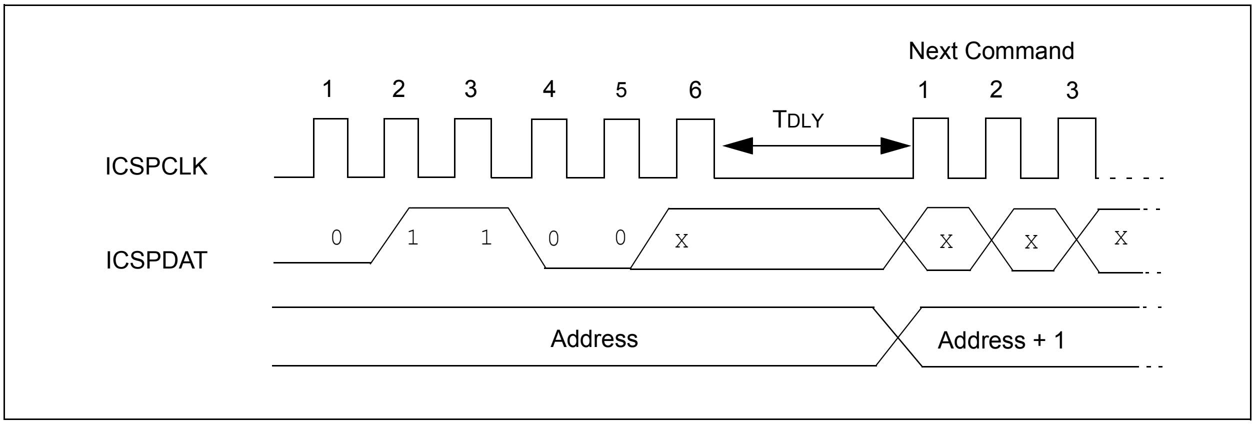


4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it.

If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h (see Figure 4-4).

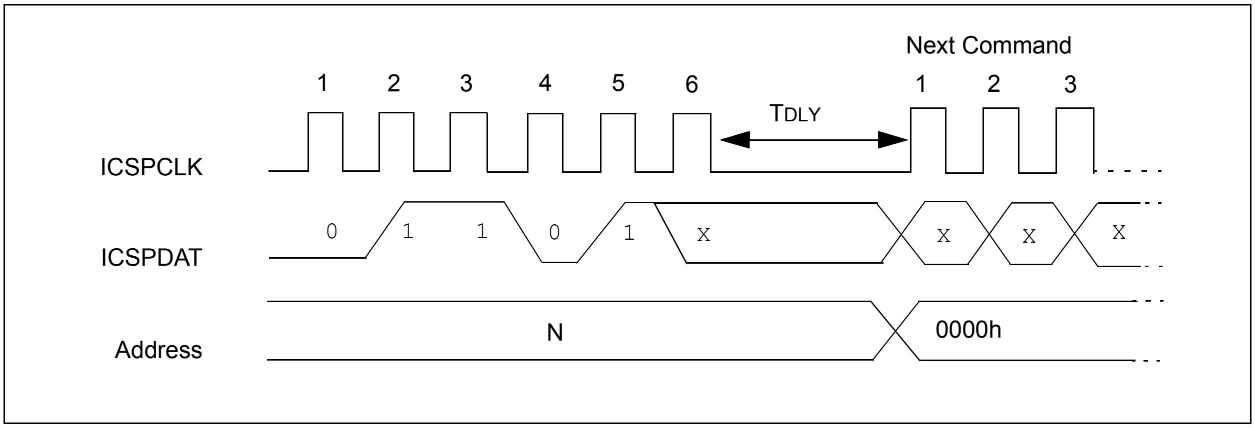
FIGURE 4-4: INCREMENT ADDRESS



4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory. See Figure 4-5.

FIGURE 4-5: RESET ADDRESS



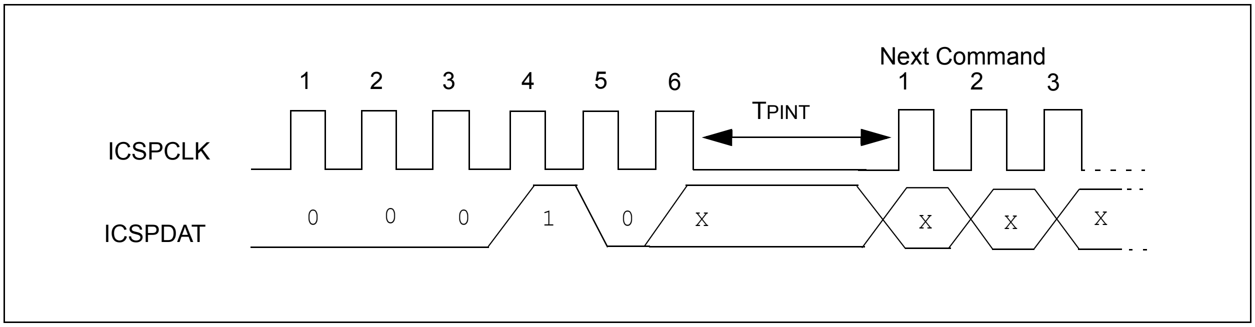
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, in order for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed. See Figure 4-6.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

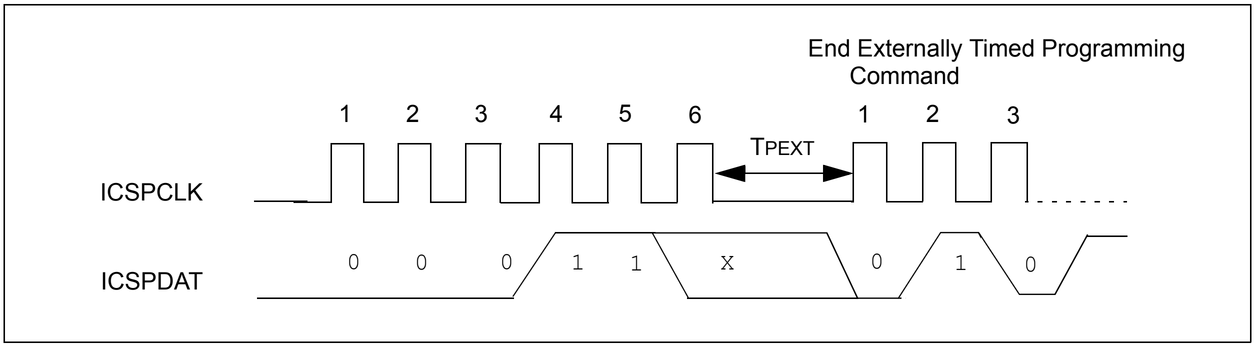


4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT. See Figure 4-7.

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING

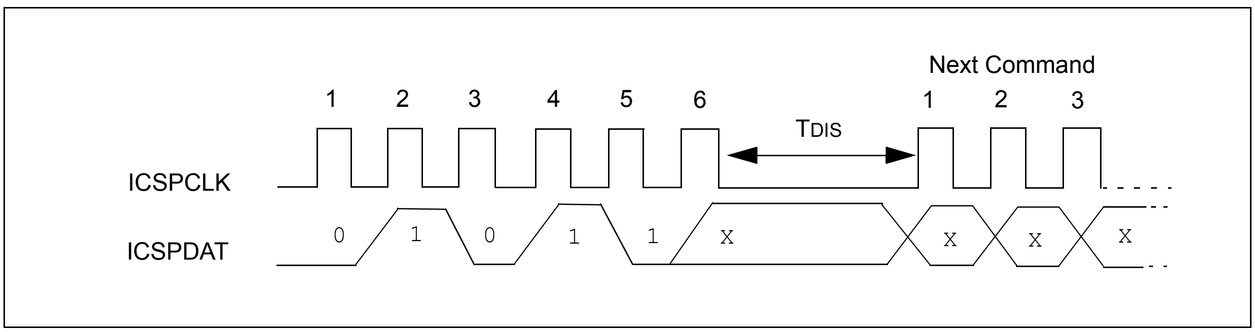


4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands. See Figure 4-8.

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions, dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

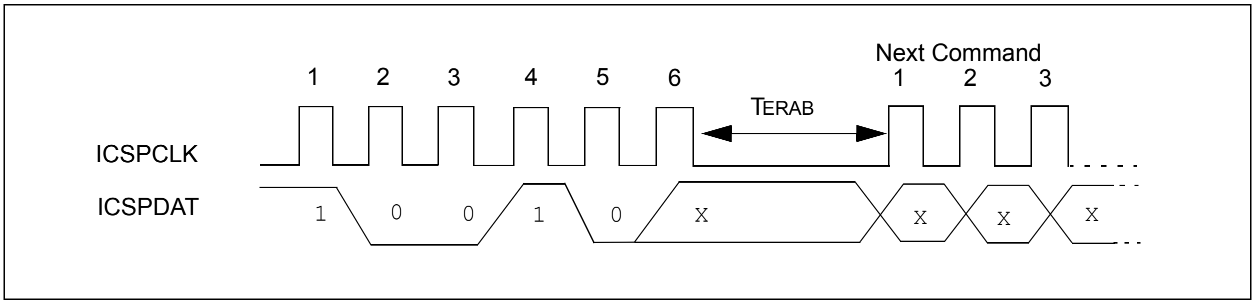
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval, TERAB, has expired. See Figure 4-9.

Note:	The Code Protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY



4.3.10 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h, the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, TERAR, has expired. See Figure 4-10.

FIGURE 4-10: ROW ERASE PROGRAM MEMORY

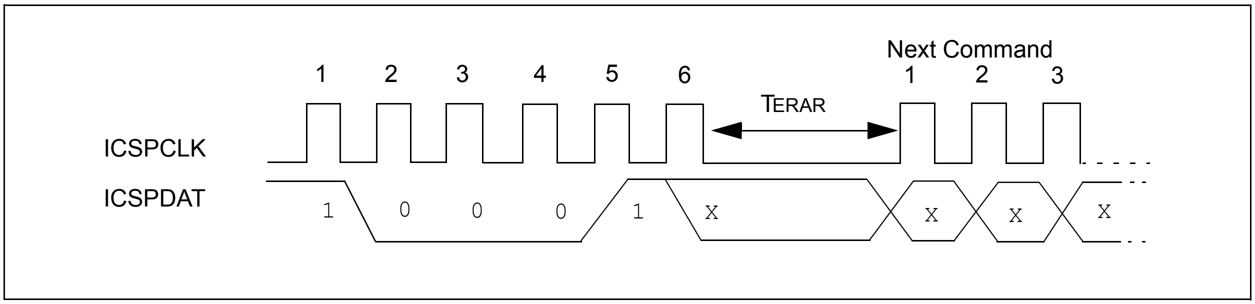


TABLE 4-2: PROGRAMMING ROW AND LATCH SIZES

Devices	PC	Erase Row Size (Number of 14-bit Words)	Write Row Size (Number of 14-bit Latches)
PIC16F1764	<15:5>	32	32
PIC16F1765			
PIC16F1768			
PIC16F1769			
PIC16LF1764			
PIC16LF1765			
PIC16LF1768			
PIC16LF1769			

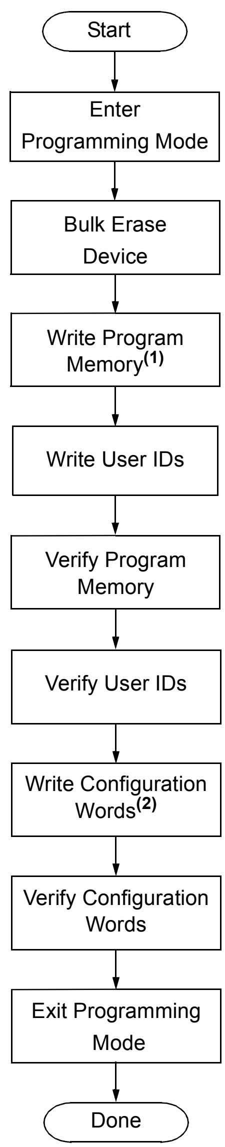
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC address bits indicated in Table 4-2 at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address 0002h-0021h in a 32-latch device will result in data being written to 0020h-003Fh.

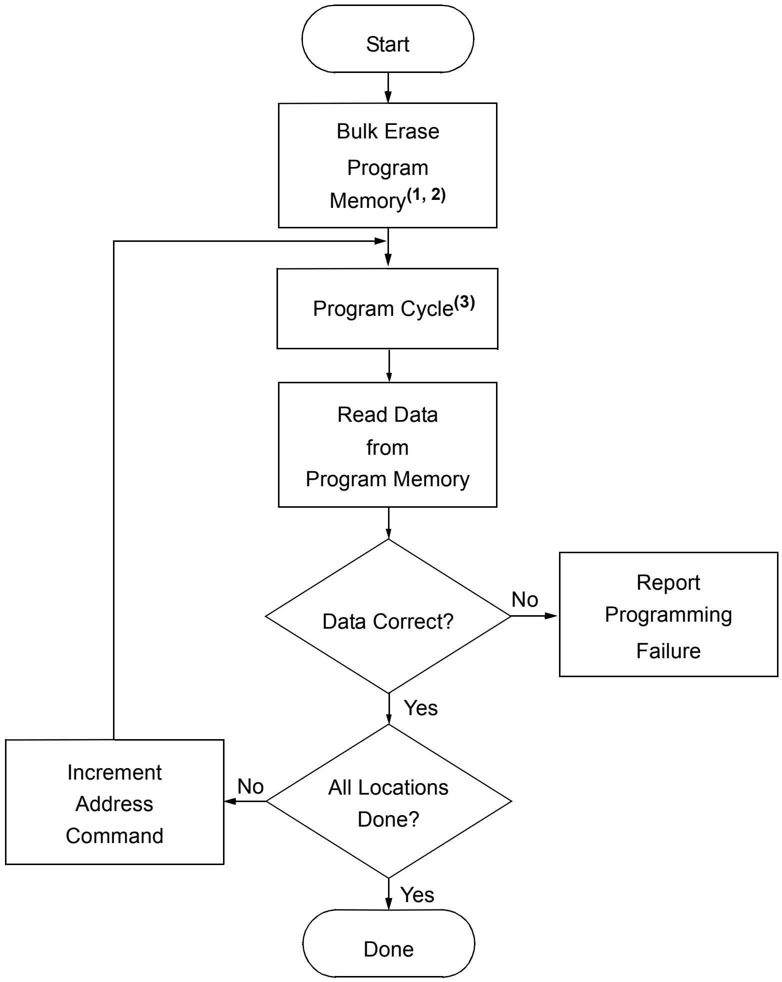
If more than the maximum number of latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. Figure 5-1 through Figure 5-6 show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 5-2.
2: See Figure 5-5.

FIGURE 5-2: PROGRAM MEMORY FLOWCHART

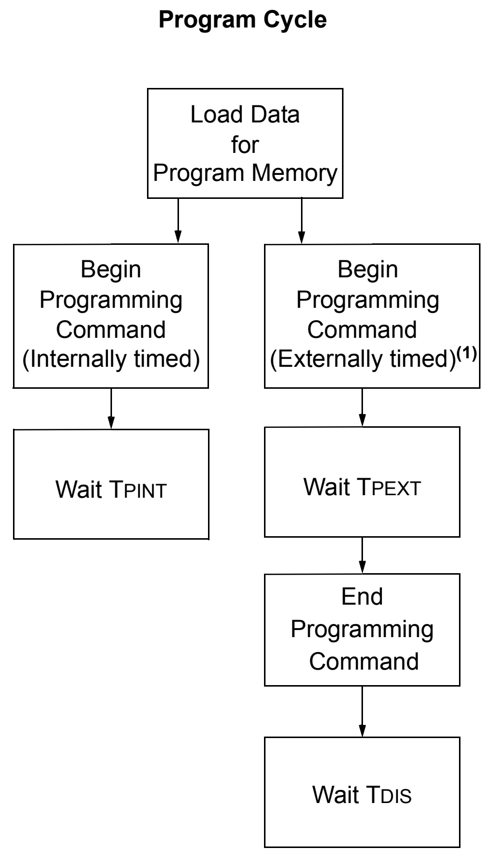


Note 1: This step is optional if the device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 5-6.

3: See Figure 5-3 or Figure 5-4.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

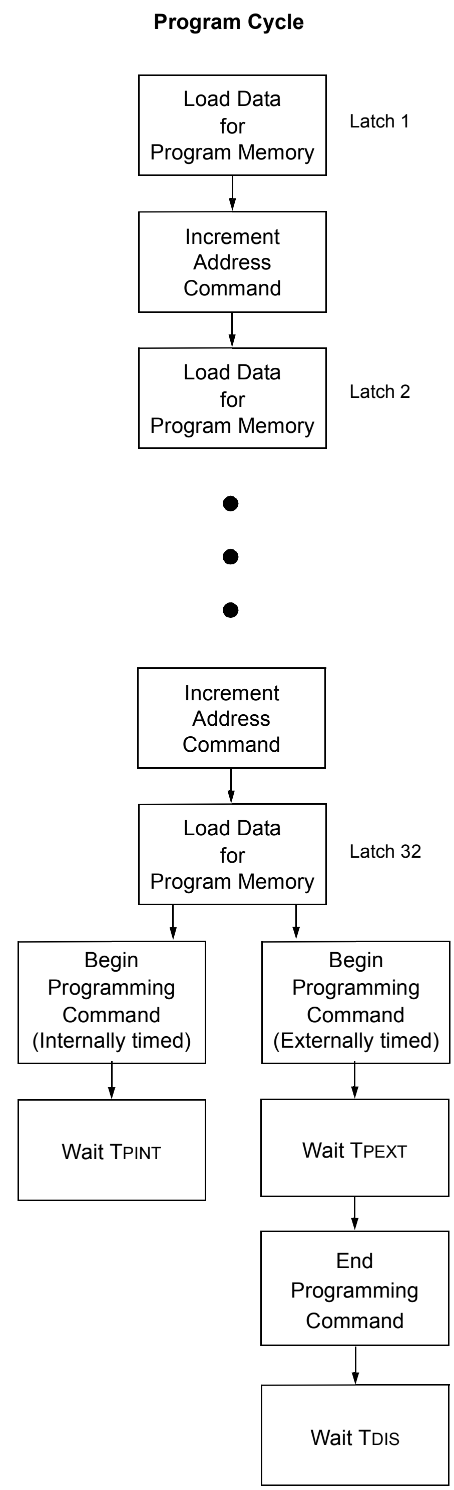
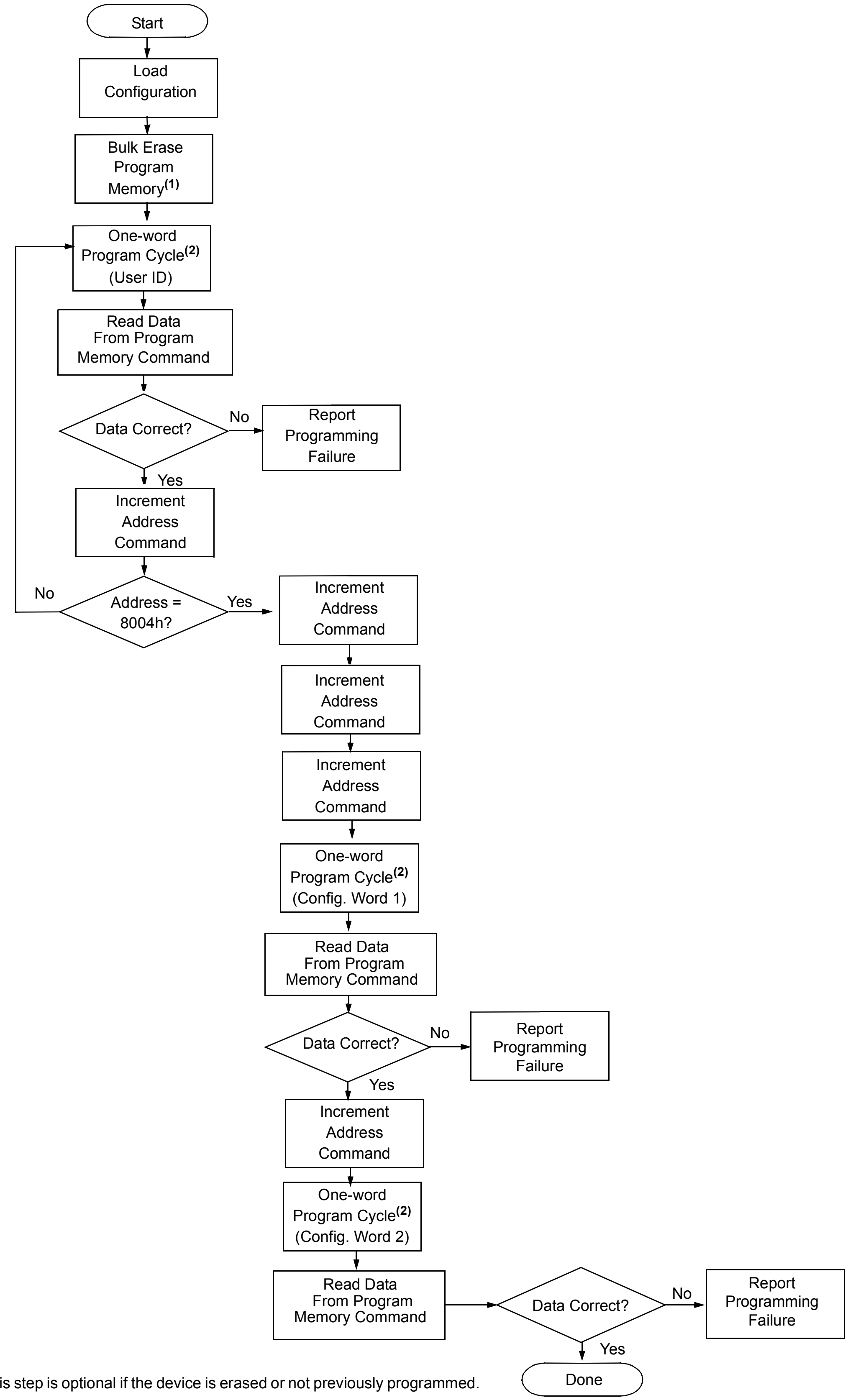


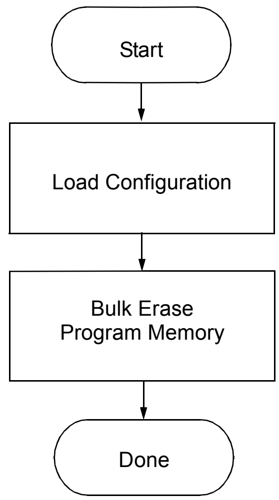
FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if the device is erased or not previously programmed.

2: See Figure 5-3.

FIGURE 5-6: ERASE FLOWCHART



Note: This sequence does not erase the Calibration Words.

6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh). Program memory can still be programmed and read during program execution.

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: The Configuration Word 1 is stored at 8007h. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC16F1764	3EFFh	3F87h
PIC16LF1764	3EFFh	3F87h
PIC16F1765	3EFFh	3F87h
PIC16LF1765	3EFFh	3F87h
PIC16F1768	3EFFh	3F87h
PIC16LF1768	3EFFh	3F87h
PIC16F1769	3EFFh	3F87h
PIC16LF1769	3EFFh	3F87h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16(L)F176X program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location (e.g., FFFh for the PIC16F1764). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to ‘0’.

7.3.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB® IDE check box for Configure → ID Memory... → Use Unprotected Checksum is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the user ID. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four user ID locations. The Most Significant checksum nibble is stored in the user ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations. The protected checksums in Table 7-2 assume that the Use Unprotected Checksum box is checked.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each user ID is used to create a 16-bit value. The Least Significant nibble of user ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of user ID location 8001h is the second Most Significant nibble, and so forth for the remaining user IDs and 16-bit value nibbles. The resulting 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to ‘0’.

TABLE 7-2: CHECKSUMS

Device	Config1			Config2		Checksum			
						Unprotected		Code-protected	
	Unprotected	Protected	Mask	Word	Mask	Blank	00AAh First and Last	Blank	00AAh First and Last
PIC16F1764	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	6E86h	EFDCh	EC8Ch	6DE2h
PIC16F1765	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	5E86h	DFDCh	DC8Ch	5DE2h
PIC16F1768	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	6E86h	EFDCh	EC8Ch	6DE2h
PIC16F1769	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	5E86h	DFDCh	DC8Ch	5DE2h
PIC16LF1764	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	6E86h	EFDCh	EC8Ch	6DE2h
PIC16LF1765	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	5E86h	DFDCh	DC8Ch	5DE2h
PIC16LF1768	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	6E86h	EFDCh	EC8Ch	6DE2h
PIC16LF1769	3FFFh	3F7Fh	3EFFh	3FFFh	3F87h	5E86h	BFDCh	DC8Ch	5DE2h

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Programming Supply Voltages and Currents							
V_{DD}	Supply Voltage (V_{DDMIN}(2), V_{DDMAX})	PIC16LF176X	1.80 2.50	—	3.60 3.60	V V	$F_{OSC} \leq$ 16 MHz F_{OSC} > 16 MHz
		PIC16F176X	2.30 2.50	—	5.50 5.50	V V	$F_{OSC} \leq$ 16 MHz F_{OSC} > 16 MHz
V_{PEW}	Read/Write and Row Erase operations		V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase operations		2.7	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle		—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming		—	—	3.0	mA	
	V_{PP}						
I_{PP}	Current on $\overline{MCLR}/V_{PP}$		—	—	600	µA	
V_{IHH}	High voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify mode entry		8.0	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry		—	—	1.0	µs	
	I/O pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input high level		0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input low level		—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT output high level		V_{DD} – 0.7 V_{DD} – 0.7 V_{DD} – 0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 2 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT output low level		—	—	V_{SS} + 0.6 V_{SS} + 0.6 V_{SS} + 0.6	V	I_{OH} = 8 mA, V_{DD} = 5V I_{OH} = 6 mA, V_{DD} = 3.3V I_{OH} = 3 mA, V_{DD} = 1.8V
V_{BOR}	Brown-out Reset Voltage: BORV = 0 (high trip) BORV = 1 (low trip)		— — —	2.70 2.40 1.90	— — —	V V V	PIC16(L)F176X PIC16F176X PIC16LF176X
Programming Mode Entry and Exit							
T_{ENTS}	Programming mode entry setup time: ICSPCLK, ICSPDAT setup time before V_{DD} or $\overline{MCLR}$↑		100	—	—	ns	
T_{ENTH}	Programming mode entry hold time: ICSPCLK, ICSPDAT hold time after V_{DD} or $\overline{MCLR}$↑		250	—	—	µs	
Serial Program/Verify							
T_{CKL}	Clock Low Pulse Width		100	—	—	ns	
T_{CKH}	Clock High Pulse Width		100	—	—	ns	
T_{DS}	Data in setup time before clock↓		100	—	—	ns	
T_{DH}	Data in hold time after clock↓		100	—	—	ns	
T_{CO}	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

2: Bulk-erased devices default to brown-out enabled. V_{DDMIN} is 2.85V when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TLZD	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	
TDLY	Data input not driven to next clock input (delay required between command/data or command/ command)	1.0	—	—	µs	
TERAB	Bulk Erase cycle time	—	—	5	ms	
TERAR	Row Erase cycle time	—	—	2.5	ms	
TPINT	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	Note 1
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	µs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	µs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

2: Bulk-erased devices default to brown-out enabled. VDDMIN is 2.85V when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

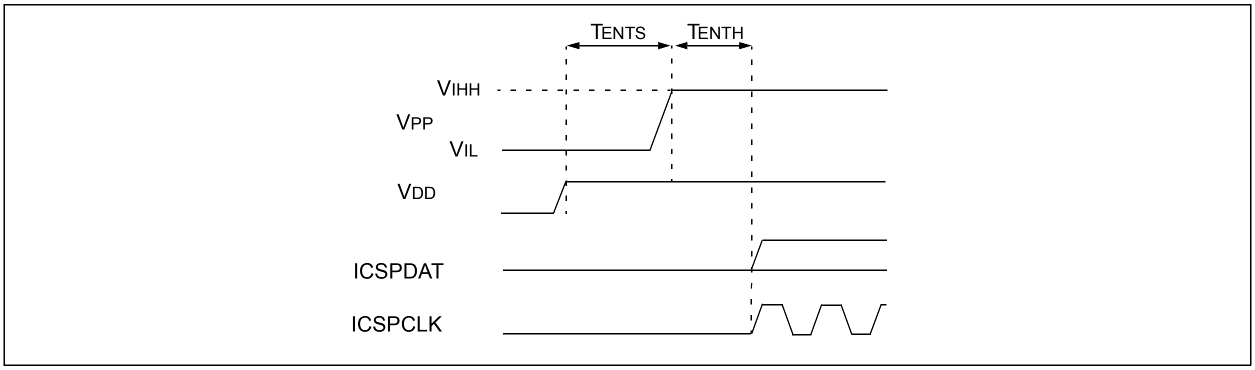


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

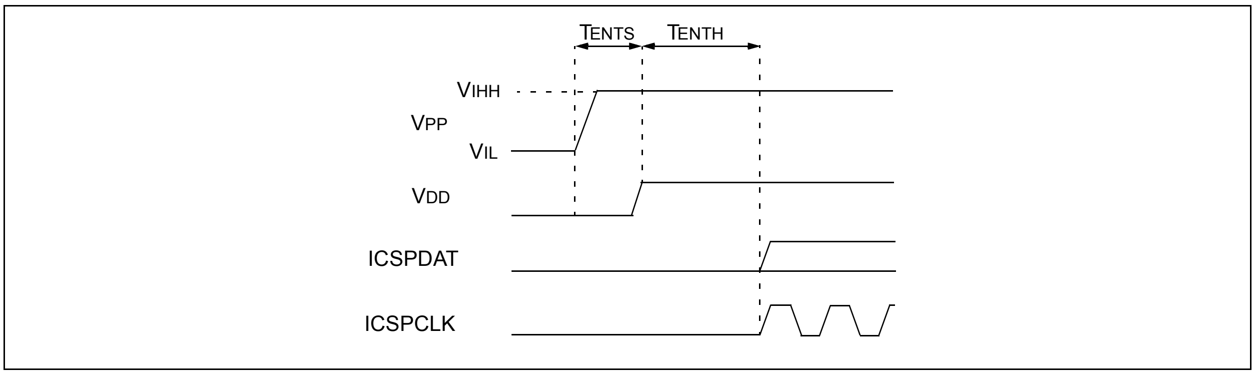


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

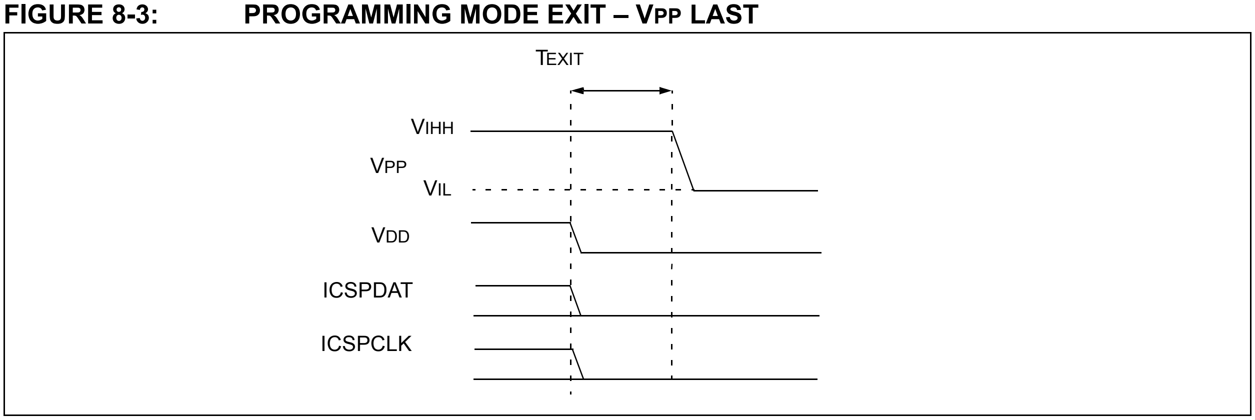


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST

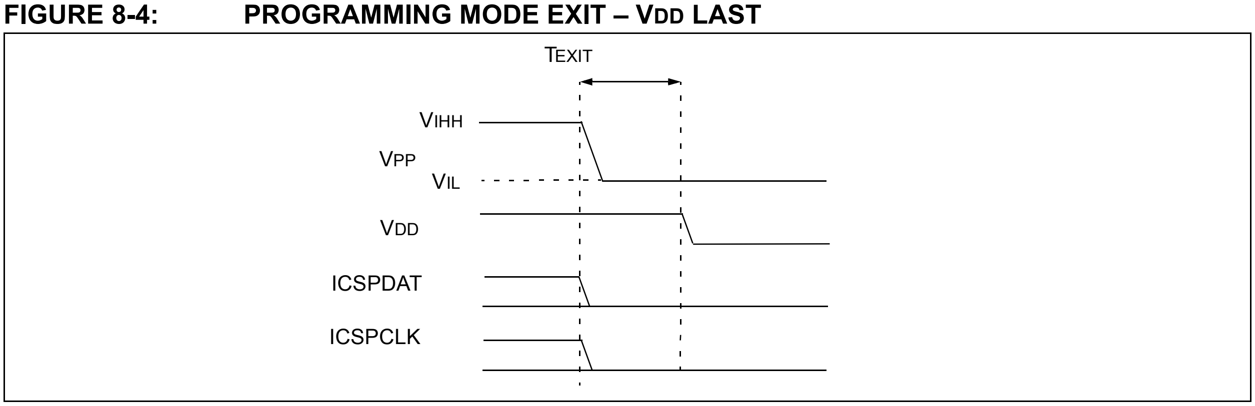


FIGURE 8-5: CLOCK AND DATA TIMING

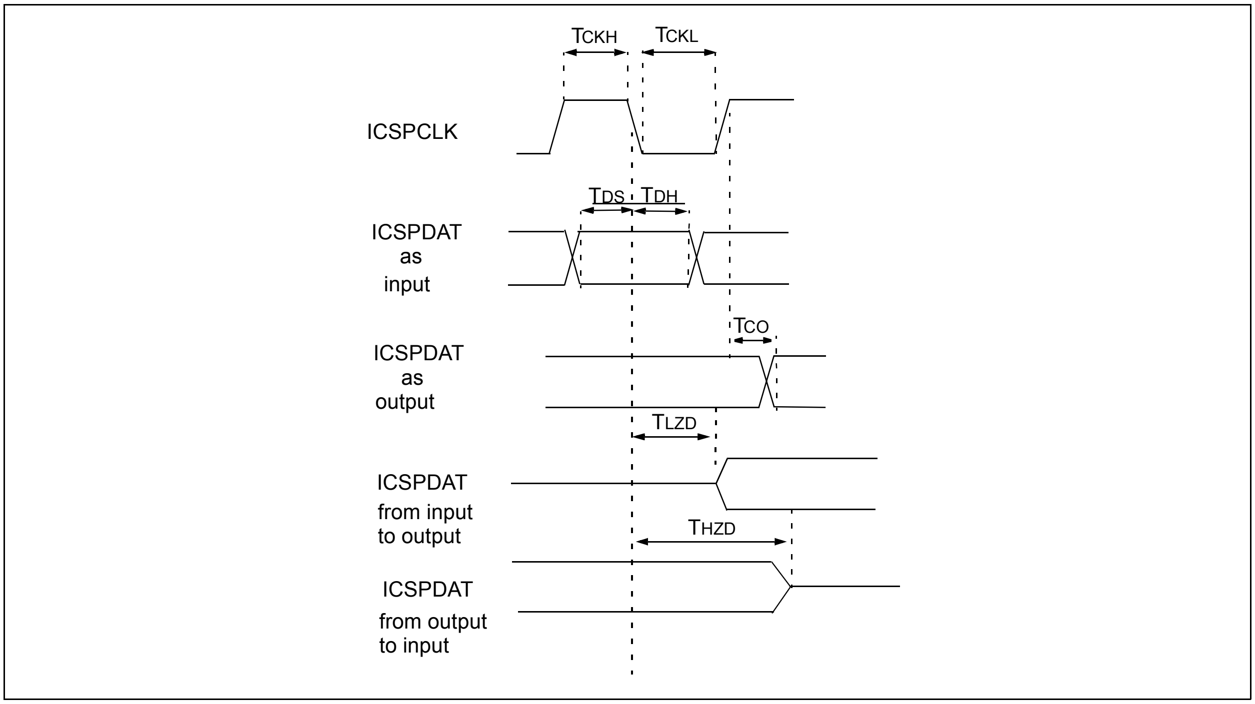


FIGURE 8-6: WRITE COMMAND – PAYLOAD TIMING

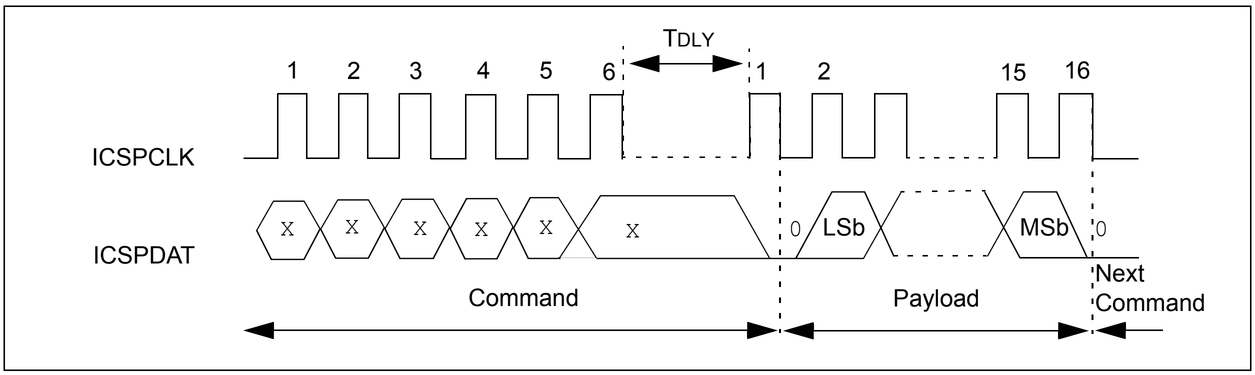


FIGURE 8-7: READ COMMAND – PAYLOAD TIMING

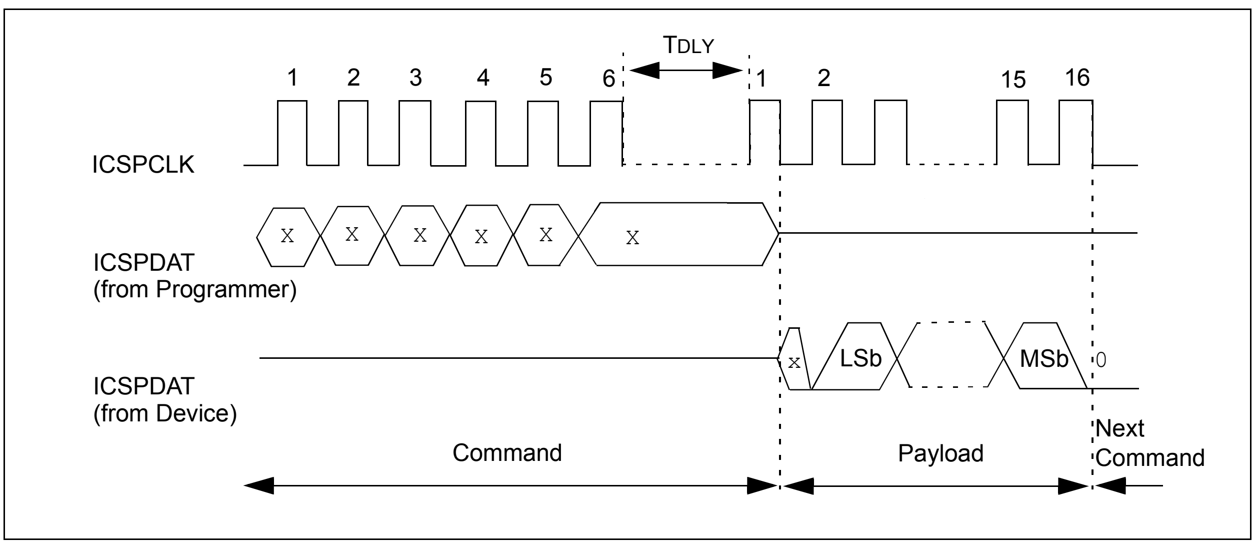


FIGURE 8-8: LVP ENTRY (POWERING-UP)

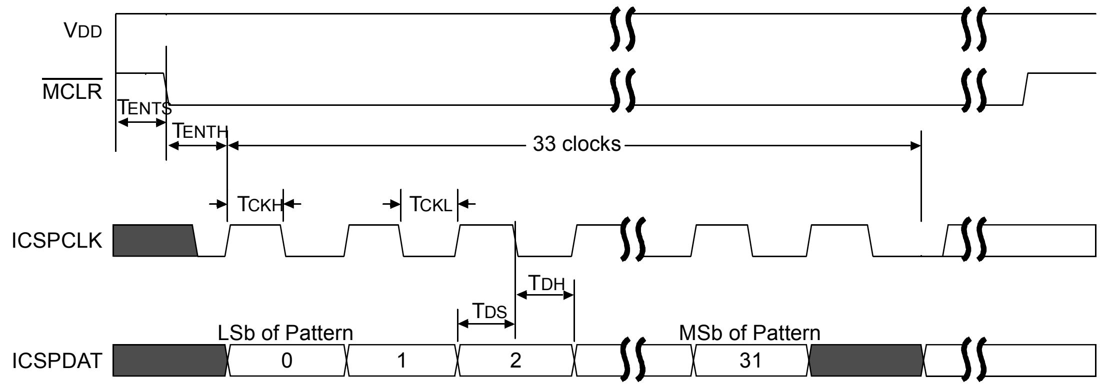
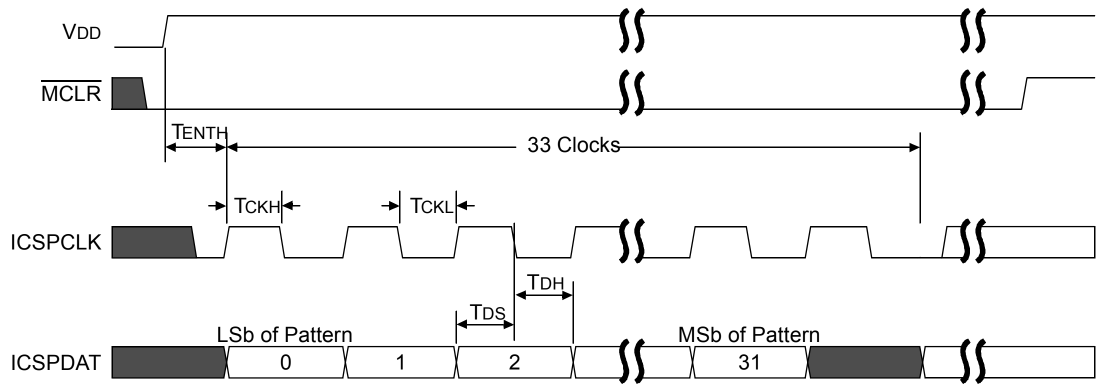


FIGURE 8-9: LVP ENTRY (POWERED)



Note: Sequence matching can start with no edge on $\overline{\text{MCLR}}$ first.

APPENDIX A: REVISION HISTORY

Revision A (05/2014)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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