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How to Configure the Memory Protection Unit (MPU)

Introduction

The Memory Protection Unit (MPU) is an optional component provided by the Cortex®-M7 core for memory protection. It divides the memory map into a number of regions with privilege permissions and access rules. This document is intended to familiarize the user with the configuration of the memory regions of the MPU, which is provided by Microchip's Cortex-M7 based MCUs.

Features of the MPU are as follows:

- Prevents an untrusted application from accessing protected memory regions for the purpose of intellectual property infringement.
- Prevents user applications from corrupting data used by the operating system.
- Separates data between processing tasks by blocking tasks from accessing other data.
- Allows memory regions to be defined as read-only so that vital data can be protected.
- Detects unexpected memory access.

In brief, the MPU provides,

- Memory protection
- Peripheral protection
- Privileged code access protection

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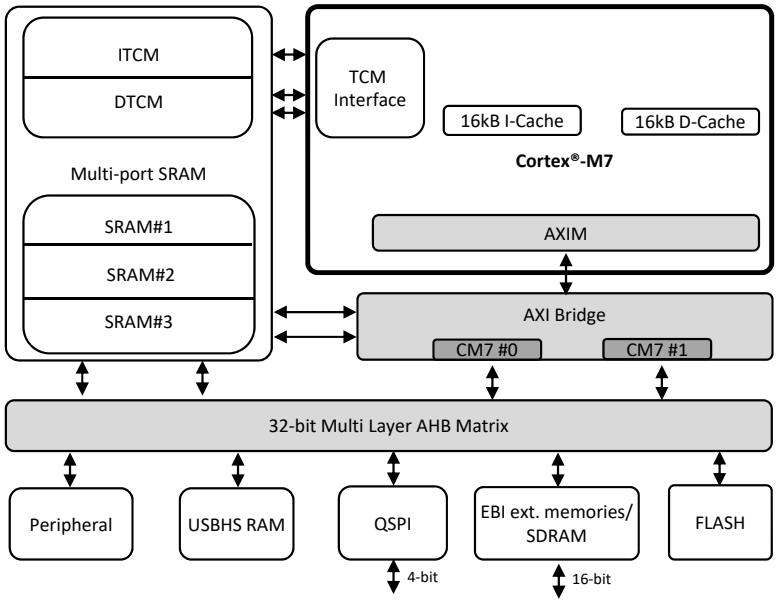
1. MPU of the Cortex-M7

The MPU option provided by the Cortex-M7 devices can be used to protect from eight to sixteen memory regions in the system space.

The Cortex-M7 based MCU's memory interface based on the MPU regions is shown in the following figure. For details on the product specific memory mapping, refer to the specific device data sheet.

Figure 1-1. Memory Interface of a Cortex-M7 based MCU



The functions provided with the MPU are based on the memory unit of region. A region is a part of the memory map with individual access rules. The memory type and attributes determine the behavior of the access to a region.

Each memory region can have an independent attribute setting. When memory regions overlap, memory access is affected by the attributes of the region with the highest number (i.e., the attributes for region 7 take precedence over the attributes of any region that overlaps region 7).

The configuration of MPU regions is based on memory types, memory regions, types, and attributes.

The MPU contains a number of registers. For the list of Cortex-M7 MPU registers, please visit: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0646a/BIHJJABA.html.

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2. Setting up the MPU in a Cortex-M7 MCU

The system should have the following memory types:

- *Normal*: refers to data or code memory space such as, Flash or SRAM
- *Device*: refers to memory mapped peripherals such as, USBHSRAM
- *Strongly-ordered*: refers to memory whose access always follows the program order (i.e., EBI, TCM)

The memory region should have the following attributes:

- Shareable or non-shareable (S)
- Cacheable or non-cacheable (C)
- Memory access permission (AP)
- Access for Instruction Fetch (XN)
- TEX and B are other bit-fields, which in combination with the above bit-fields, define the memory attribute for each MPU memory region

Figure 2-1. Memory Region Attributes

Memory Region	Memory Access Attribute; Shareable bit	Access Permission; Instruction Access
#1 ITCM	Strongly Ordered; Shareable	RW access from privileged SW only; Instruction fetches enabled
#2 FLASH	Normal; Not shareable; Cacheable; Inner Write back; no write allocate	Read only, by privileged or unprivileged SW; Instruction fetches enabled
#3 DTCM	Strongly Ordered; Shareable	RW access from privileged SW only; Instruction fetches enabled
#4 SRAM #1	Normal; Not shareable; Cacheable; Inner Write back; no write allocate	RW full access; Instruction fetches enabled
#5 SRAM #2	Normal; Not shareable; Cacheable; Inner Write back; no write allocate	RW full access; Instruction fetches enabled
#6 PERIPHERAL	Device; Shareable	RW full access; Instruction fetches disabled
#7 EXTERNAL	Strongly Ordered; Shareable	RW full access; Instruction fetches enabled
#8 SDRAM	Normal; Shareable; Cacheable; Inner write back; write and read allocate	RW full access; Instruction fetches enabled
#9 QSPI	Strongly Ordered; Shareable	RW full access; Instruction fetches enabled
#10 USBHS	Device; Shareable	RW full access; Instruction fetches disabled
#11 SRAM #3	Normal, Shareable, Outer and inner non-cacheable	RW full access; Instruction fetches enabled

For more information on the attribute bit-fields, please visit: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dai0179b/CHDFDFIG.html.

The memory mapping of a Cortex-M7 based MCU defines the general memory spaces. Each memory space has a definite memory type in logical operations. This is the default value for the memory type bits in the MPU region attribute register and also the basic design principle of a MPU system.

The basic memory access behaviors for a Cortex-M7 based MCU are listed in Memory Region Attributes. All the region attributes for the memory type must follow this table. For example, the peripheral region can never be set as a non-XN type, and it is always set as device type, non-cacheable, and non-executable.

Software Implementation

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The MPU registers need to be programmed and enabled before use. This is usually done in the initialization phase of any application running on the target MCU, after the system startup.

The MPU configuration involves the following three-step operation:

1. Select the memory region.
2. Configure the attributes for the selected memory region (TEX, S, C, B, AP, XN).
   – Repeat above two steps for all valid memory regions
3. Enable MPU.

If access is gained to an area of memory without the required permissions, a memory management fault is raised. The memory management fault exception must be set before enabling the MPU module. If any illegal access is detected, the system will enter the memory management fault handler.

The System Handler Control and State Register (SHCSR) of the System Control Block (SCB) is used to enable the MemManage Fault exception. For more details, please visit: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0646a/CIHFDJCA.html.

Flow Diagram

The following flowchart briefly explains the steps involved for setting up the MPU regions.

1. Select the MPU region using the MPU->RNR register.
2. Write the base address of the MPU region selected by the MPU->RNR to MPU->RBAR register.
3. Write the attributes of the MPU region selected by the MPU->RNR to MPU->RASR register.
4. Enable MPU in the MPU->CTRL register.

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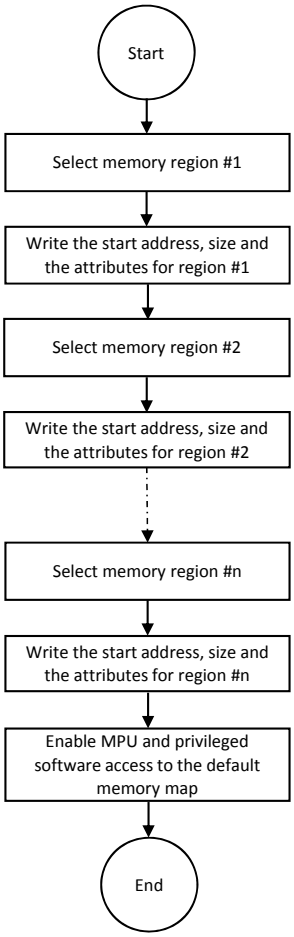
Figure 2-2. MPU Configuration Flow



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3. MPU Region Update

The MPU region attribute can be updated at run-time to satisfy different requirements. To update the attribute of a region, consider the following actions:

- The region must be disabled before changing the attributes.
- To avoid unexpected behavior, the interrupt routine must be disabled before the update.
- The access to the MPU registers should be aligned. A DSB and ISB instruction are required before updating the MPU, which ensures that the outstanding memory transfers are finished. The memory barrier instructions are not required if the update procedure happens in an exception handler, as the memory barrier behavior will automatically take place in an exception entry and return.

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4. MPU Setup Tips

Tip:

1. The processor does not support unaligned accesses to MPU registers. The MPU registers support aligned word accesses only.
2. If the MPU has previously been programmed, disable the unused regions to prevent any previous region settings from affecting the new MPU setup.
3. Disable the interrupts before updating the attributes of a region that the interrupt handlers might access.

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5. References

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