
USB to SPI Bridging with Microchip USB 3.1 Gen 1 Hubs

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INTRODUCTION

The USB to SPI bridging feature of Microchip hubs provides system designers with expanded system control and potential BOM reductions. When using Microchip's USB hubs, a separate USB to SPI device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SPI device is implemented. This feature is available on the Microchip USB5734 and USB58xx/USB59xx USB3.1 Gen 1 Hubs.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable/Disable SPI Pass-Through Interface
- SPI Write
- SPI Read

SECTIONS

[Section 1.0, General Information](#)

[Section 2.0, Part Number Specific Information](#)

[Section 3.0, ProTouch2 DLL Implementation](#)

[Section 4.0, Manual Implementation](#)

REFERENCES

Consult the following documents for details on the specific parts referred to in this document:

- *Microchip USB5734 Data Sheet*
- *Microchip USB5806 Data Sheet*
- *Microchip USB5816 Data Sheet*
- *Microchip USB5826 Data Sheet*
- *Microchip USB5906 Data Sheet*
- *Microchip USB5916 Data Sheet*
- *Microchip USB5926 Data Sheet*
- *Microchip AN1903 Configuration Options for the USB5734 and USB5744*
- *Microchip AN2316 Configuration Options for the USB58xx and USB59xx*

1.0 GENERAL INFORMATION

Microchip hub USB Bridging features in Microchip hubs work via host commands sent to a Hub Feature Controller embedded within the hub located on an additional internal USB port. In order for the bridging features to work correctly, this internal Hub Feature Controller must be enabled by default. Table 1 provides details on default Hub Feature Controller settings by device.

TABLE 1: DEFAULT SETTINGS FOR THE HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Feature Controller Default Setting
USB5734	4-Port USB3.1 Gen 1 Hub	Enabled by default
USB5806	6-Port USB3.1 Gen1 Hub	Enabled by default
USB5816	6-Port USB3.1 Gen1 Hub with Type-C™ Support on 1 Downstream Port	Enabled by default
USB5826	6-Port USB3.1 Gen1 Hub with Type-C Support on 2 Downstream Ports	Enabled by default
USB5906	6-Port USB3.1 Gen1 Hub with Type-C Support on the Upstream Port	Enabled by default
USB5916	6-Port USB3.1 Gen1 Hub with Type-C Support on the Upstream Port and 1 Downstream Port	Enabled by default
USB5926	6-Port USB3.1 Gen1 Hub with Type-C Support on the Upstream Port and 2 Downstream Ports	Enabled by default

The Hub Feature Controller is a USB2.0 WinUSB class device connected to an extra internal USB port in the hub. For example, in a four port hub, the Hub Controller is connected to port 5 of the USB2.0 portion of the hub. The Product ID (PID) for the Hub Controller is 0x2740. All bridging commands are addressed to the Hub Controller, not the Hub.

FIGURE 1-1: MICROCHIP HUB CONTROLLER EXAMPLE

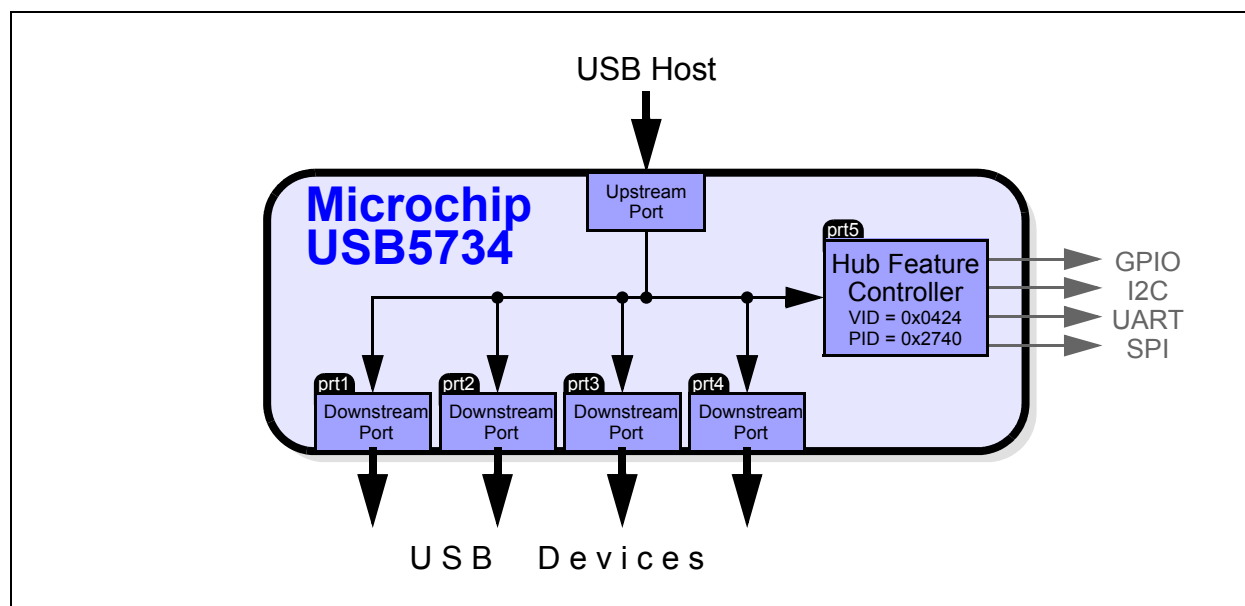
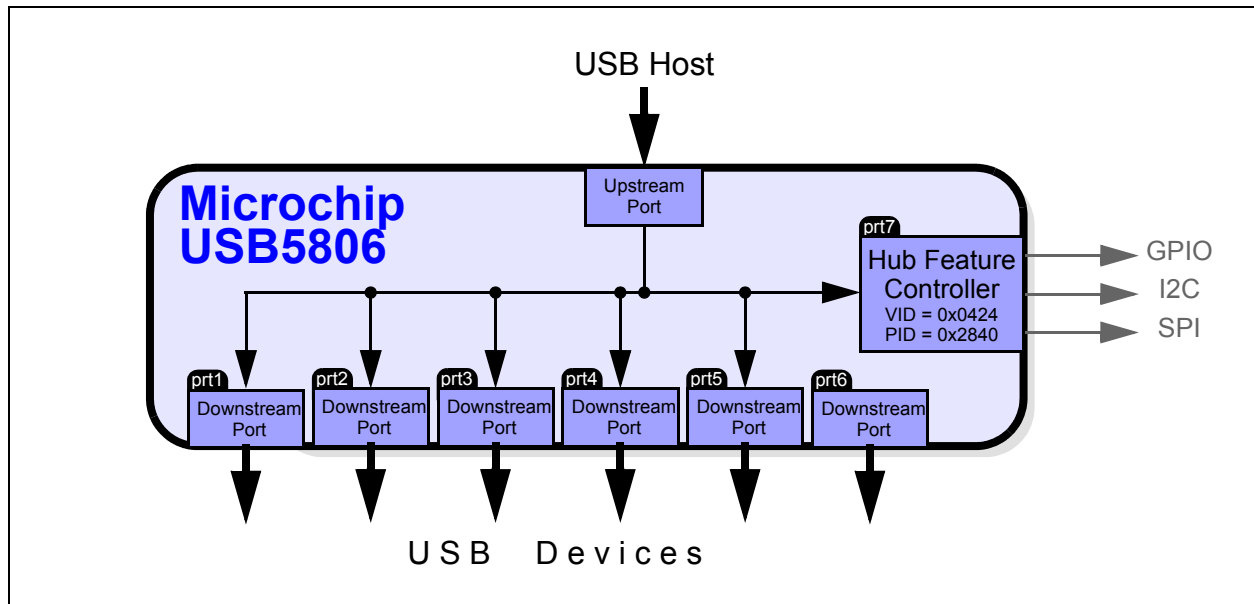


FIGURE 1-2: MICROCHIP HUB CONTROLLER EXAMPLE



1.1 SPI Bridging Commands

The following SPI Functions are supported:

- Enable/Disable SPI Pass-Through Interface
- SPI Write
- SPI Read

1.1.1 ENABLE/DISABLE THE SPI PASS-THROUGH INTERFACE

A single command to enable the SPI interface is required before performing any SPI Write or Read commands. The SPI interface operates at 60 Hz. The SPI interface may be disabled after writing/reading to the device is complete.

1.1.2 SPI WRITE/(READ)

The SPI interface works as a complete pass-through. This means that the host must properly arrange data payloads in the appropriate SPI compatible format and bit order, including the SPI slave device address. Up to 256 Bytes of data payload may be sent per SPI write command sequence.

Data may also be read from a SPI device via the SPI Write command. Up to 512 bytes of data may be read from the SPI device per read. The read data is stored in the internal registers of the hub starting at register 0x4A10. To retrieve the data, you must use a USB to Register Read command. Further details can be found in *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*.

1.2 SPI Interface Setup Requirements

1.2.1 SPI MASTER INTERFACE

The SPI Interface always acts as a SPI master.

1.2.2 SPI MODES OF OPERATION

Both SPI Modes 0 and 3 are supported:

- Mode 0: Clock Polarity = 0, Clock Edge = 1
- Mode 3: Clock Polarity = 1, Clock Edge = 0

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Dual Output Enable mode is also supported.

The default mode of operation is Mode 0 with Dual Output Enable mode disabled. If the mode of operation is to be modified, a register write to the SPI_CTL register must be performed. See *Microchip AN1903 Configuration Options for the USB5734 and USB5744* or *Microchip AN2316 Configuration Options for the USB58xx and USB59xx* for details on how to modify that register.

2.0 PART NUMBER SPECIFIC INFORMATION

2.1 Part Summary

The following tables display the SPI interface pins by part number as well as any notes on those pins.

2.2 USB5734

TABLE 2: USB5734 SPI INTERFACE PINS

Pin #	Name	Notes
42	SPI_CLK/(I2C_SLCV_CFG0)	SPI Clock (60 MHz) I2C_SLV_CFG0 strap is sampled at power on and it must have no pull-up/down resistors detected at power on to enter SPI Mode
43	SPI_DO/(I2C_SLCV_CFG1)	SPI Data Out I2C_SLV_CFG1 strap is sampled at power on and it must have no pull-up/down resistors detected at power on to enter SPI Mode
44	SPI_DI	SPI Data In
45	SPI_CE_N	SPI Chip Enable

2.3 USB58xx/USB59xx

TABLE 3: USB58XX/USB59XX I2C INTERFACE PINS

Pin #	Name	Notes
65	SPI_CLK/C_ATTACH3/GPIO4	SPI Clock (60 MHz) When implementing the SPI bridging feature, the hub should not be configured for Type-C operation on Downstream Ports 2 or 3.
66	SPI_DO/C_ATTACH2/GPIO5	SPI Data Out When implementing the SPI bridging feature, the hub should not be configured for Type-C operation on Downstream Ports 2 or 3.
67	SPI_DI/GPIO9/ <u>CFG_BC_EN</u>	SPI Data In This pin is also used as the Battery Charging configuration strap. It is generally not recommended to use this configuration strap when implementing the SPI bridging feature.
68	SPI_CE_N/GPIO7/ <u>CFG_NON_REM</u>	SPI Chip Enable This pin is also used as the Port Non-Removable configuration strap. It is generally not recommended to use this configuration strap when implementing the SPI bridging feature.

3.0 PROTOUCH2 DLL IMPLEMENTATION

The simplest method for implementing the USB to SPI bridging functions is to use the publicly available ProTouch2 DLL library. The PT2 DLL library is available for Windows operating systems. Visit the product page for any of the hubs listed in this document on microchip.com to download the ProTouch2 package. Using the libraries available in the ProTouch2 DLL library, the bridging features can be implemented in C-code.

The PT2 DLL library package contains the following:

- ProTouch2 DLL User Guide: Detail description of how to use the SDK and call each function
- ProTouch2 Release Notes:
- Library Files:
 - For Windows: A “.dll” and a “.lib” file
- Example code

3.1 Commands included in the DLL Library

- **MchpUsbSpiSetConfig:** Enables or Disables the SPI interface.
- **MchpUsbSpiFlashWrite:** Write up to 255 Bytes of data to an SPI slave device.
- **MchpUsbSpiFlashRead:** Read up to 255 Bytes of data from an SPI slave device.
- **MchpUsbSpiFlashRead:** Read/Write from a SPI slave device.

For additional details on how to use the PT2 DLL library to implement USB to SPI bridging, download the ProTouch2 package and read the User's Manual.

4.0 MANUAL IMPLEMENTATION

The USB to SPI bridging features may be implemented at the lowest level if you have the ability to build USB packets. This approach is required if you are not using a Windows or Linux host system and cannot use the ProTouch2 DLL library.

The details of the SPI pass-through control packets are shown below.

4.1 Enable SPI Pass-Through Interface Command

The follow SETUP packet command is required to enable the SPI pass-through interface. The interface must be enabled before any Write or Read commands may be performed. Note that there is no data phase to this USB transaction,

TABLE 4: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x60	Register read command: CMD_SPI_ENTER_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x00	No data stage

4.2 SPI Write Command

This command is used to write data to or read data from a SPI peripheral connected to the USB hub.

TABLE 5: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x61	Register read command: CMD_SPI_WRITE
wValue	0xFFFF	The total length of data to be sent to the SPI peripheral (the size of the data following the SETUP packet).
wIndex	0x0000	Reserved
wLength	0xNN	The number of bytes the SPI interface will return for the command sent

The maximum amount of data that can be read from one USB command is 512 Bytes by specifying wValue = 517 and wLength = 5.

The maximum amount of data that can be written to a SPI peripheral is 256 Bytes by specifying wValue = wLength = 260.

4.2.1 SPI WRITE USB TRANSACTION SEQUENCE:

1. SETUP PACKET: To send 'Write Enable' OpCode to SPI ROM (wValue = wLength = 1)
2. DATA: 0x06 (opcode for 'Write Enable').
3. STATUS: An IN-Zero Length Packet is sent from hub.
4. SETUP PACKET: To send data payload
5. DATA: EP0 Data to SPI ROM with 0x02 + 24bit SPI address + Data Stream
6. STATUS: If an IN-Zero Length Packet is sent from hub, transfer was a success. If an IN-STALL packet is sent from hub, there was an error during transfer.

4.2.2 SPI READ USB TRANSACTION SEQUENCE:

1. SETUP PACKET: As defined above.
2. DATA: EP0 OUT Data to SPI ROM with 0x0B + 24Bit SPI Address + 0x00 (dummy byte).
3. STATUS: If an IN-Zero Length Packet is sent from hub, transfer was a success. If an IN-STALL packet is sent from hub, there was an error during transfer, likely due to missing ACK from the SPI slave.
4. Perform Configuration Register Read on hub starting at register 0x4A10 to retrieve read data. See *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*

4.3 Disable SPI Pass-Through Interface Command

The follow SETUP packet command is required to enable the SPI pass-through interface. Note that there is no data phase to this USB transaction,

TABLE 6: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x62	Register read command: CMD_SPI_ENTER_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x00	No data stage

5.0 EXAMPLES

5.1 Write 512 Bytes to a SPI ROM

1. Enable the SPI Pass-Through Interface

TABLE 7: ENABLE SPI INTERFACE SETUP COMMAND

Setup Parameter	Value
bmRequestType	0x41
bRequest	0x60
wValue	0x0000
wIndex	0x0000
wLength	0x00

2. Send a SPI Write/Read Command to read 512 Bytes of data.

TABLE 8: SPI WRITE SETUP COMMAND

Setup Parameter	Value
bmRequestType	0x41
bRequest	0x61
wValue	0x0205 (517)
wIndex	0x0000
wLength	0x0005

3. EP0 OUT data = 0x0B, 0xXX, 0xYY, 0xZZ, 0x00, 0xXX, 0xYY, 0xZZ.

Note: 0xXX, 0xYY, 0xZZ is the 24 Bit physical SPI address of the SPI peripheral.

4. Read response via USB to Configuration Register Read from register 0x4A10. Further details can be found in *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*.
5. Do one of the following:
 - Close the SPI Interface with the Disable SPI Pass-Through Command
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

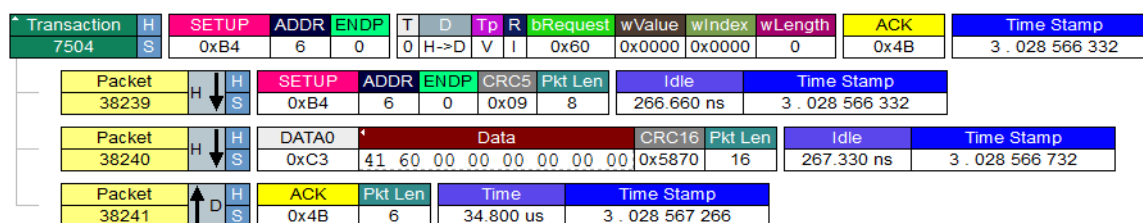
5.2 Enable the SPI Pass-Through Interface

1. **Command Phase (SETUP Transaction):** Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller to enable the SPI pass-through interface:

TABLE 9: EXAMPLE I2C WRITE SETUP PACKET

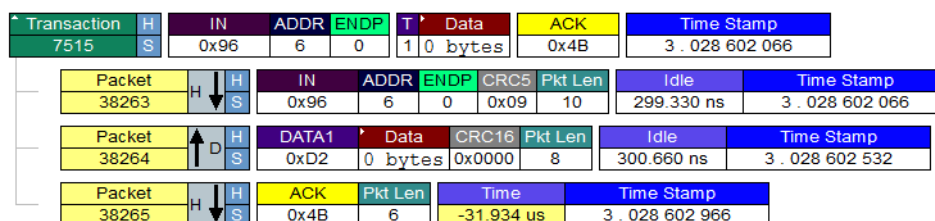
Field	Value	Note
bmRequestType	0x41	
bRequest	0x60	
wValue	0x0000	
wIndex	0x0000	
wLength	0x0000	

FIGURE 1: SETUP TRANSACTION EXAMPLE



2. **Status (IN Transaction):** The host sends an IN packet to the Hub Feature Controller, to which the Hub Feature controller replies with a zero data length packet. The host ACKs to complete the bridging command.

FIGURE 2: IN TRANSACTION EXAMPLE



5.3 Read the JEDEC ID from an attached SPI Device

- Command Phase 1 (SETUP Transaction 1):** The JEDEC ID gives manufacturer information and memory information. This example shows how to read the JEDEC ID from an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller send a SPI Write command to the attached SPI device.

TABLE 10: SPI JEDEC ID READ SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0001	
wIndex	0x0000	
wLength	0x0004	

FIGURE 3: SPI JEDEC ID READ SETUP TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	TP	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
3465	S	0xB4	7	0	0	H→D	V	I	0x61	0x0001	0x0000	4	0x4B	1 . 404 729 532

Packet	H	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
17616	H	S	0xB4	7	0	0x16	8	300.660 ns	1 . 404 729 532

Packet	H	H	DATA0	Data				CRC16	Pkt Len	Idle	Time Stamp				
17617	H	S	0xC3	41	61	01	00	00	00	04	00	0x90FB	16	267.330 ns	1 . 404 729 966

Packet		D	ACK	Pkt Len	Time	Time Stamp
17618	H	S	0x4B	6	10.666 us	1 . 404 730 500

- Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by the data bytes of length wLength. In this example, the 0x9F data is the opcode for reading a JEDEC ID in a SPI device. Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 4: SPI JEDEC ID IN TRANSACTION EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	D	TP	R	Data	NYET	Time Stamp
3469	S		0x87	7	0	1	4 bytes		0x69		1 . 404 744 432
Packet		H	OUT	ADDR	ENDP	CRC5	Pkt Len		Idle		Time Stamp
17626	H	S	0x87	7	0	0x16	10		267.330 ns		1 . 404 744 432
Packet		H	DATA1			Data	CRC16	Pkt Len	Idle		Time Stamp
17627	H	S	0xD2	9F	00 00 00 00	0x8BF3	14		300.660 ns		1 . 404 744 866
Packet		H	NYET	Pkt Len		Time		Time Stamp			
17628	H	S	0x69	6		44.532 us		1 . 404 745 400			

- Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 5: SPI JEDEC ID OUT TRANSACTION EXAMPLE

Transaction	H	IN	ADDR	ENDP	T	D	TP	R	Data	ACK	Time Stamp
3485	S		0x96	7	0	1	0 bytes		0x4B		1 . 404 789 932
Packet		H	IN	ADDR	ENDP	CRC5	Pkt Len		Idle		Time Stamp
17659	H	S	0x96	7	0	0x16	8		334.660 ns		1 . 404 789 932
Packet		H	DATA1			Data	CRC16	Pkt Len	Idle		Time Stamp
17660	H	S	0xD2	0 bytes	0x0000	8		298.660 ns			1 . 404 790 400
Packet		H	ACK	Pkt Len		Time		Time Stamp			
17661	H	S	0x4B	6		-55.632 us		1 . 404 790 832			

4. **Retrieve the Returned Data (SETUP Transaction 2):** The SPI device will respond to the opcode command and the returned data will be stored in the hub's internal register starting at address 0x4A10. A USB to Register Read command can retrieve the data. This command is setup as:

TABLE 11: SPI JEDEC ID REGISTER READ SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0xC1	
bRequest	0x04	
wValue	0x4A10	The hub's internal register address
wIndex	0x0000	
wLength	0x0004	A JEDEC ID request will return 4 bytes. The first byte will be a dummy 0x00.

FIGURE 6: SPI JEDEC ID REGISTER READ SETUP TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	TP	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
3486	S	0xB4	7	0	0	D→H	V	I	0x04	0x4A10	0x0000	4	0x4B	1 . 404 967 332
Packet	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp						
17664	S	0xB4	7	0	0x16	10	267.330 ns	1 . 404 967 332						
Packet	H	DATA0	Data				CRC16	Pkt Len	Idle	Time Stamp				
17665	S	0xC3	C1	04	10	4A	00	00	04	00	0x756C	16	267.330 ns	1 . 404 967 766
Packet	H	ACK	Pkt Len	Time	Time Stamp									
17666	S	0x4B	6	25.300 us	1 . 404 968 300									

5. **Data Phase 2 (IN Transaction 2):** Host sends an IN packet to retrieve the data from the 0x4A10 register. In this example, the JEDEC ID that is returned is 0xBF, 0x25, 0x4B. The host replies with an ACK after receiving the data.

FIGURE 7: SPI JEDEC ID REGISTER READ IN TRANSACTION EXAMPLE

Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time Stamp
3495	S	0x96	7	0	1	4 bytes	0x4B	1 . 404 993 600

Packet	H	IN	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
17683	S	0x96	7	0	0x16	8	332.660 ns	1 . 404 993 600

Packet	D	DATA1	Data			CRC16	Pkt Len	Idle	Time Stamp	
17684	S	0xD2	00	BF	25	4B	0x2919	12	300.000 ns	1 . 404 994 066

Packet	H	ACK	Pkt Len	Time	Time Stamp
17685	S	0x4B	6	2.300 us	1 . 404 994 566

6. **Status Phase 2 (OUT Transaction 2):** Host sends an OUT packet followed by a zero length data packet. The Hub Feature Controller ACKs to complete the bridging command.

FIGURE 8: SPI JEDEC ID REGISTER READ OUT TRANSACTION EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time Stamp
3497	S	0x87	7	0	1	0 bytes	0x4B	1 . 404 999 366

Packet	H	H	OUT	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
17688	S	↓	0x87	7	0	0x16	8	300.660 ns	1 . 404 999 366

Packet	H	H	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp
17689	S	↓	0xD2	0 bytes	0x0000	8	298.660 ns	1 . 404 999 800

Packet	H	D	ACK	Pkt Len	Time	Time Stamp
17690	S	↑	0x4B	6	-28.532 us	1 . 405 000 232

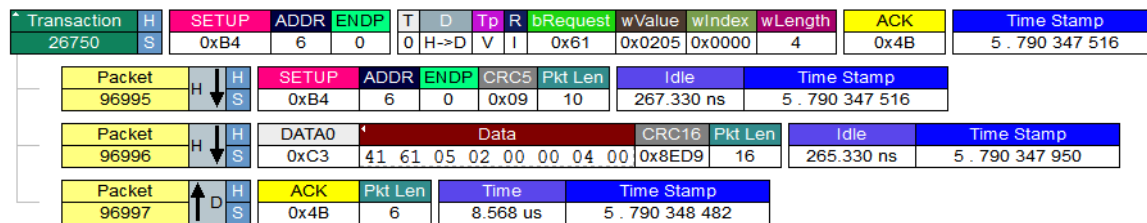
5.4 Read 512 Bytes from an attached SPI Device

1. **Command Phase 1 (SETUP Transaction 1):** This example shows how to perform a block read of 512 bytes (the maximum number of bytes per command) from an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller send a SPI Write command to the attached SPI device

TABLE 12: SPI BLOCK READ COMMAND SETUP PACKET EXAMPLE

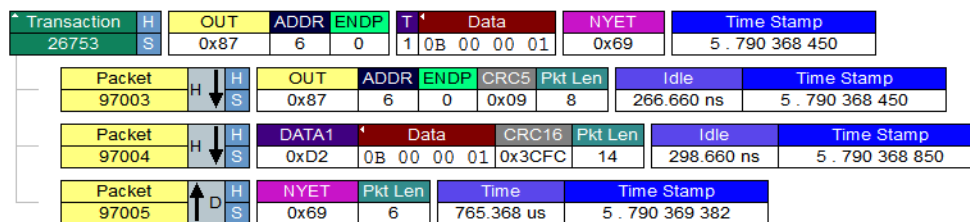
Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0205 (517)	The first 5 Bytes of any SPI read must be ignored; Therefore, 5 must be added to the number of Bytes to be read.
wIndex	0x0000	
wLength	0x0004	

FIGURE 9: SPI BLOCK READ COMMAND SETUP TRANSACTION EXAMPLE



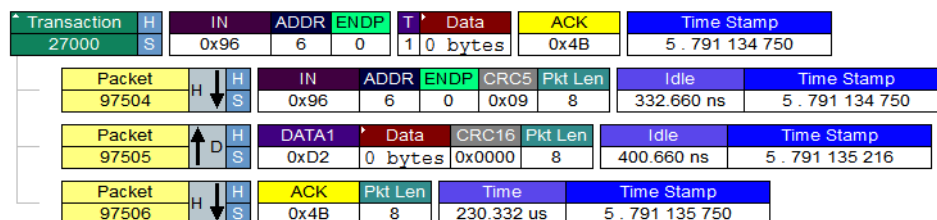
2. **Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by the data bytes of length wLength. In this example, the 0x0B is the opcode for a block read in this specific SPI device, the next 0x00,0x00,0x01 is the register address to begin reading from the SPI device. The Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 10: SPI BLOCK READ COMMAND IN TRANSACTION EXAMPLE



3. **Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 11: SPI BLOCK READ COMMAND OUT TRANSACTION EXAMPLE

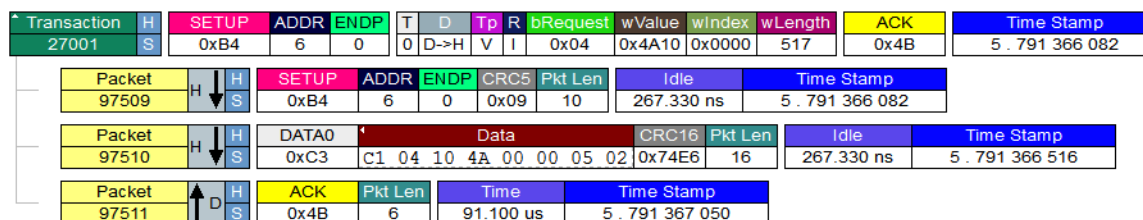


4. **Retrieve the Returned Data (SETUP Transaction 2):** The SPI device will respond to the opcode command and the returned data will be stored in the hub's internal register starting at address 0x4A10. For a SPI Block Read, the first 5 bytes must be ignored. A USB to Register Read command can retrieve the data. This command is setup as:

TABLE 13: REGISTER READ SETUP PACKET EXAMPLE

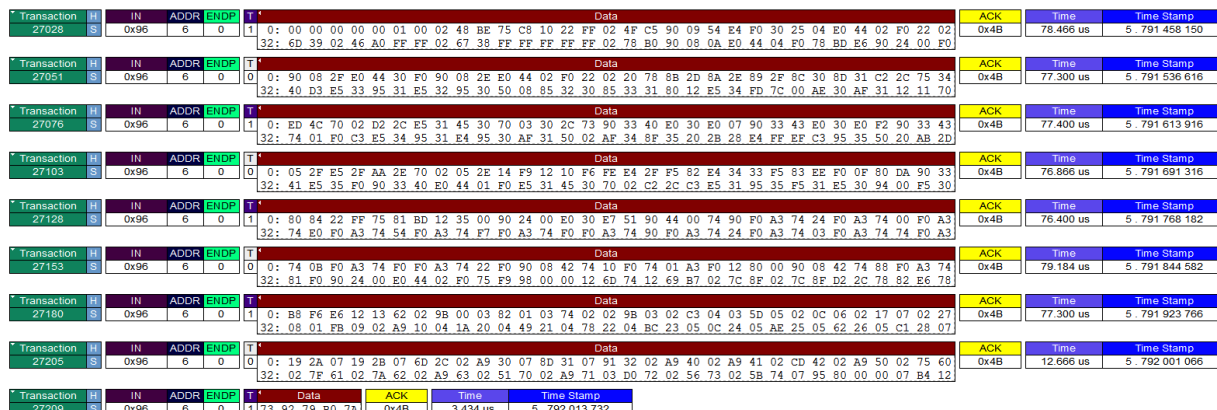
Field	Value	Note
bmRequestType	0xC1	
bRequest	0x04	
wValue	0x4A10	The hub's internal register address
wIndex	0x0000	
wLength	0x0205	517 Bytes will be read (512 + 5 dummy bytes)

FIGURE 12: REGISTER READ SETUP TRANSACTION EXAMPLE



5. **Data Phase 2 (IN Data Payload Transaction):** Hub sends a series of IN packets (64 Bytes per packet) until all 517 bytes are read. The first 5 bytes should always be ignored.

FIGURE 13: REGISTER READ IN TRANSACTION EXAMPLE



6. **Status Phase 2 (OUT Transaction 2):** Host sends an OUT packet followed by a zero length data packet. The Hub Feature Controller ACKs to complete the bridging command.

FIGURE 14: REGISTER READ OUT TRANSACTION EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time Stamp	
27211	S	0x87	6	0	1	0 bytes	0x4B	5 . 792 019 800	
Packet	H	OUT	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp	
97942	S	0x87	6	0	0x09	8	266.660 ns	5 . 792 019 800	
Packet	H	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp		
97943	S	0xD2	0 bytes	0x0000	8	332.660 ns	5 . 792 020 200		
Packet	D	ACK	Pkt Len	Time	Time Stamp				
97944	S	0x4B	6	2.165 sec	5 . 792 020 666				

7. After completing the SPI Read, do one of the following:
 - Close the SPI Interface with the Disable SPI Pass-Through command.
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

5.5 Write 256 Bytes to an attached SPI Device

1. **Command Phase 1 (SETUP Transaction 1):** This example shows how to perform a block write of 256 bytes to an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller to enable the SPI write feature.

TABLE 14: SPI WRITE ENABLE SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0001	
wIndex	0x0000	
wLength	0x0001	

FIGURE 15: SPI WRITE ENABLE SETUP TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	TP	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
98000	S	0xB4	6	0	0	H→D	V	I	0x61	0x0001	0x0000	1	0x4B	19 . 101 512 616

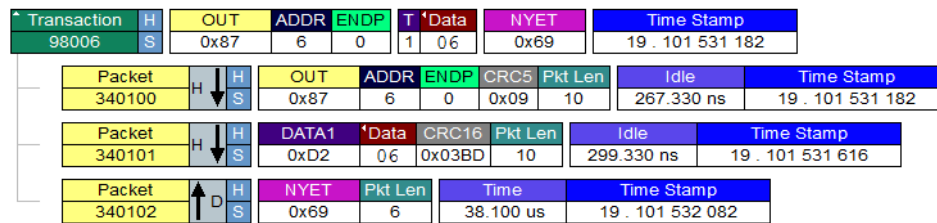
Packet	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
340086	S	0xB4	6	0	0x09	10	267.330 ns	19 . 101 512 616

Packet	H	DATA0	Data				CRC16	Pkt Len	Idle	Time Stamp				
340087	S	0xC3	41	61	01	00	00	00	01	00	0x50F1	16	265.330 ns	19 . 101 513 050

Packet	D	ACK	Pkt Len	Time	Time Stamp
340088	S	0x4B	6	14.200 us	19 . 101 513 582

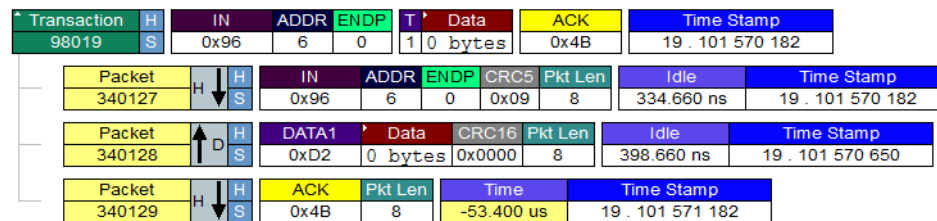
2. **Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by a single byte data payload of 0x06. 0x06 is the SPI write enable command. The Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 16: SPI WRITE ENABLE TRANSACTION EXAMPLE



3. **Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 17: SPI WRITE DATA OUT TRANSACTION EXAMPLE

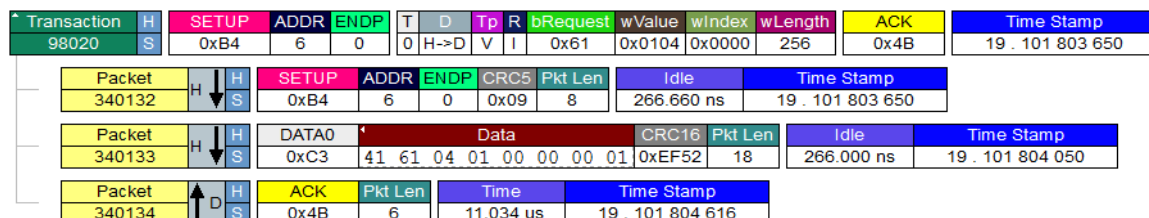


4. **Send the SPI Write Data Payload (SETUP Transaction 2):** The SPI device is now ready to receive the data payload. For a SPI Block Write of 256 bytes, the SETUP command is:

TABLE 15: SPI WRITE DATA SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0104 (260)	The 256 byte data payload + 4 extra command bytes
wIndex	0x0000	
wLength	0x0100 (256)	The 256 byte data payload

FIGURE 18: SPI WRITE DATA TRANSACTION EXAMPLE



5. **Data Phase 2 (OUT Data Payload Transaction):** Host sends a series of OUT packets (64 Bytes per packet) until all 256 + 4 command bytes are sent. The first 4 bytes must be 0x02, 0xXX, 0xYY, 0xZZ where 0xXX, 0xYY, 0xZZ is the 24 bit physical address of the SPI Flash. In this example, the SPI address is 0x111111.

FIGURE 19: SPI WRITE DATA OUT TRANSACTIONS EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data
98025	S	0x87	6	0	1	0: 02 11 11 11 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32: 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32
Transaction	H	OUT	ADDR	ENDP	T	Data
98050	S	0x87	6	0	0	0: 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F 70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F 80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
Transaction	H	OUT	ADDR	ENDP	T	Data
98072	S	0x87	6	0	1	0: 6C 6D 6E 6F 70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F 80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
Transaction	H	OUT	ADDR	ENDP	T	Data
98093	S	0x87	6	0	0	0: AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF

6. **Status Phase 2 (IN Transaction 2):** Host sends an IN packet and the hub responds with a zero length data packet. The Host ACKs to complete the bridging command.

FIGURE 20: SPI WRITE DATA IN TRANSACTION EXAMPLE

Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time Stamp	
98343	S	0x96	6	0	1	0 bytes	0x4B	19 . 102 743 066	
Packet	H	H	IN	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
340790	S	S	0x96	6	0	0x09	8	300.660 ns	19 . 102 743 066
Packet	H	D	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp	
340791	S	S	0xD2	0 bytes	0x0000	8	432.660 ns	19 . 102 743 500	
Packet	H	H	ACK	Pkt Len	Time	Time Stamp			
340792	S	S	0x4B	8	-935.950 us	19 . 102 744 066			

7. After completing the SPI Write, do one of the following:
- Close the SPI Interface with the Disable SPI Pass-Through command.
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001999B (12-07-16)	All	Fixed references to <i>AN2316 Configuration Options for the USB58xx and USB59xx</i> throughout.
		Trademark and Sales Listing pages updated.
		Updated minor formatting and grammar issues throughout.
DS00001999A (09-11-15)	All	Initial release.

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