Board Design Recommendations for ZL30151, ZL30169, ZL30281, ZL30622, ZL30722 and ZL3025x Devices

Introduction

This document is intended to provide circuit design and PCB layout guidelines for the ZL30151, ZL30169, ZL30250, ZL30251, ZL30252, ZL30253, ZL30622 and ZL30722 series of any-to-any clock multipliers, jitter attenuators, and telecom timing integrated circuits (ICs). This document also applies to the ZL30281 three Output PCIe Clock Generator

Power Supply

Jitter levels on the clock output of a timing device may increase if the device is exposed to noise on its power supply pins. For optimal jitter performance, the device should be isolated from noise on power planes as recommended by the Microsemi application notes relevant for that particular device. The recommendations in these application notes should cover most of the real life situations. In extremely noisy environments the user should consider linear regulators to generate the supply voltage for the timing device.

The application note ZLAN-490 is covering the power supply decoupling recommendations for ZL30151, ZL30169, ZL30250, ZL30251, ZL30252, ZL30253, ZL30281, ZL30622 and ZL30722 series.

The following section shows the application of ZLAN-490 recommendations to a ZL30251 design which has all output clock signals configured to use 3.3 V supply. A total of two power supply islands are required in this case.

The PCB placement and routing presented below are just for reference. Other valid implementations are possible as long as the main guidelines outlined below are followed.

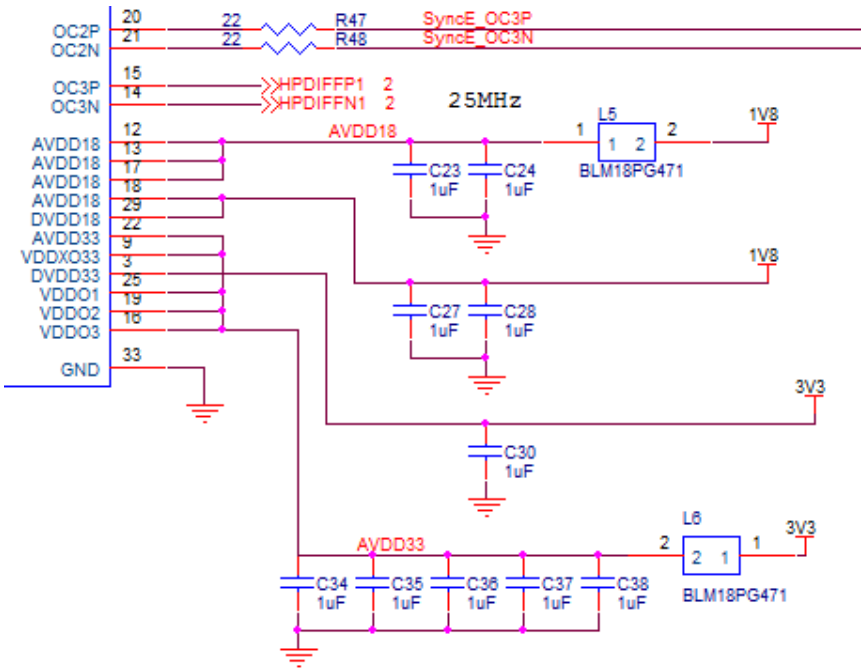

Figure 1 · ZL30251 Power Supply Decoupling Scheme Example

The ZL30251 device is located on the top layer (primary side) of the PCB. The breakout vias for the power supply pins (highlighted in the following picture) are placed as close as possible to the pins to minimize the length of the power supply routing to the internal power layers and to the decoupling capacitors placed on the bottom layer.

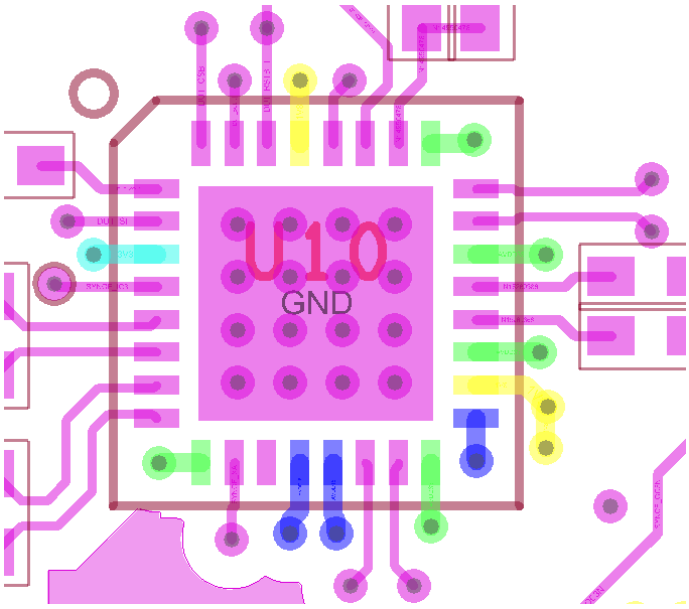

Figure 2 · ZL30251 Device Placed on the Top Layer of the PCB

All the decoupling capacitors are placed on the bottom layer of the PCB, with the 1uF capacitors placed beside the ZL30251 power supply breakout vias in order to minimize the distance to the timing device. In this example, the bottom layer is used also to route the AVDD18 power island.

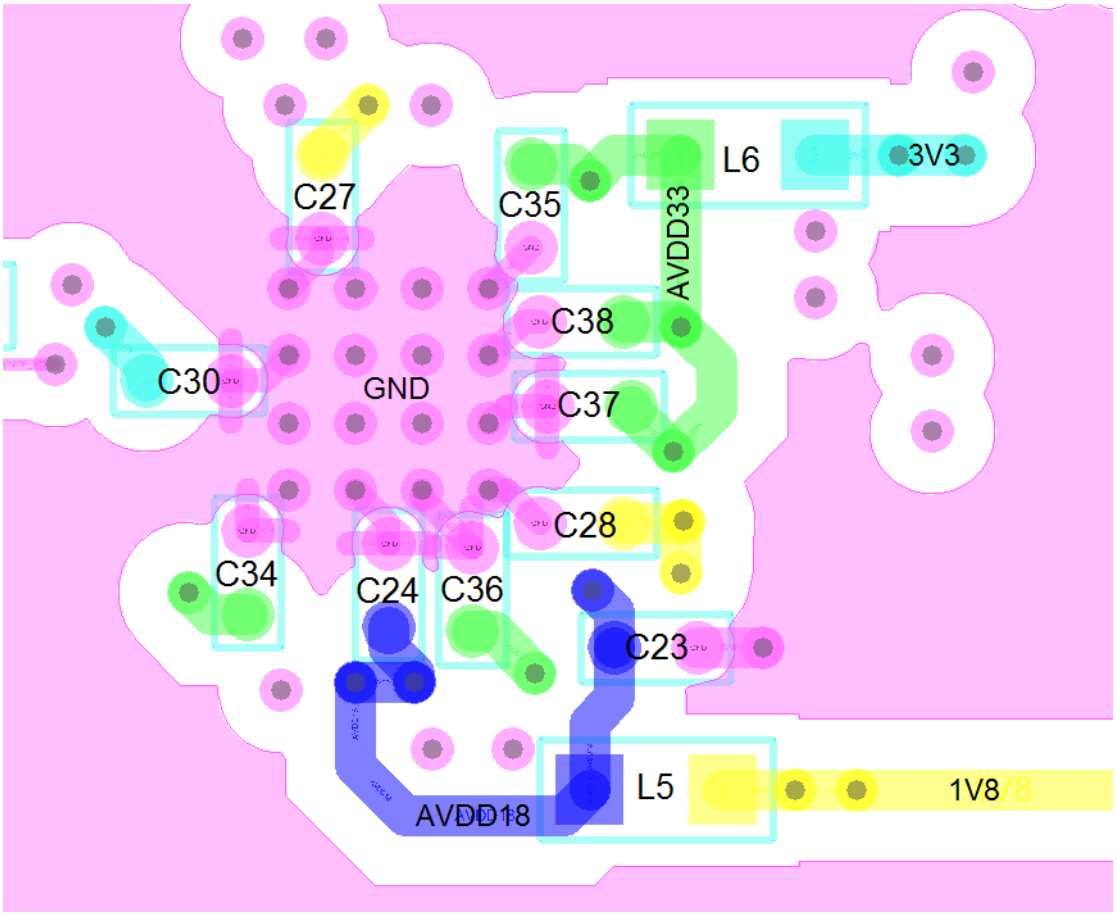

Figure 3 · Decoupling Placement on the Bottom Layer (through PCB view)

One internal layer is used to implement the AVDD33 power island and the distribution of 1.8V to pin 18 and 29.

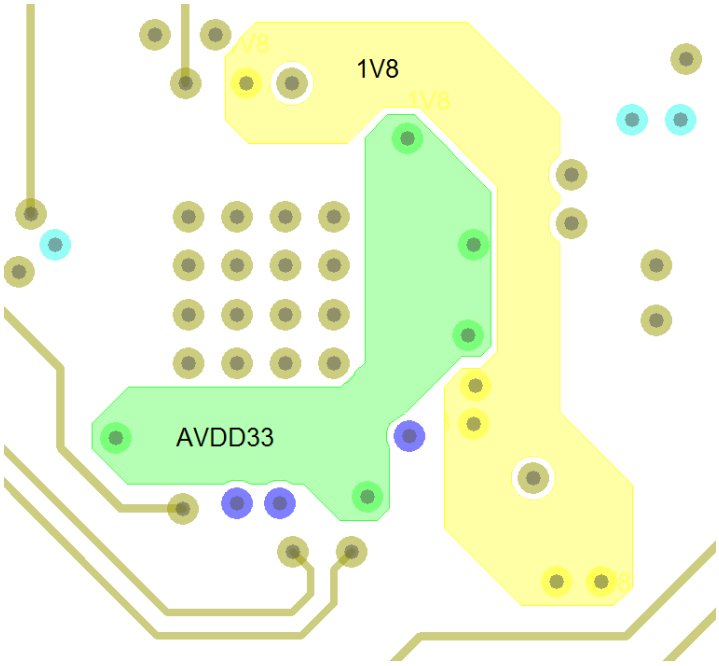

Figure 4 · Internal Layer Implementation of Power Supply Islands

Local Reference

ZL30151, ZL30169, ZL30250, ZL30251, ZL30252, ZL30253, ZL30281, ZL30622 and ZL30722 series devices can use an oscillator or a crystal as a local reference clock. This local reference clock is providing the internal system clock when the device is in DPLL mode or it can provide the reference clock used in APLL mode to synthesize the output clocks. In both cases the jitter on the output of the timing device is directly impacted by the jitter of this local reference clock. For this reason it is important to provide a low jitter local reference clock.

Application Note ZLAN-442 provides a list of crystals and oscillators for Microsemi next generation timing solutions.

Local Oscillator

Whenever possible select the highest recommended oscillator frequency. The higher the oscillator frequency the lower is the jitter on the output of the timing device.

As a general rule, the oscillator has to be placed on the PCB as close as possible to the timing device in order to minimize the length of the clock signal tracks and reduce the possibility of noise coupling from adjacent circuits. The signal trace should be properly terminated to minimize reflections.

Noise on the oscillator's power supply can dramatically increase the jitter on its output clock. The oscillator has to be supplied with a clean voltage in order to minimize the jitter caused by power supply noise.

LC filters are an effective way to filter noise with frequencies above 50-100KHz. For lower noise frequencies, the LC filtering becomes unfeasible due to the size of the LC components that have to be used. The alternative solution is to use a low dropout regulator.

In most situations, a power isolation filter consisting of a ferrite bead and several capacitors is enough to attenuate the voltage noise on the oscillator power supply to levels that are no longer impacting the output jitter.

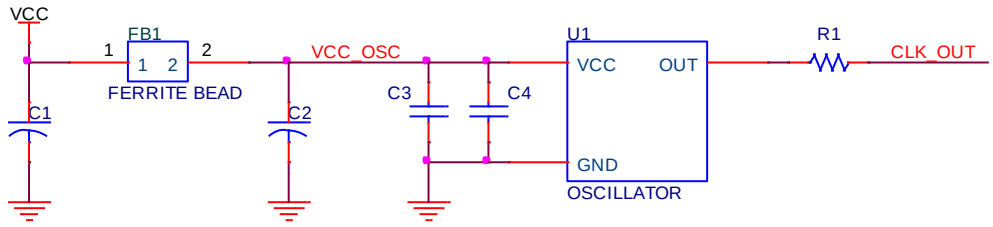

Figure 5 · Typical Power Supply Decoupling Circuit Recommended for Oscillators

C1, C2 are attenuating the low frequency noise on the VCC rail. Use a low ESR, 22-33uF, capacitor (usually tantalum /Polymer/Os_Con type) in a package that allows migration to larger values up to 100uF (for example 1206 package).

C3, C4 provide a low impedance path to GND for high frequency noise. Use 100nF and 10nF 0402, X7R or X5R, multilayer ceramic capacitors.

FB1 is used to increase the insertion loss of the filter. The ferrite bead should have saturation current double the maximum supply current of the oscillator and an impedance of several hundred ohm at 100MHz. It should have also a low DC resistance in order to prevent a large voltage drop over the ferrite bead. Some examples of ferrite beads which can be used for this purpose are: BLM18PG121, BLM18PG221 or BLM18PG471 from Murata.

In layout, place C3, C4 as close as possible to the oscillator VCC pin and minimize the mounted inductance introduced by the layout that is limiting the effectiveness of the capacitors (via close to pads, multiple via).

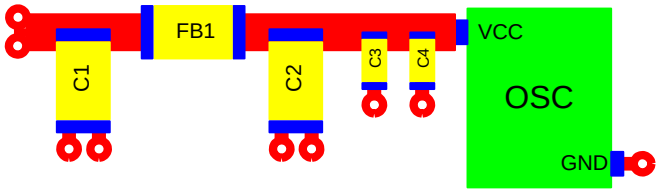

Figure 6 · Recommended Layout Placement of the Power Supply Decoupling Circuit

Local Oscillator Buffering

In order to reduce the cost, some designers are tempted to use a single local oscillator to feed several timing devices through a fan-out buffer. Microsemi does not recommend this approach; any buffer added on the local oscillator clock path will increase its jitter and will increase the jitter on the output of the timing circuit.

If a particular design can accommodate a higher output clock jitter, a buffer can be used. In this case it is important to select a clock fan-out buffer with very low additive jitter. The power supply of the buffer has to be properly filtered using a circuit similar with the one suggested for the oscillator. The clock tracks should be properly terminated and routed as short as possible to minimize noise coupling from other circuits.

Crystal

If a crystal recommended by Microsemi is not used, Application Note ZLAN-494 provides details how to select a crystal by identifying the relevant crystal parameters and their recommended range. The same application note provides also the methodology, formulas and an example of how to calculate the passive components associated with the crystal oscillator circuit based on the crystal's parameters.

When designing the PCB layout consider the following recommendations:

- Place the crystal as close as possible to the timing chip.
- Place the R and C components close to the crystal pins.
- Minimize the length of signal tracks.
- Place a GND ring around the crystal circuits.
- Have a GND plane on the internal layer underneath the crystal circuits.

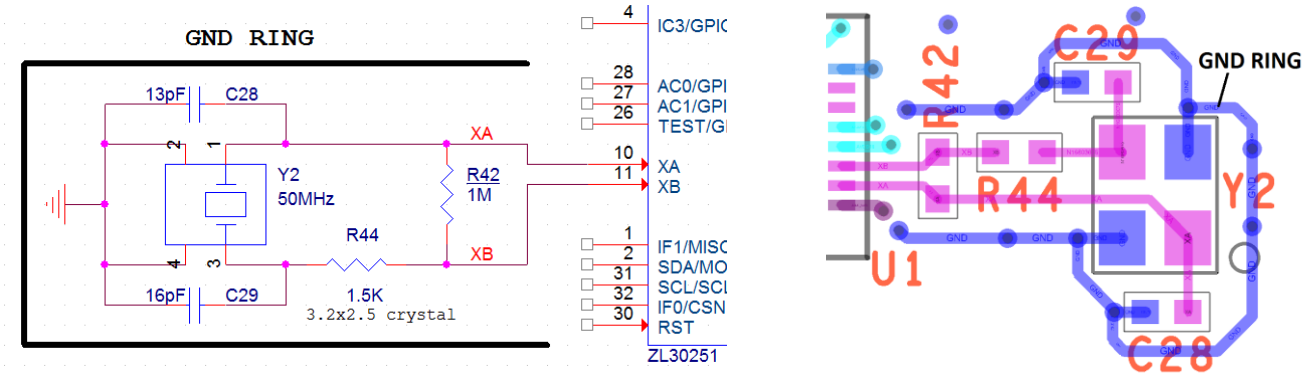

Figure 7 · Example of Crystal Circuit Implementation. Schematic and PCB View.

Output Clock Distribution.

In cases where a clock has to be provided to several circuits and there are not enough outputs available to achieve this, an external fan-out buffer can be used.

In order to minimize the jitter introduced by the fan-out buffer consider the following recommendations:

- Use Microsemi low jitter fan-out buffers such as a ZL40203; visit www.microsemi.com/timing-and-synchronization for clock buffer selection.
- Properly decouple the power supply of the fan-out buffer as recommended by Microsemi datasheet for that specific device.
- Properly terminate the inputs and the outputs as recommended by Microsemi datasheet for that specific device.
- Use differential paired clocks where possible, especially for longer route lengths transitioning "noisy" areas of the PCB.

Layout Recommendations.

One characteristic common to most of the modern electronic systems is the increase density of the circuits on the PCB's. The designer has to pack together in a limited space noisy circuits like switch mode power supplies and big digital IC's with noise sensitive clocking and analog circuits. While it is difficult to meet all the conflicting constraints generated by this situation, a bit of planning and following some simple rules can help to find an acceptable compromise solution. Here are some of the elements to consider at the layout design stage:

- Place the clocking circuits in "low noise" areas of the board away from switching mode power supplies, big/noisy digital circuits (FPGA/ASICs) and the high current path associated with them.
- Limit the length of the clock traces.
- Match the length of the p and n signals within a differential pair.
- Use controlled impedance routing and proper terminations for high speed signals/clocks as a way to preserve the signal integrity of the signal and reduce noise emission.
- Avoid routing the clock traces over discontinuities in the reference GND and power planes.
- Use extra clearance between clock tracks and adjacent signals (especially when they are high speed / fast slew rate signals) to reduce the crosstalk.
- In the case of differential pairs, keep a minimum clearance of at least 2S between pairs; where S is the spacing between P and N tracks of a differential pair.
- Minimize the use of via in the clock traces. Avoid unnecessary bends; when necessary use 45° or round bend.
- When power decoupling implementation involves local power islands, minimize the capacitive coupling between power islands and between the power islands and the main power planes (try to not overlap them when are in adjacent layers not separated by a GND plane layer). Avoid routing noisy digital signals in adjacent layers next to the power islands.
- Make the connection between power supply pins (VCC and GND) and power planes as short as possible using a dedicated via and tracks wider than for regular signals (minimize the impedance of this connection). No via sharing between power supply pins.
- Place the decoupling capacitors as close as possible to the power pins of the IC. Place break out via as close as possible to the capacitor pins and connect them with tracks wider than for regular signal. No via sharing between decoupling. When possible use multiple via breakout to reduce further the impedance of this connection.
- On power distribution path, minimize the number of layer changes. Use multiple via at each layer change to limit the voltage drop especially on high current paths.
- Stack-up selection. It is preferable to route the clock traces on the signal layers placed between GND layers or GND and Power layers. If there are two signal layers adjacent in the stack-up, keep a 90deg angle between the routing directions of the two layers in order to minimize the crosstalk. For example route the signals East/West on one layer and North/South on the other.

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