REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		8-28-03
B	Added Required External Pull-ups, nLDEV Clarification, New Logo		5-25-04
C	Clarified Crystal Circuit Requirements		7-15-04
D	Added MII MDIO Pull-up Resistor Information		4-20-05

Document Description

Schematic Checklist for the LAN91C111, 128-pin QFP Package

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SC471184	D

Schematic Checklist for LAN91C111

Information Particular for the 128-pin QFP Package

LAN91C111 QFP Phy Interface:

1. TPO+ (pin 16); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to +3.3V. This pin also connects to the transmit channel of the magnetics.

2. TPO- (pin 17); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to +3.3V. This pin also connects to the transmit channel of the magnetics.

3. TPI+ (pin 19); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 24.9Ω, 1.0% resistor in series with a 0.01 μF capacitor (C_{rxterm}) to +3.3V. This pin must also connect in series to another 24.9Ω, 1.0% resistor that provides the receive channel connection to the magnetics.

4. TPI- (pin 20); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 24.9Ω, 1.0% resistor in series with a 0.01 μF capacitor (C_{rxterm}) to +3.3V. This pin must also connect in series to another 24.9Ω, 1.0% resistor that provides the receive channel connection to the magnetics.

5. Only one 0.01 μF capacitor (C_{rxterm}) to +3.3V is required. It is shared by both pins 19 & 20.

LAN91C111 QFP Magnetics:

1. The center tap connection on the LAN91C111 side for the transmit channel must be connected to +3.3V directly.

2. The center tap connection on the LAN91C111 side for the receive channel must remain a no-connection.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TPO+ (pin 16) of the LAN91C111.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TPO- (pin 17) of the LAN91C111.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPI+ (pin 19) of the LAN91C111.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPI- (pin 20) of the LAN91C111.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Power Connections:

1. VCC pins on the LAN91C111 QFP are 3, 35, 46, 64, 79, 100, 112 & 122. They require connection to +3.3V.

2. Each power pin should have one .01 μF (or smaller) capacitor to decouple the LAN91C111. The capacitor size should be SMD_0603 or smaller.

3. AVDD pins on the LAN91C111 QFP are 13 & 18. They require connection to +3.3V.

4. Each AVDD pin should have one .01 μF (or smaller) capacitor to decouple the LAN91C111. The capacitor size should be SMD_0603 or smaller.

5. Unless there are some issues with EMI problems, we recommend tying the VCC & the AVDD pins together and connect them to a +3.3V power plane.

6. If EMI problems are encountered, ferrite beads may be placed in series with the voltage connections of the VCC pins or the AVDD pins or both. This may or may not pay dividends at EMI testing. If ferrite beads are used, be certain to place bulk capacitors on each side of the ferrite bead.

Ground Connections:

1. Digital Ground pins on the LAN91C111 QFP are 26, 41, 54, 59, 69, 74, 95, 105, 110 & 119. They need to be connected directly to a solid ground plane.

2. AVSS pins on the LAN91C111 are 15 & 21. They need to be connected directly to a solid ground plane.

3. We recommend that the Digital Ground pins and the AVSS pins be tied together to the same ground plane.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN91C111 QFP. For exact specifications and tolerances refer to the latest revision LAN91C111 data sheet.

2. XTAL1 (pin 1) on the LAN91C111 QFP is the clock circuit input. This pin requires a 10 – 30 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 2) on the LAN91C111 QFP is the clock circuit output. We recommend placing a 5 - 15Ω resistor in series with this pin to the crystal for EMI purposes. The other side of the resistor can then connect to a matching 10 – 30 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the value for the series resistor is system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

EEPROM Interface:

1. EECS (pin 12) on the LAN91C111 QFP connects to the external EEPROM's CS pin.

2. EESK (pin 11) on the LAN91C111 QFP connects to the external EEPROM's serial clock pin.

3. EEDO (pin 9) on the LAN91C111 QFP connects to the external EEPROM's Data In pin.

4. EEDI (pin 10) on the LAN91C111 QFP connects to the external EEPROM's Data Out pin.

5. Be sure to strap the external EEPROM for 64 x 16 operation.

6. In order to use the EEPROM interface, be sure ENEEP (pin 8) can be strapped high. ENEEP is an input signal with an internal pull-up. This signal must be grounded if no EEPROM is connected to the LAN91C111 QFP.

7. ISO0 (pin 5), ISO1 (pin 6) & ISO2 (pin 7) control what data is used from the EEPROM. Strap these pins to a known state. These input signals have internal pull-ups.

RBIAS resistor:

1. RBIAS (pin 14) on the LAN91C111 QFP should connect to ground through an 11.0K Ω, 1.0% resistor.

MII Interface:

1. When utilizing either an external MII Phy or an MII Connector, the following table indicates the proper connections for the 18 signals.

From:	Connects To:	
LAN91C111 QFP	**MII Physical Device**	**MII Connector**
RXD0 (pin 126)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 125)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 124)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 123)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 127)	RX_DV	RX_DV (contact 8)
RX_ER (pin 128)	RX_ER	RX_ER (contact 10)
RX25 (pin 120)	RX_CLK	RX_CLK (contact 9)
TXD0 (pin 118)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 117)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 116)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 115)	TXD<3>	TXD<3> (contact 17)
TXEN100 (pin 113)	TX_EN	TX_EN (contact 13)
TX25 (pin 111)	TX_CLK	TX_CLK (contact 12)
CRS100 (pin 121)	CRS	CRS (contact 19)
COL100 (pin 114)	COL	COL (contact 18)
MDI (pin 27)	MDIO	MDIO (contact 2)
MDO (pin 28)	MDIO	MDIO (contact 2)
MCLK (pin 29)	MDC	MDC (contact 3)

2. If the MII interface is not used by the system, do not terminate on the board level. These pins have the proper internal terminations and should be left as no-connects.

Required External Pull-ups:

1. ARDY (pin 40) is an open-drain output of the LAN91C111 QFP. An external pull-up resistor is required for this signal.

2. nLEDA (pin 24) is an open-drain output of the LAN91C111 QFP. An external pull-up resistor is required for this signal.

3. nLEDB (pin 25) is an open-drain output of the LAN91C111 QFP. An external pull-up resistor is required for this signal.

4. When using the MII interface of the LAN91C111 QFP with an external Physical device on board, a pull-up resistor on the signal MDIO must be incorporated. A pull-up resistor of 1.5KΩ to +5V is required for this application. If the LAN91C111 QFP is used with the industry standard MII connector, the 1.5KΩ is not required as this pull-up will be on the plug-in MII PCB.

CPU Interface:

1. A1 – A15 Address Bus: Please refer to the latest revision of the LAN91C111 Application Note for exact implementation of the CPU interface selected.

2. D0 – D31 Data Bus: Please refer to the latest revision of the LAN91C111 Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN91C111 Application Note for exact implementation of the CPU interface selected.

Miscellaneous:

1. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

2. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

3. nLDEV (pin 47) is a regular output buffer of the LAN91C111 QFP. Depending upon the application, an open-drain output buffer may be required to interface this signal to the system. In an ISA application, for instance, where there may be multiple devices connected to this signal (nIOCS16) in the system, the open-drain buffer is required. If the open-drain buffer is required, remember to provide a pull-up resistor somewhere in the system for the buffer.

LAN91C111 QFP QuickCheck Pinout Table:

Use the following table to check the LAN91C111 QFP shape in your schematic.

LAN91C111 QFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	XTAL1	39	nADS	65	D19	103	D5
2	XTAL2	40	ARDY	66	D18	104	D4
3	VDD	41	GND	67	D17	105	GND
4	nCSOUT	42	nVLBUS	68	D16	106	D3
5	IOS0	43	AEN	69	GND	107	D2
6	IOS1	44	LCLK	70	D15	108	D1
7	IOS2	45	nSRDY	71	D14	109	D0
8	ENEEP	46	VDD	72	D13	110	GND
9	EEDO	47	nLDEV	73	D12	111	TX25
10	EEDI	48	nRDYRTN	74	GND	112	VDD
11	EESK	49	X25OUT	75	D11	113	TXEN100
12	EECS	50	D31	76	D10	114	COL100
13	AVDD	51	D30	77	D9	115	TXD3
14	RBIAS	52	D29	78	D8	116	TXD2
15	AGND	53	D28	79	VDD	117	TXD1
16	TPO+	54	GND	80	A1	118	TXD0
17	TPO-	55	D27	81	A2	119	GND
18	AVDD	56	D26	82	A3	120	RX25
19	TPI+	57	D25	83	A4	121	CRS100
20	TPI-	58	D24	84	A5	122	VDD
21	AGND	59	GND	85	A6	123	RXD3
22	nLNK	60	D23	86	A7	124	RXD2
23	LBK	61	D22	87	A8	125	RXD1
24	nLEDA	62	D21	88	A9	126	RXD0
25	nLEDB	63	D20	89	A10	127	RX_DV
26	GND	64	VDD	90	A11	128	RX_ER
27	MDI			91	A12		
28	MDO			92	A13		
29	MCLK			93	A14		
30	nCNTRL			94	A15		
31	INTR0			95	GND		
32	RESET			96	nBE0		
33	nRD			97	nBE1		
34	nWR			98	nBE2		
35	VDD			99	nBE3		
36	nDATACS			100	VDD		
37	nCYCLE			101	D7		
38	W/nR			102	D6		

Reference Material:

1. SMSC LAN91C111 Data Sheet; check web site for latest revision.
2. SMSC LAN91C111 EVB Schematic, Assembly No. 6173; check web site for latest revision.
3. SMSC LAN91C111 EVB PCB, Assembly No. 6173; order PCB from web site.
4. SMSC LAN91C111 EVB PCB Bill of Materials, Assembly No. 6173; check web site for latest revision.
5. SMSC LAN91C111 Application Note 9-6; check web site for latest revision.
6. SMSC FAQ for LAN91C111 Application Note 9-0; check web site for latest revision.
7. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.