Atmel AVR178: Atmel AT90PWM81/161 Schematic Checklist

Features

- **Power supplies**
- **Reset circuit**
- **Clocks and crystal oscillators**
- **ISP/debugWIRE**

1 Introduction

A good hardware design comes from a proper schematic.

This application note describes a common checklist that should be used when starting and reviewing the schematics for an Atmel® AT90PWM81/161 design.

8-bit Atmel Microcontrollers

Application Note

Rev. 8396B-AVR-01/12

2 Power supplies

2.1 Power supply connections

Figure 2-1. Power supply schematic.

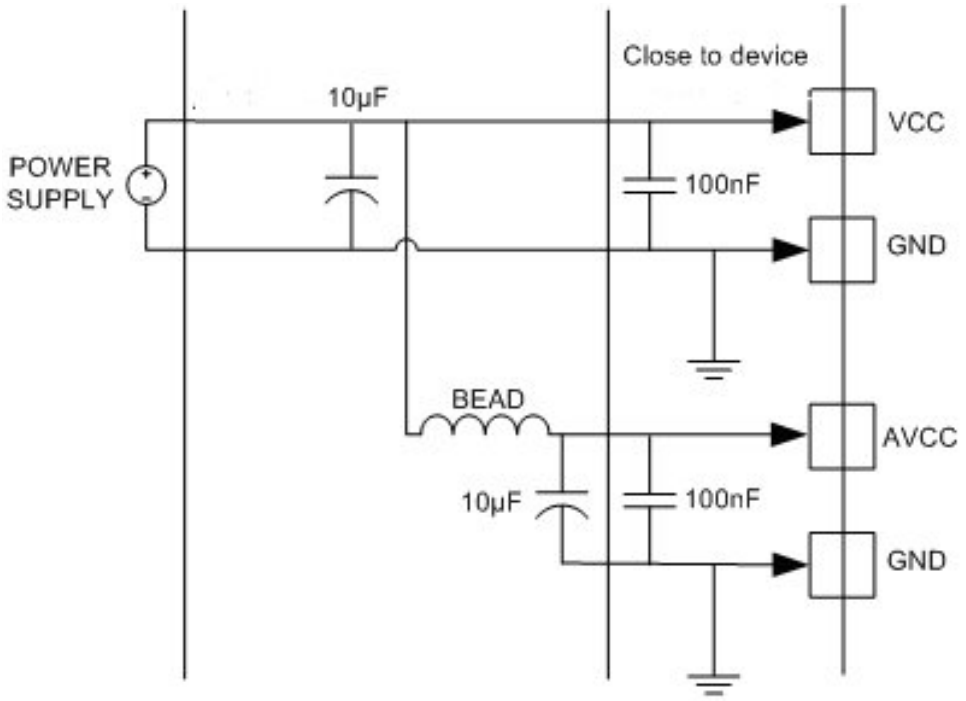

Table 2-1. Power supply connections.

Signal name	Recommended pin connection	Description
VCC	2.7V to 5.5V Decoupling/filtering capacitors 100nF (1)(2) and 10µF (1)	Digital supply voltage
AVCC	2.7V to 5.5V Decoupling/filtering capacitors 100nF (1)(2) and 10µF (1) Ferrite bead (3) prevents V_{CC} noise from interfering with AV_{CC}	Analog supply voltage
GND		Ground

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group. Low ESR capacitors should be used for better decoupling.
3. Ferrite bead has better filtering performance than the common inductor at high frequency. It can be added between V_{CC} and AV_{CC} to prevent digital noise from entering the analog power. The bead should provide enough impedance (for example, 50Ω at 20MHz and 220Ω at 100MHz) for separating the digital power from the analog power.

2.2 External analog reference connections

The following schematic checklist is necessary only if the design is using the external analog reference. If the internal reference is used, the circuit is not necessary.

Figure 2-2. External analog reference schematic.

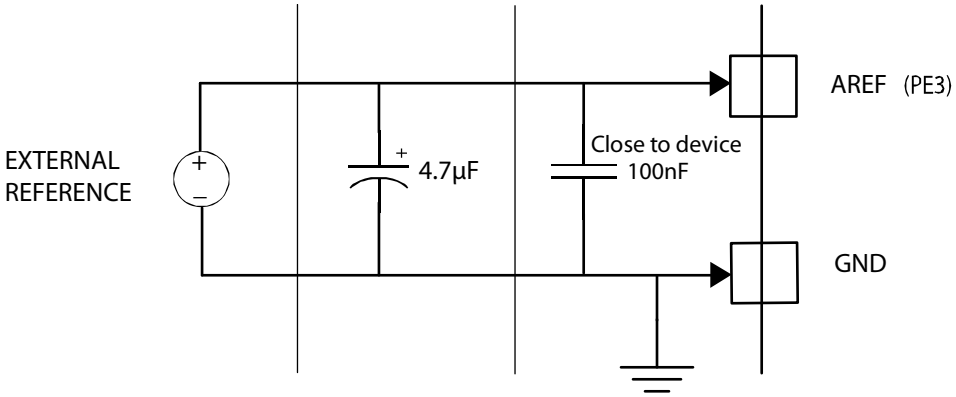

Table 2-2. External analog reference connections.

Signal name	Recommended pin connection	Description
AREF	2.56V to AV_{CC}-0.6V Decoupling/filtering capacitors 100nF (1)(2) and 4.7µF (1)	External references from AREF pin on PORT E3
GND		Ground

Notes: 1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device.

3 External reset circuit

The external reset circuit is connected to the reset pin when the external reset function is used. If internal reset is used, the circuit is not necessary. The reset switch also can be removed if manual reset is not necessary.

Figure 3-1. External reset circuit example schematic.

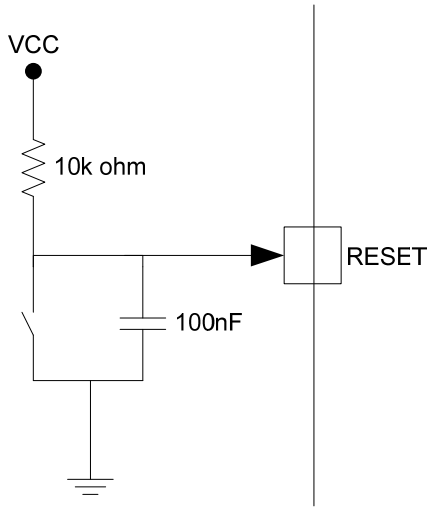

Table 3-1. Reset circuit connections.

Signal name	Recommended pin connection	Description
RESET	Reset low-level threshold voltage V_{CC} = 2.7 – 5.5V: below 0.2 × V_{CC}	reset pin

Note: This pull-up resistor makes sure that RESET does not go low unintentionally. When PDI programming and debugging are used, the reset line is used as the clock. In this case, the reset pull-up should be 10kΩ or greater or be removed altogether.

Any reset capacitors should be removed if PDI programming and debugging are used. Other external reset sources should be disconnected.

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source example schematic.

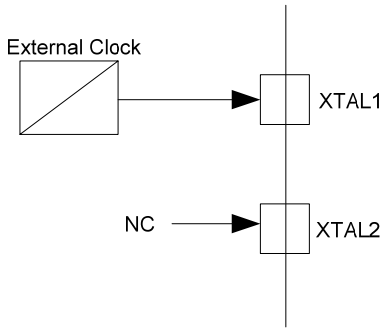

Table 4-1. External clock source connections.

Signal name	Recommended pin connection	Description
XTAL1	XTAL1 is used as input for an external clock signal	Input for inverting oscillator pin 1
XTAL2	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic.

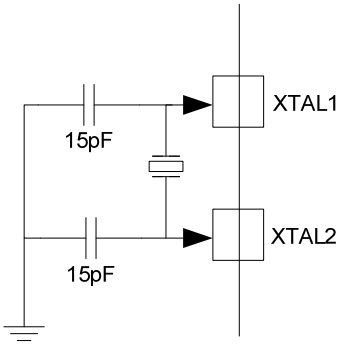

Table 4-2. Crystal oscillator checklist.

Signal name	Recommended pin connection	Description
XTAL1	Biasing capacitor 15pF (1)(2)	External crystal between 0.9MHz and 16MHz
XTAL2	Biasing capacitor 15pF (1)(2)	

Notes:
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used, or refer to the application note, “AVR042: AVR Hardware Design Considerations.”
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

5 ISP port

5.1 ISP/debugWIRE

Figure 5-1. ISP/DW port interface example schematic.

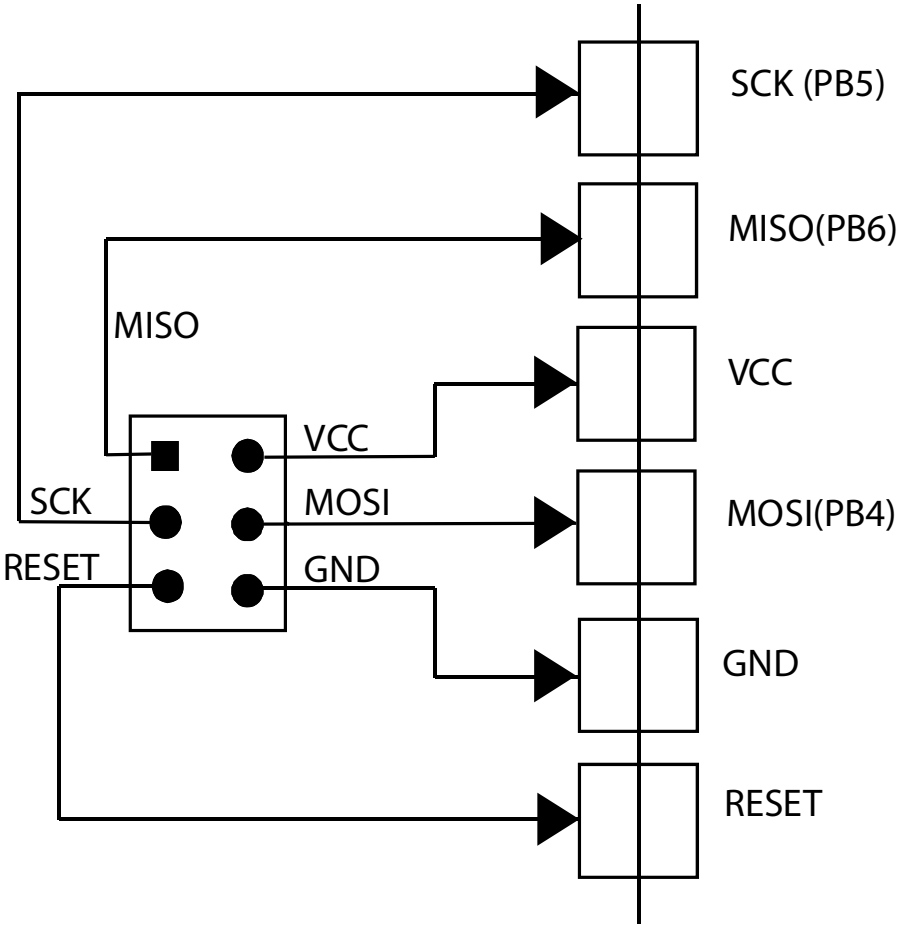

Table 5-1. ISP/DW port interface checklist.

Signal name	Description
MISO	SPI communication
SCK	SPI clock
MOSI	SPI communication
RESET	Device external reset line and used in debugWIRE
VCC	Digital supply voltage
GND	Ground

NOTE

Some precautions regarding the reset line should be taken to ensure proper communication via the debugWIRE interface. Pull-up resistors on the reset line must not be smaller than 10kΩ (the pull-up resistor is not required for debugWIRE functionality), and there should be no capacitive load. Other logic connected to the reset line should be removed during debugging.

6 Suggested reading

6.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available at: http://www.atmel.com/dyn/resources/prod_documents/doc77340.pdf.

6.2 Evaluation kit schematic

The Atmel AVR® STK®521 evaluation kit contains the full schematic for the board; it can be used as a reference design. The schematic is available in User Guide: http://www.atmel.com/dyn/resources/prod_documents/doc8194.pdf.

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