

Hardware Limit Timer on PIC® Microcontrollers

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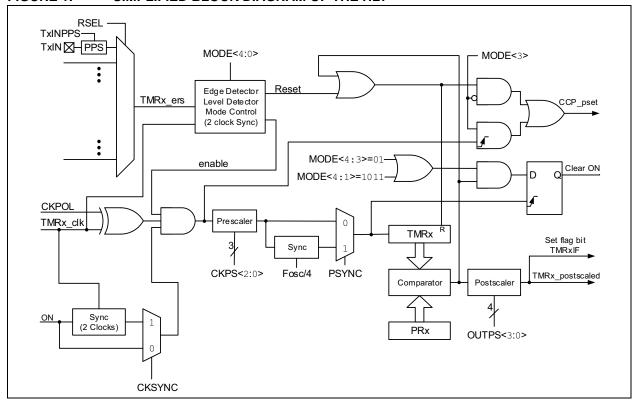
INTRODUCTION

PIC[®] microcontrollers are equipped with hardware features that are useful for implementing Fault detection in safety critical applications. The Hardware Limit Timer (HLT), which has hardware monitoring capabilities for missed periodic events, is one such feature. This on-chip peripheral helps in detecting external hardware Fault conditions like Stall and Stop conditions in a motor control application. It can also be used for any precise timing application that has a dependency on an external signal. This document aims at familiarizing the reader with the functionality of the HLT and its different modes of operation.

THE HARDWARE LIMIT TIMER

The Hardware Limit Timer is an enhanced version of Microchip's PIC microcontroller Timer2 module with the addition of an asynchronous external Reset capability and one-shot functionality. The timer can be started, stopped and reset based on an external event. This external signal can be from an external input pin or can be derived from on-chip core independent peripherals such as a comparator or the Zero-Cross Detect (ZCD). The timer can produce an interrupt signal when an expected event is missed. Using the HLT feature minimizes the CPU overhead, thereby freeing the CPU for other time-critical applications. The HLT also eliminates the need of any external components for fault handling. It has multiple modes of operation and selectable clock sources, which makes the design flexible. The simplified block diagram of Timer2 with the hardware limit feature is shown in Figure 1. The HLT is started by setting the ON bit of the TxCON register. The mode of operation is controlled by the MODE bits of the TxHLT register.

FIGURE 1: SIMPLIFIED BLOCK DIAGRAM OF THE HLT



The Hardware Limit Timer can be clocked using one of the following clock sources:

- FOSC (System Clock)
- FOSC/4 (Instruction Clock)
- LFINTOSC (Low-Frequency Internal Oscillator)
- MFINTOSC (Medium-Frequency Internal Oscillator)
- HFINTOSC (High-Frequency Internal Oscillator)
- Timer0 or Timer1 Output Pin
- Timer Input Pin

For the external source to the HLT, the following external trigger sources can be chosen:

- Complementary Waveform Generator (CWG)
- Zero-Cross Detect (ZCD)
- Capture/Compare/PWM (CCP)
- Timer4
- Timer6
- Comparator

Note: Some of these features might vary depending on the family of products. Refer to the product specific data sheet for

further details.

MODES OF OPERATION

The modes in the HLT can be broadly classified into Rollover Pulse mode, One-Shot mode and Monostable mode. The Hardware Limit Timer feature for these modes allows the selected input to clear the TMRx register and restart the timing sequence. There are both edge-sensitive and level-sensitive options defined. Table 1 summarizes all the modes of the timer and the working of each mode.

TABLE 1: MODES OF OPERATION OF HLT WITH START, STOP AND RESET CONDITIONS

Mode		Operation	Start	Reset	Stop	
Rollover Pulse	Software Gate	Software-controlled ON bit, legacy Timer2 operation	ON = 1	Period match event	ON = 0	
	Hardware Gate, Active-High	Hardware gate, active-high	Input signal = 1 and ON = 1 Period match even		Input signal = 0 or ON = 0	
	Hardware Gate, Active-Low	Hardware gate, active-low	Input signal = 0 and ON = 1	Period match event	Input signal = 1 or ON = 0	
	Rollover Pulse with HLT action (Edge-Triggered Hardware Limit mode and Level-Triggered Hardware Limit mode) ⁽¹⁾	Input either edge Reset		Input edge	ON = 0	
		Input rising edge Reset		Input rising edge		
		Input falling edge Reset	ON = 1	Input falling edge		
		Input active-low Reset		Input signal = 0	ON = 0 or held in Reset by	
		Input active-high Reset		Input signal = 1	input signal	

Note 1: The modes that are highlighted in the table are the HLT modes.

TABLE 1: MODES OF OPERATION OF HLT WITH START, STOP AND RESET CONDITIONS

Mode		Operation	Start	Reset	Stop	
One-Shot mode	One-Shot SW Start	Software-controlled ON bit	ON = 1	Period match event		
	One-Shot Edge-Triggered Start	Input rising edge start	Input signal rising edge and ON = 1			
		Input falling edge start	Input signal falling edge and ON = 1	Period match event	ON = 0 or next clock after	
		Input either edge start	Input signal either edge and ON = 1			
	One-Shot Edge-Triggered Start with HLT Action (Edge-Triggered Hardware Limit One-Shot mode) ⁽¹⁾	Input rising edge start and Reset	Input signal rising edge and ON = 1	Input signal rising edge	period match until ON bit is set by software	
		Input falling edge start and Reset	Input signal falling edge and ON = 1	Input signal falling edge		
		Input rising edge start and active-low Reset	Input signal rising edge and ON = 1	Input signal = 0		
		Input falling edge start and active-high Reset	Input signal falling edge and ON = 1	Input signal = 1		
	One-Shot Level-Triggered Start with HLT Action (Level Triggered Hardware Limit One-Shot Mode)*	Input high start and active-low Reset	Input signal = 1 and ON = 1	Input signal = 0		
		Input low start and active-high Reset	Input signal = 0 and ON = 1	Input signal = 1	ON = 0 or held in Reset	
Monostable	Edge-Triggered Start	Input either edge Reset	Input signal rising edge and ON = 1		ON = 0 or next clock after period match until next input edge	
		Input rising edge Reset	Input signal rising edge and ON = 1	Period match event		
		Input falling edge Reset	Input signal rising edge and ON = 1		mpat ougo	

Note 1: The modes that are highlighted in the table are the HLT modes.

The following sections will provide more details about the HLT modes of the Rollover Pulse mode and the One-Shot modes.

Rollover Pulse Mode with Hardware Limit Timer

In the Rollover Pulse mode, the ON bit allows the user to start and stop the timer. The timer increments with each clock input with the ON bit set and stops incrementing when the ON bit is cleared. If the ON bit is set again, then the timer continues to increment from where it stopped. On a period match, the timer resets on the next clock and continues counting from '0'. The Rollover Pulse modes with the hardware limit feature are:

- Edge-Triggered Hardware Limit mode
- · Level-Triggered Hardware Limit mode

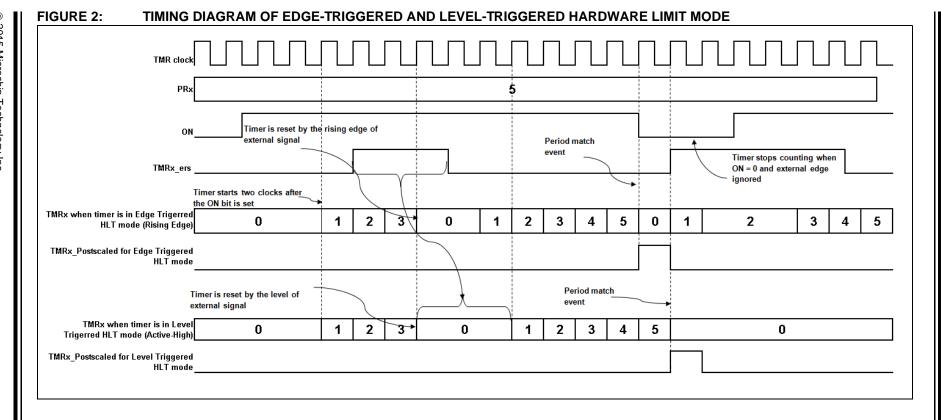
In Edge-Triggered Hardware Limit mode, setting the ON bit starts the timer. The external signal can reset the timer before the period match occurs.

The external edges for Reset can be:

- Reset on rising edge (MODE<4:0> = 00101)
- Reset on falling edge (MODE<4:0>= 00100)
- Rising or falling either edge can reset the counter (MODE<4:0> = 00011)

The external signal level can also be used to reset the timer. This level can be a high state or a low state (MODE<4:0> = 00010 or MODE<4:0> = 00001). The operation of the Edge-Triggered Hardware Limit mode and Level-Triggered Hardware Limit mode is illustrated in Figure 2.

- **Note 1:** The setting and clearing of the ON bit is executed by the CPU. CPU execution is asynchronous to the timer clock input.
 - **2:** The timer events consume up to two clock cycles for starting and stopping.



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One-Shot Mode

Unlike in the Rollover Pulse mode, in One-Shot mode, the ON bit is cleared in hardware when the timer rolls over. Only one timer interrupt is generated and the timer stops counting. The ON bit must be set by software to start another timer cycle. This mode is useful when the user desires to time a single event rather than a periodic event. The One-Shot modes with the hardware limit feature are:

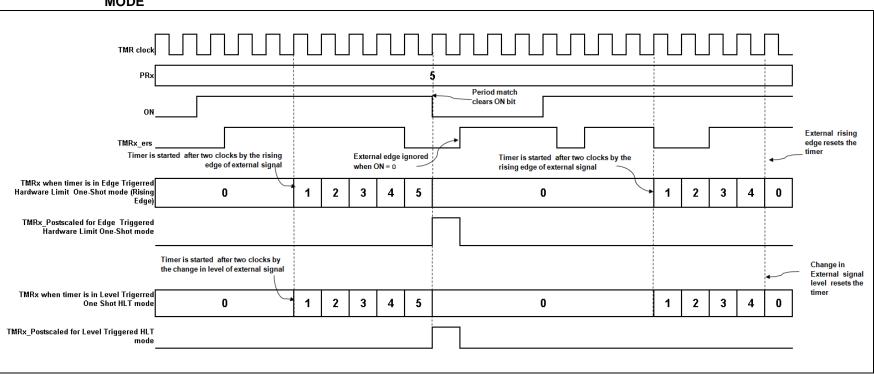
- Edge-Triggered Hardware Limit One-Shot mode
- · Level-Triggered Hardware Limit One-Shot mode

Edge-Triggered Hardware Limit One-Shot mode features not only an edge-triggered start but it also resets the timer on subsequent edges of the external signal (i.e., once the ON bit is set, the occurrence of the first edge of the external signal will start the timer). The timer runs until another edge of the external signal or until a period match occurs. The timer will automatically resume counting after the subsequent Reset edge and it will run until the period match occurs. There are two ways that this mode can be achieved:

- Rising Edge Start and Reset (MODE<4:0> = 01100)
- Falling Edge Start and Reset (MODE<4:0> = 01101)

In Level-Triggered Hardware Limit One-Shot mode, the level of the external signal starts and resets the timer. This level can be configured to either a high state or a low state (MODE<4:0> = 011110 or MODE<4:0> = 01111). The timer does not start until the ON bit is set and the external signal occurs. The timer keeps running until the external signal is at the same level. Once the level of the external signal changes its state, the timer is reset. Reset levels can either be high or low. The operation of the Edge-Triggered One-Shot Hardware Limit mode and Level-Triggered One-Shot Hardware Limit mode are illustrated in Figure 3.

FIGURE 3: TIMING DIAGRAM OF EDGE-TRIGGERED HARDWARE LIMIT AND LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE



Monostable Mode

In this mode, the timer stops after a rollover but it does not clear the ON bit. An external signal edge is again required to start the timer. The timer stops either on clearing the ON bit or on the period match event. The following edges will start the timer:

- Rising Edge (MODE<4:0> = 10001)
- Falling Edge (MODE<4:0> = 10010)
- Rising or Falling Edge (MODE<4:0> = 10011)

CONFIGURATION OF TIMER2 WITH THE HARDWARE LIMIT FEATURE

Table 2 contains the summary of registers associated with the Hardware Limit Timer.

TABLE 2: REGISTERS ASSOCIATED WITH TIMER2 WITH THE HARDWARE LIMIT FEATURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxCLKCON	_	_	_	_	_	TxCS<2:0>		
TxCON	ON	CKPS<2:0>			OUTPS<3:0>			
TxRST	_	_	_	_	RSEL<3:0>			
TxHLT	PSYNC	CKPOL	CKSYNC	_	MODE<3:0>			

The TxCS bits of the TxCLKCON register are used for the clock selection. The external signal source selection is done in the TxRST register. Prescaler and postscaler settings are done in the TxCON register. Example 1 shows the code snippet used to configure Timer2 registers to operate in Edge-Triggered Rollover Pulse Hardware Limit mode.

EXAMPLE 1: CODE SNIPPET FOR CONFIGURATION OF TIMER2 IN EDGE-TRIGGERED HARDWARE LIMIT MODE

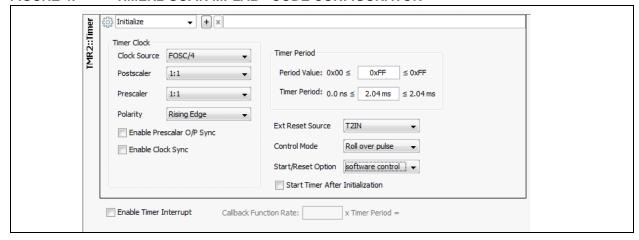
```
T2CLKCONbits.T2CS = 0b0000; //Clock input is Fosc/4
T2CONbits.CKPS = 0b111; //Prescaler setting 1:128
T2CONbits.OUTPS = 0b1111; //Postscaler setting 1:16
T2RSTbits.RSEL = 0b0000; //Selecting Timer2 input as external source
T2HLTbits.PSYNC = 1; //Prescaler synchronization bit
T2HLTbits.CKPOL = 0; //Rising edge of input clock clocks timer
T2HLTbits.CKSYNC = 1; //ON bit synchronized to input clock
T2HLTbits.MODE = 0b01100; //Edge triggered hardware limit mode -rising edge
T2CONbits.ON = 1; //Timer is switched on
```

USING THE MPLAB® CODE CONFIGURATOR FOR CODE GENERATION OF THE HLT

The MPLAB[®] Code Configurator, which is a plug-in tool for MPLAB[®] X IDE, generates the drivers for controlling and driving the HLT based on the settings and selections made in the GUI.

The clock source selection, prescaler and postscaler settings can be done to meet the time period requirements desired by the user. External source selection and mode of operation can be picked from the drop-down selection provided by the GUI (see Figure 4). For further details refer to the "MPLAB® Code Configurator User's Guide" (DS40001725).

FIGURE 4: TIMER2 GUI IN MPLAB® CODE CONFIGURATOR



API List for the HLT

The following API is generated by MCC for the HLT module:

- void TMR2_Initialize(void): This API initializes the TxCON, TxCLKCON, TxHLT, TxRST, TxPR, TxTMR and interrupt flags, and it starts the timer.
- void TMR2_ModeSet(TMR2_HLT_MODE mode):
 This API configures different types of HLT modes.
- void TMR2_ExtResetSourceSet (TMR2_HLT_EXT_RESET_SOURCE reset): This API configures different types of HLT external Reset source.
- void TMR2_Start(void): This API starts the timer by writing to the TMRxON bit.
- void TMR2_Stop(void): This API stops the timer by clearing the TMRxON bit.
- uint8_t TMR2_Counter8BitGet(void): This API is used to get the TxTMR register value.
- void TMR2_Counter8BitSet(uint8_t timerVal): This API writes to the Timer register.
- void TMR2_Period8BitSet(uint8_t periodVal): This API is used to set the Period register to a particular value.
- void TMR2_Period8BitSet(uint8_t periodVal): This API is used to check if overflow has occurred, which is done by checking the TMRIF bit.

CONCLUSION

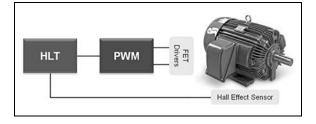
This technical brief describes how the Hardware Limit Timer module works on PIC microcontrollers. It familiarizes the reader with the hardware limit features of the Rollover Pulse modes and One-Shot modes. As explained in this technical brief, the timer in its suitable mode can be used for Fault detection in motors and in variable frequency PWM for power supply. More details can be found in each product specific data sheet.

APPENDIX A: APPLICATIONS OF THE HARDWARE LIMIT TIMER

A.1 Fault Detection in a Motor Using the HLT

The HLT in Edge-Triggered Hardware Limit Timer mode can be used in Fault detection of a cooling fan motor (Figure A-1). The RPM sensor or tachometer output of the fan is used as an external signal to the HLT. The Period register of the timer is set to a value that is sufficiently larger than the RPM count of the fan or more than the frequency of the fan tachometer output. Under normal conditions, when the fan is spinning, it gives periodic tachometer pulses. These pulses reset the timer before the period match occurs and the timer starts counting again. In the case of a Fault condition in the fan (i.e., the fan has stalled), it stops giving tachometer pulses. In this scenario, the timer continues to increment until the period match occurs. This event generates an interrupt and this interrupt can be registered to indicate that the fan is not spinning and that there is a Fault.

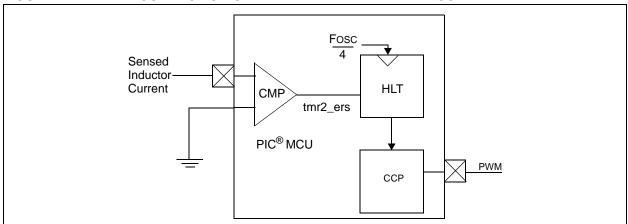
FIGURE A-1: FAULT DETECTION IN A MOTOR



A.2 Fixed ON Time Variable Frequency PWM Generation Using the HLT

Monostable Edge-Triggered Start mode can be used in a DC-DC converter application that is operating in Critical Conduction mode, with soft switching. By detecting the zero inductor current (used as external signal to the timer), HLT can be started for a fixed ON time. The Period register can be set to a value that is sufficiently large value, more than the maximum ON time. When HLT is used along with CCP for PWM generation, the output pulse remains active until a match of the CCP Duty register with the Timer register occurs (Figure A-2). The next pulse begins only at the next external edge, which is the ZCD event of the inductor current. This is an example of a fixed ON time variable frequency PWM generation (Figure A-3).

FIGURE A-2: INTERCONNECTION OF THE TIMER2 WITH HLT AND CCP



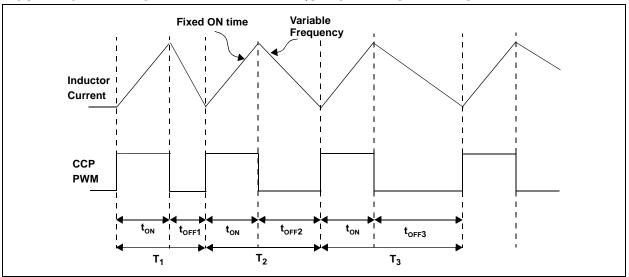


FIGURE A-3: FIXED ON TIME VARIABLE FREQUENCY PWM GENERATION

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