AN 26.20

SMBus Slave Interface for the USB553XB

1 SMBus Slave Interface

The SMBus slave interface can be used to customize the functionality of the USB553XB hub. Through this interface the SOC is able to control the digital and USB lines for internal testing, configure the hub to function with the desired options when enumerating, and load custom firmware to fully unlock the features of the embedded processor.

1.1 References

- USB5532 Datasheet
- USB5533 Datasheet
- USB5534 Datasheet
- USB5537 Datasheet

System Management Bus Specification, Version 1.0, http://smbus.org/specs

1.2 SMBus Protocol

The SMBus protocol is a flexible 2-pin serial protocol used for low speed communication between integrated circuits. The protocol consists of a SMBCLK pin generated by the SMBus Master and a bi-directional SMBDATA pin that can be driven by a Master or a Slave. The bus requires a pull up resistor on both SMBCLK and SMBDATA to function. The hub configure the pins as Open/Drain buffers where the driver will either tristate the pin or drive the pin to GND. The input threshold for the high level ranges from 1.2V to 3.3V, allowing the hub to communicate with a large sample of SOCs on the market. Refer to the System Management Bus Specification for more details on the timing specifications of the bus.

2 SMBus Access

When the SMBus pins are pulled up during POR, the hub will enter SMBus Slave mode. In this mode the SOC may modify any of the configuration settings to customize the hub to their purposes. The SOC can configure the hub as USB Full Speed only, or have the hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. The hub can be addressed at the address 2Dh and interprets the data bytes as follows:

2.1 SMBus Block Write

The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands as well as a pointer to the hubs internal memory. After the address, the next byte of data is the count of data bytes that will

follow, up to 128 bytes in a block. Finally a write of 00h is used to terminate the write operation followed by the SMBus stop signal.

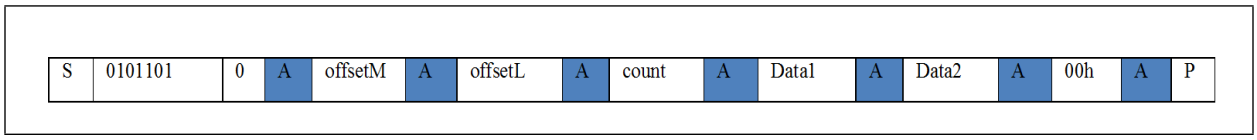

Figure 2.1 SMBus Block Write

2.2 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address followed by a repeat Start signal and an Address+Direction(1) byte. The hub will then start to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified.

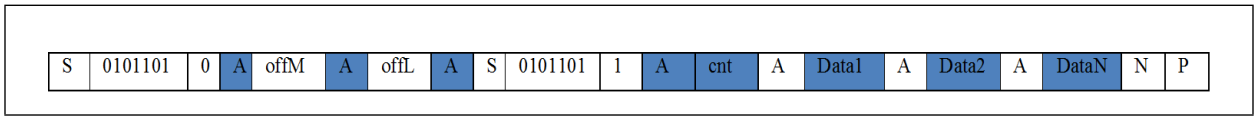

Figure 2.2 SMBus Block Read

2.3 Special Commands

There are special commands that can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or simply reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command.

Table 2.1 Special SMBus Commands

OPERATION	OPCODE	DESCRIPTION
Program OTP	9933h	Permanently program the configuration blocks to the part.
Read OTP	9934h	Place the contents of the OTP configuration blocks into the RAM at location 0x001E
SPI Device Access	9935h	Execute the SPI command to the attached SPI device.
Reboot	9936h	Restart the Hub state machine.
Configuration Register Access	9937h	Read and Write Configuration Registers
Extended Command	993Eh	Execute Extended Status Commands
USB Attach	AA55h	Enter Configuration Stage
USB Attach with SMBus Access	AA56h	Enter Configuration Stage with SMBus Access Enabled

3 Accessing Configuration Registers

The Configuration Register Access operation allows the SMBus Master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent the hub will interpret the memory starting at offset 00h as follows:

Table 3.1 Memory Format for Configuration Register Access

RAM ADDRESS	DESCRIPTION	NOTES
0000h	Direction	0 = Register Write, 1 = Register Read.
0001h	Data Length	Number of bytes to Read/Write when executing the command.
0002h	Configuration Address MSB	The upper byte of the 16-bit configuration register address.
0003h	Configuration Address LSB	The lower byte of the 16-bit configuration register address.
0004h	Data1	The first byte of data to write to or read from the Configuration Address.
...	...	...
0004h+N	DataN	The Nth byte of data to write to or read from the Configuration Address, N is equal to the Data Length.

3.1 Configuration Register Write Example

The following example shows how the SMBus messages will be formatted to set the VID of the hub to a custom value, AA55h.

1. Write data to the memory of the hub:

Table 3.2 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	06h	Number of bytes to write to memory.
4	00h	Write Configuration Register.
5	02h	Writing two data bytes.
6	30h	VID is in register **30**00h.
7	00h	VID is in register 30**00**h.
8	55h	LSB of Vendor ID AA**55**h.
9	AAh	MSB of Vendor ID **AA**55h.

2. Execute the Configuration Register Access command:

Table 3.3 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

3.2 Configuration Register Read Example

The following example shows how to read the Charger Detection register to find out what type of charger the hub has connected to:

1. Write data to the memory of the hub.

Table 3.4 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	04h	Number of bytes to write to memory.
4	01h	Read Configuration Register.
5	01h	Reading one data bytes.
6	30h	BC Detect is in register **30**E2h.
7	E2h	BC Detect is in register 30**E2**h.

2. Execute the Configuration Register Access command.

Table 3.5 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

3. Read back data starting at memory offset 04h, which is where the Data byte starts.

Table 3.6 Example SMBus Read Command

BYTE	VALUE	COMMENTS
0	5Ah	Address plus Write bit.
1	00h	Memory Address **00**04h.
2	04h	Memory Address 00**04**h.
3	59h	Address plus Read bit.
4	80h	Device sends 128 bytes of data.
5	56h	Charging Downstream Port Detected.

Note: Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set, the SMBus Master can send a stop at any time.

3.3 Configuration Registers

Below is the list of configuration registers and their address. The INIT column is the values that will be loaded when the USB Attach commands are sent.

Table 3.7 Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
30FFh	R/W	STCD	Hub Status/Command Register	05h
3C00h	R/W	PRT_PWR_SEL1	Port 1 Power Select	03h
3C04h	R/W	PRT_PWR_SEL2	Port 2 Power Select	03h
3C08h	R/W	PRT_PWR_SEL3	Port 3 Power Select	03h
3C0Ch	R/W	PRT_PWR_SEL4	Port 4 Power Select	03h
3C10h	R/W	PRT_PWR_SEL5	Port 5 Power Select	24h
3C14h	R/W	PRT_PWR_SEL6	Port 6 Power Select	23h
3C18h	R/W	PRT_PWR_SEL7	Port 7 Power Select	23h
3C20h	R/W	OCS_CFG_SEL1	Port 1 OCS Select	01h
3C24h	R/W	OCS_CFG_SEL2	Port 2 OCS Select	01h
3C28h	R/W	OCS_CFG_SEL3	Port 3 OCS Select	01h
3C2Ch	R/W	OCS_CFG_SEL4	Port 4 OCS Select	01h
3C30h	R/W	OCS_CFG_SEL5	Port 5 OCS Select	01h
3C34h	R/W	OCS_CFG_SEL6	Port 6 OCS Select	01h
3C38h	R/W	OCS_CFG_SEL7	Port 7 OCS Select	01h
5246h	R/W	CDP_DETECT	Charging Downstream Detected	Note 3.1

Table 3.7 Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
525Bh	R/W	OSC_GANG_SRC	OCS Pin Select	00h
60CAh	R/W	HS_UP_BOOST	USB Upstream Boost Register	00h
60CCh	R/W	HS_UP_SENSE	USB Upstream VariSense Register	00h
61C0h	R/W	SS_UP_STATE	USB3 Upstream Link State	Note 3.1
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register	00h
64CCh	R/W	HS_P1_SENSE	USB Port 1 VariSense Register	00h
65C0h	R/W	SS_P1_STATE	USB3 Port 1 Link State	Note 3.1
68CAh	R/W	HS_P2_BOOST	USB Port 2 Boost Register	00h
68CCh	R/W	HS_P2_SENSE	USB Port 2 VariSense Register	00h
69C0h	R/W	SS_P2_STATE	USB3 Port 2 Link State	Note 3.1
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register	00h
6CCCh	R/W	HS_P3_SENSE	USB Port 3 Varisense Register	00h
6DC0h	R/W	SS_P3_STATE	USB3 Port 3 Link State	Note 3.1
70CAh	R/W	HS_P4_BOOST	USB Port 4 Boost Register	00h
70CCh	R/W	HS_P4_SENSE	USB Port 4 Varisense Register	00h
71C0h	R/W	SS_P4_STATE	USB3 Port 4 Link State	Note 3.1
74CAh	R/W	HS_P5_BOOST	USB Port 5 Boost Register	00h
74CCh	R/W	HS_P5_SENSE	USB Port 5 Varisense Register	00h
78CAh	R/W	HS_P6_BOOST	USB Port 6 Boost Register	00h
78CCh	R/W	HS_P6_SENSE	USB Port 6 Varisense Register	00h
7CCAh	R/W	HS_P7_BOOST	USB Port 7 Boost Register	00h
7CCCh	R/W	HS_P7_SENSE	USB Port 7 Varisense Register	00h

Note 3.1 Status registers do not have a default value because the status can change depending on system conditions.

3.3.1 Register Definitions

Table 3.8 Hub Status/Command Register

STCD (0x30FF)			HUB COMMAND AND STATUS REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved. Software must never write a ‘1’ to these bits.
2	INTFW_PW_DN	R/W	Disable the hub configuration register access by disabling the clock running its configuration space. 0 = Hub configuration register access is enabled and hub configuration clock is running. 1 = Hub configuration register access is disabled and hub configuration clock is stopped. **Note:** This bit is write once and is only cleared by assertion of the external RESET_N pin
1	RESET	R/W	Reset the internal memory back to nRESET assertion default settings. **Note:** During this reset, this bit is automatically cleared to its default value of 0. 0 = Normal Run/Idle State. 1 = Force a reset of the registers to their default state.
0	Reserved	R/W	Reserved

3.3.1.1 USB3 Port Power and OCS Controllers

Table 3.9 Port 1 Power Select

PRT_PWR_SEL1 (0x3C00)			PORT 1 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.

Table 3.9 Port 1 Power Select

PRT_PWR_SEL1 (0x3C00)			PORT 1 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.10 Port 2 Power Select

PRT_PWR_SEL2 (0x3C04)			PORT 2 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.11 Port 3 Power Select

PRT_PWR_SEL3 (0x3C08)			PORT 3 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.

Table 3.11 Port 3 Power Select

PRT_PWR_SEL3 (0x3C08)			PORT 3 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.12 Port 4 Power Select

PRT_PWR_SEL4 (0x3C0C)			PORT 4 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.13 Port 5 Power Select

PRT_PWR_SEL5 (0x3C10)			PORT 5 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.14 Port 6 Power Select

PRT_PWR_SEL6 (0x3C14)			PORT 6 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.15 Port 7 Power Select

PRT_PWR_SEL7 (0x3C18)			PORT 7 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

Table 3.16 Port 1 OCS Select

OCS_CFG_SEL1 (0x3C20)			PORT 1 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.17 Port 2 OCS Select

OCS_CFG_SEL2 (0x3C24)			PORT 2 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.

Table 3.17 Port 2 OCS Select

OCS_CFG_SEL2 (0x3C24)			PORT 2 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.18 Port 3 OCS Select

OCS_CFG_SEL3 (0x3C28)			PORT 3 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.19 Port 4 OCS Select

OCS_CFG_SEL4 (0x3C2C)			PORT 4 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.20 Port 5 OCS Select

OCS_CFG_SEL5 (0x3C30)			PORT 5 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.21 Port 6 OCS Select

OCS_CFG_SEL6 (0x3C34)			PORT 6 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

Table 3.22 Port 7 OCS Select

OCS_CFG_SEL7 (0x3C38)			PORT 7 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

3.3.1.2 General Hub Status Registers

Table 3.23 Charging Downstream Detected

CDP_DETECT (0x5246)			CHARGING DOWNSTREAM DETECTED
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	Reserved	R/W	Reserved
6	P7_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
5	P6_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
4	P5_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
3	P4_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
2	P3_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
1	P2_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
0	P1_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.

Table 3.24 OCS Gang Control

OCS_GANG (0x525A)			OCS GANG CONTROL
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	P7_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
6	P6_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
5	P5_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
4	P4_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.

Table 3.24 OCS Gang Control

OCS_GANG (0x525A)			OCS GANG CONTROL
BIT	**NAME**	**R/W**	**DESCRIPTION**
3	P3_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
2	P2_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
1	P1_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the pin selected in OCS Pin Select.
0	Reserved	R/W	Reserved

3.3.1.3 Individual Port Analog Registers

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Table 3.25 USB Upstream Boost Register

HS_UP_BOOST (0x60CA)			USB UPSTREAM BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

Table 3.26 USB Upstream VariSense Register

PHY_UP_SENSE (0x60CC)			USB UPSTREAM VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved

Table 3.26 USB Upstream VariSense Register

PHY_UP_SENSE (0x60CC)			USB UPSTREAM VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.27 USB3 Upstream Link State

SS_UP_STATE (0x61C0)			USB3 UPSTREAM LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to USB3 Link States for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to USB3 Link States for more details.

Table 3.28 USB Port 1 Boost Register

HS_P1_BOOST (0x64CA)			USB PORT 1 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.29 USB Port 1 VariSense Register

PHY_P1_SENSE (0x64CC)			USB PORT 1 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.30 USB3 Port 1 Link State

SS_P1_STATE (0x65C0)			USB3 PORT1 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to USB3 Link States for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to USB3 Link States for more details.

Table 3.31 USB Port 2 Boost Register

HS_P2_BOOST (0x68CA)			USB PORT 2 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.32 USB Port 2 VariSense Register

PHY_P2_SENSE (0x68CC)			USB PORT 2 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.33 USB3 Port 2 Link State

SS_P2_STATE (0x69C0)			USB3 PORT 2 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to USB3 Link States for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to USB3 Link States for more details.

Table 3.34 USB Port 3 Boost Register

HS_P3_BOOST (0x6CCA)			USB PORT 3 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.35 USB Port 3 Varisense Register

PHY_P3_SENSE (0x6CCC)			USB PORT 3 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.36 USB3 Port 3 Link State

SS_P3_STATE (0x6DC0)			USB3 PORT 3 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to USB3 Link States for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to USB3 Link States for more details.

Table 3.37 USB Port 4 Boost Register

HS_P4_BOOST (0x70CA)			USB PORT 4 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.38 USB Port 4 Varisense Register

PHY_P4_SENSE (0x70CC)			USB PORT 4 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.39 USB3 Port 4 Link State

SS_P4_STATE (0x71C0)			USB3 PORT 4 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to USB3 Link States for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to USB3 Link States for more details.

Table 3.40 USB Port 5 Boost Register

HS_P5_BOOST (0x74CA)			USB PORT 4 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.41 USB Port 5 Varisense Register

PHY_P5_SENSE (0x74CC)			USB PORT 5 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.42 USB Port 6 Boost Register

HS_P6_BOOST (0x78CA)			USB PORT 6 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.43 USB Port 6 Varisense Register

PHY_P6_SENSE (0x78CC)			USB PORT 6 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved

Table 3.43 USB Port 6 Varisense Register

PHY_P6_SENSE (0x78CC)			USB PORT 6 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

Table 3.44 USB Port 7 Boost Register

HS_P7_BOOST (0x7CCA)			USB PORT 7 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3'b000: Nominal 3'b001: Decrease by 5% 3'b010: Increase by 10% 3'b011: Increase by 5% 3'b100: Increase by 20% 3'b101: Increase by 15% 3'b110: Increase by 30% 3'b111: Increase by 25%

Table 3.45 USB Port 7 Varisense Register

PHY_P4_SENSE (0x7CCC)			USB PORT 7 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

3.3.1.4 USB3 Link States

Table 3.46 USB3 Link States

NUM	LINK STATE	LINK SUB STATES
00h	U0	-
01h	U1	-
02h	U2	-
03h	U3	-
04h	SIS.Disabled	00h = Power3 01h = Power3A 02h = Main
05h	RX.Detect	00h = Init 01h = Power2 02h = Reset 03h = Reset_T 04h = Active0 05h = Active1 06h = Quiet
06h	SS.Inactive	00h = Reset 01h = Power2 02h = Quiet0 03h = Quiet1 04h = Disconnect Detect0 05h = Disconnect Detect1
07h	Polling	00h = Reset 01h = Power0 02h = LFPS 03h = RXEQ 04h = Active 05h = Configuration 06h = Idle
08h	Recovery	00h = ResetT 01h = Power0 02h = Active 03h = Configuration 04h = Idle
09h	Hot Reset	00h = Reset 01h = Go 02h = Active1 03h = Active2 04h = Exit
0Ah	Compliance	-
0Bh	Loopback	-

4 Configuration File

The USB553XB can be customized to meet various system requirements. To do this, the hub needs to be able to change the device descriptors based on the configuration, before the hub has entered

the attach state. The Configuration File contains a series of commands that hub executes to manipulate the registers used during enumeration. This includes the ID numbers, various strings, and how the downstream ports are connected.

The contents of the configuration file need to be written to the main memory of the part starting at address 001Eh. After the configuration data is in memory, the USB Attach commands will cause the configuration commands to be executed before enumeration. The commands can also be permanently added to the part through the OTP program command.

4.1 Configuration File Format

Configuration files are used for programming registers that are loaded upon sending the USB Attach command. Most registers require configuration via this method. If registers are written to prior to USB attach, the hub will overwrite these values with internal defaults. Writing to registers after USB attach will either have no effect or is otherwise not supported for many registers. Loading configuration files allows the hub to override the default configuration and to properly load the registers prior to USB attach.

The configuration area is 2017 bytes and contains multiple configuration blocks. A configuration block consists of a header area, metadata area, and a data area. The metadata area contains the commands necessary to interpret the data properly so the order of the data is critical.

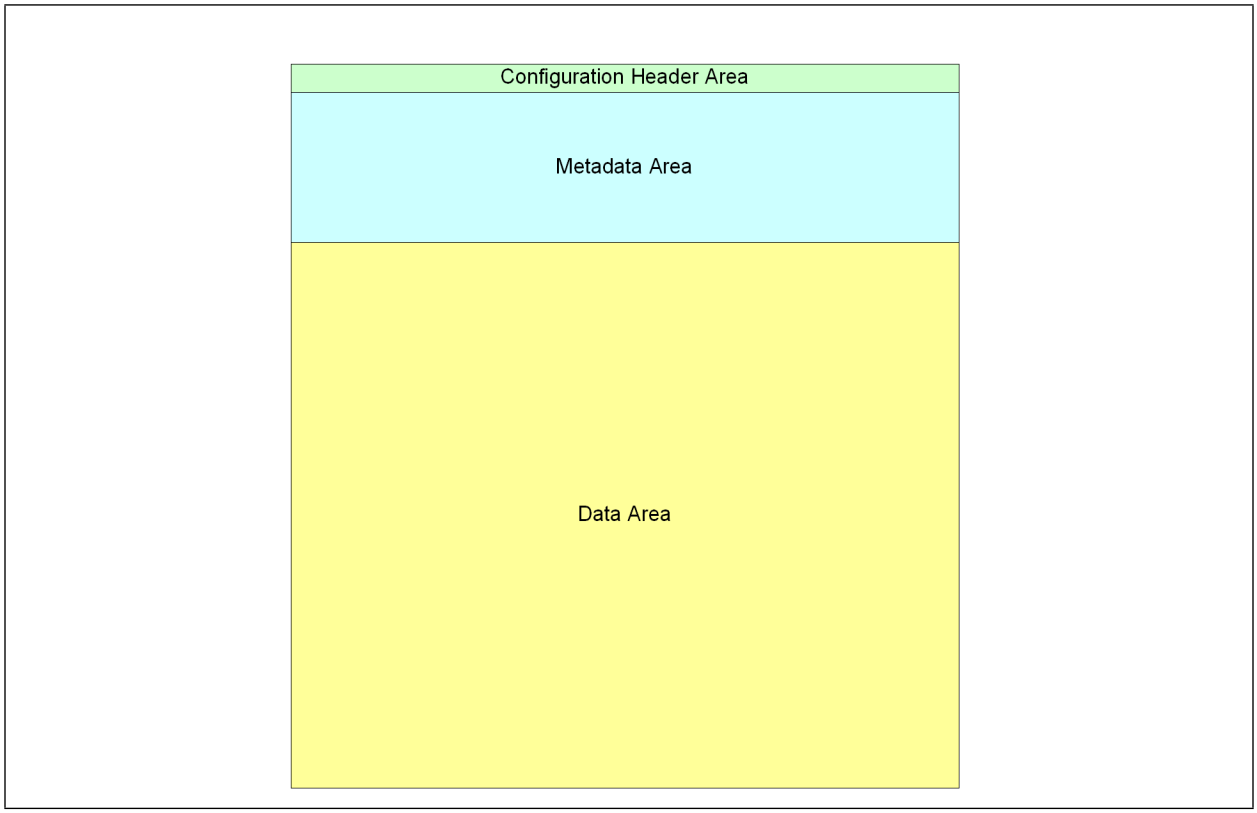

Figure 4.1 Configuration Block

4.1.1 Header Format

The header is a constant pattern followed by the number of metadata entries in the block.

Table 4.1 Configuration Block Header

Byte	Value	Notes
0	43h	‘C’
1	46h	‘F’
2	47h	‘G’
3	42h	‘B’
4	00h-FFh	Metadata Entries 0-255

4.1.2 Metadata Format

Each metadata entry is comprised of a 13-bit data command and an 11-bit data size field. The two fields are spread across three 8-bit registers as follows:

Table 4.2 Metadata

BIT/ BYTE	7	6	5	4	3	2	1	0
0	Data Command [12:5]							
1	Data Command [4:0]					Data Size [10:8]		
2	Data Size [7:0]							

4.1.3 Data Format

The data is formatted based on the Data Command in the metadata section. The order of the data must match the order of the metadata commands.

Table 4.3 Configuration File Commands

COMMAND	DESCRIPTION	DATA SIZE	DATA FORMAT
800h	Writes the data value to one register address.	3 Bytes	0 = Address MSB 1 = Address LSB 2 = Data
801h	Write the data values to two sequential register.	4 Bytes	0 = Address MSB 1 = Address LSB 2 = Data0 3 = Data1

Table 4.3 Configuration File Commands

COMMAND	DESCRIPTION	DATA SIZE	DATA FORMAT
802h	Write the data values to four sequential registers.	6 Bytes	0 = Address MSB 1 = Address LSB 2 = Data0 3 = Data1 4 = Data2 5 = Data3
803h	Write an array of data values to sequential registers.	N Bytes	0 = Address MSB 1 = Address LSB 2 = Length MSB 3 = Length LSB 4 = Data0 .. N-1 = Data[Length]
80Fh	Clear specific bits in a register. Bits are set to 1 to clear the bit.	3 Bytes	0 = Address MSB 1 = Address LSB 2 = Bit Mask
810h	Set specific bits in a register. Bits are set to 1 to clear the bit.	3 Bytes	0 = Address MSB 1 = Address LSB 2 = Bit Mask

4.1.4 Example Configuration File

The following is a simple configuration block that changes how the hub is configured:

Table 4.4 Example Configuration File

BYTE	DATA	NOTE
0	43h	‘C’
1	46h	‘F’
2	47h	‘G’
3	42h	‘B’
4	04h	4 Metadata Commands.
5	40h	Command 1: 802h Write 4 values to the VID and PID registers.
6	10h	
7	06h	Data Size 1: 6 bytes.
8	40h	Command 2: 810h Set the port disable bit in USB register.
9	80h	
10	03h	Data Size 2: 3 bytes.
11	40h	Command 3: 803h Write ‘SMSC’ to the manufacturer string.
12	18h	

Table 4.4 Example Configuration File

BYTE	DATA	NOTE
13	12h	Data Size 3: 12 bytes.
14	40h	Command 4: 800h Write to manufacturer string length.
15	00h	
16	03h	Data Size 4: 3 bytes.
17	30h	MSB of address **30**00h.
18	00h	LSB of address 30**00h.**
19	24h	VID 04**24**h LSB.
20	04h	VID **04**24h MSB.
21	34h	PID 21**34**h LSB.
22	21h	PID **21**34h MSB.
23	30h	MSB of address **30**0Ah.
24	0Ah	LSB of address 30**0A**h**.**
25	10h	Set bit 4 to disable port 4.
26	30h	MSB of address **30**16h.
27	16h	LSB of address 30**16**h.
28	00h	MSB of length 8 bytes.
29	08h	LSB of lenght 8 bytes.
30	53h	‘S’
31	00h	Unicode is 16-bit.
32	4Dh	‘M’
33	00h	Unicode is 16-bit.
34	53h	‘S’
35	00h	Unicode is 16-bit.
36	43h	‘C’
37	00h	Unicode is 16-bit.
38	30h	MSB of address **30**13h.
39	13h	LSB of address 30**13**h.
40	04h	String Length of 4 characters.

4.2 Configuration File Registers

The following registers must be manipulated through the configuration file to ensure they are loaded during enumeration. The INIT column is the values that are loaded by default.

Table 4.5 Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
0951h	R/W	BC_ENABLE	Downstream Battery Charging Enable	00h
0952h	R/W	APL_MOD	Apple Charging Mode	00h
3000h	R/W	USB2_VIDL	USB2 Vendor ID LSB	24h
3001h	R/W	USB2_VIDM	USB2 Vendor ID MSB	04h
3002h	R/W	USB2_PIDL	USB2 Product ID LSB	3Xh
3003h	R/W	USB2_PIDM	USB2 Product ID MSB	21h
3004h	R/W	USB2_DIDL	USB2 Device ID LSB	00h
3005h	R/W	USB2_DIDM	USB2 Device ID MSB	50h
3006h	R/W	USB2_CFG1	USB2 Hub Configuration Data Byte 1	9Bh
3007h	R/W	USB2_CFG2	USB2 Hub Configuration Data Byte 2	20h
3008h	R/W	USB2_CFG3	USB2 Hub Configuration Data Byte 3	01h
3009h	R/W	USB2_NRD	USB2 Non-Removable Device	00h
300Ah	R/W	USB2_PDS	USB2 Port Disable for Self Powered Operation	00h
300Bh	R/W	USB2_PDB	USB2 Port Disable for Bus Powered Operation	00h
300Ch	R/W	USB2_MAXPS	Max Power For Self Powered Operation	00h
300Dh	R/W	USB2_MAXPB	Max Power For Bus Powered Operation	32h
300Eh	R/W	USB2_HCMCS	USB2 Max Current For Self Powered Operation	00h
300Fh	R/W	USB2_HCMCB	USB2 Max Current For Bus Powered Operation	32h
3010h	R/W	USB2_PWRT	USB2 Power-On Time Register	32h
3011h	R/W	USB2_LANG_ID_H	USB2 Language ID High Register	04h
3012h	R/W	USB2_LANG_ID_L	USB2 Language ID Low Register	09h
3013h	R/W	USB2_MFR_STR_LEN	USB2 Manufacturer String Length Register	04h
3014h	R/W	USB2_PRD_STR_LEN	USB2 Product String Length Register	07h
3015h	R/W	USB2_SER_STR_LEN	USB2 Serial String Length Register	00h
3016h~ 3053h	R/W	USB2_MAN_STIRNG	USB2 Manufacturer String	Range

Table 4.5 Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
3054h-3091h	R/W	USB2_PRD_STRING	USB2 Product String	Range
3092h-30CFh	R/W	USB2_SER_STRING	USB2 Serial String	Range
30FAh	R/W	PRTSP	Hub Port Swap Register	00h
30FBh	R/W	HUB_PRT_REMAP_12	Hub Port Remap12 Register	00h
30FCh	R/W	HUB_PRT_REMAP_34	Hub Port Remap34 Register	00h
30FDh	R/W	HUB_PRT_REMAP_56	Hub Port Remap56 Register	00h
30FEh	R/W	HUB_PRT_REMAP_7	Hub Port Remap7 Register	00h
3844h	R/W	USB3_HUB_CONFIG	USB3 Hub Control	01h
5040h	R/W	USB3_DEV_DES_LEN	USB3 Serial String Bytes	12h
5041h	R/W	USB3_DEV_DES_TYP	USB3 Manufacturer String Bytes	01h
5042h	R/W	USB3_DEV_DES_USBL	USB3 Product String Length	00h
5048h	R/W	USB3_DEV_DES_VIDL	USB3 Device Descriptor VID LSB	24h
5049h	R/W	USB3_DEV_DES_VIDM	USB3 Device Descriptor VID MSB	04h
504Ah	R/W	USB3_DEV_DES_PIDL	USB3 Device Descriptor PID LSB	3Xh
504Bh	R/W	USB3_DEV_DES_PIDM	USB3 Device Descriptor PID MSB	55h
504Ch	R/W	USB3_DEV_DES_DIDL	USB3 Device Descriptor DID LSB	00h
504Dh	R/W	USB3_DEV_DES_DIDM	USB3 Device Descriptor DID MSB	50h
504Eh	R/W	USB3_DEV_DES_MAN	USB3 Descriptor Manufacturer Index	02h
5054F	R/W	USB3_DEV_DES_PROD	USB3 Descriptor Product Index	00h
5050h	R/W	USB3_DEV_DES_SN	USB3 Descriptor Serial Index	00h
505Bh	R/W	USB3_CON_DES_ATT	USB3 Configuration Attributes	E0h
50A3h	R/W	USB3_HUB_DES_CHAR_L	USB3 Hub Characteristics	09h
50A5h	R/W	USB3_HUB_DES_PWRT	USB3 Power On Time	30h
50A6h	R/W	USB3_HUB_DES_CRNT	USB3 Hub Max Current	00h
50B4h	R/W	USB3_SER_LEN	USB3 Serial String Length	1Ah
50B6h-50F3h	R/W	USB3_SER_STRING	USB3 Serial String	Range
50F4h	R/W	USB3_MAN_LEN	USB3 Manufacturer String Length	0Ah

Table 4.5 Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
50F6h-5133h	R/W	USB3_MAN_STRING	USB3 Manufacturer String	Range
5134h	R/W	USB3_PRD_LEN	USB3 Product String Length	10h
5136h-5173h	R/W	USB3_PRD_STRING	USB3 Product String	Range
5243h	R/W	STRAP_DIS	Pin Strap Disable	32h
525Ah	R/W	OCS_PORT_GANG	OCS Gang Control	00h

4.2.1 Register Definitions

4.2.1.1 Downstream Battery Charging Registers

Table 4.6 Downstream Battery Charging Enable

BC_ENABLE (0x0951)			DOWNSTREAM BATTERY CHARGING ENABLE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	Reserved	R/W	Reserved
6	P7_EN	R/W	Enable Battery Charging on Port 7
5	P6_EN	R/W	Enable Battery Charging on Port 6
4	P5_EN	R/W	Enable Battery Charging on Port 5
3	P4_EN	R/W	Enable Battery Charging on Port 4
2	P3_EN	R/W	Enable Battery Charging on Port 3
1	P2_EN	R/W	Enable Battery Charging on Port 2
0	P1_EN	R/W	Enable Battery Charging on Port 1

Note: To enable battery charging through this register the PIN_STRAP_DISABLE bit in Register 5243h must be 0.

Table 4.7 Apple Charging Mode

APL_MOD (0x0952)			APPLE CHARGING MODE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	Reserved	R/W	Reserved

Table 4.7 Apple Charging Mode

APL_MOD (0x0952)			APPLE CHARGING MODE
6	P7_APL	R/W	0 = Apple 1A profile is generated on the Port 7 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 7 DP/DM pins when the upstream port is not enumerated.
5	P6_APL	R/W	0 = Apple 1A profile is generated on the Port 6 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 6 DP/DM pins when the upstream port is not enumerated.
4	P5_APL	R/W	0 = Apple 1A profile is generated on the Port 5 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 5 DP/DM pins when the upstream port is not enumerated.
3	P4_APL	R/W	0 = Apple 1A profile is generated on the Port 4 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 4 DP/DM pins when the upstream port is not enumerated.
2	P3_APL	R/W	0 = Apple 1A profile is generated on the Port 3 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 3 DP/DM pins when the upstream port is not enumerated.
1	P2_APL	R/W	0 = Apple 1A profile is generated on the Port 2 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 2 DP/DM pins when the upstream port is not enumerated.
0	P1_APL	R/W	0 = Apple 1A profile is generated on the Port 1 DP/DM pins when the upstream port is not enumerated, or the hub is suspended with nothing connected to the downstream port and remote wake-up disabled. 1 = Apple 2A profile is generated on the Port 1 DP/DM pins when the upstream port is not enumerated.

4.2.1.2 USB2.0 Hub Enumeration and Functionality Registers

Table 4.8 USB2 Vendor ID LSB

USB2_VIDL (0x3000)			USB2 VENDOR ID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	VID_LSB	R/W	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Implementors Forum).

Table 4.9 USB2 Vendor ID MSB

USB2_VIDM (0x3001)			USB2 VENDOR ID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	VID_MSB	R/W	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Implementors Forum).

Table 4.10 USB2 Product ID LSB

USB2_PIDL (0x3002)			USB2 PRODUCT ID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PID_LSB	R/W	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product.

Table 4.11 USB2 Product ID MSB

USB2_PIDM (0x3003)			USB2 PRODUCT ID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PID_MSB	R/W	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product.

Table 4.12 USB2 Device ID LSB

USB2_DIDL (0x3004)			USB2 DEVICE ID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	DID_LSB	R/W	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

Table 4.13 USB2 Device ID MSB

USB2_DIDM (0x3005)			USB2 DEVICE ID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	DID_MSB	R/W	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

Table 4.14 USB2 Hub Configuration Data Byte 1

USB2_CFG1 (0x3006)			USB2 HUB CONFIGURATION DATA BYTE 1
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	SELF_BUS_PWR	R/W	Self or Bus Power: Selects between Self- and Bus-Powered operation. The hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the SMSC hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available downstream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB2.0 specifications are not violated. When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current. 0 = Bus-Powered operation. 1 = Self-Powered operation.
6	Reserved	R/W	Reserved
5	HS_DISABLE	R/W	High Speed Disable: Disables the capability to attach as either a High/Full- speed device, and forces attachment as Full-speed only i.e. (no High-Speed support). 0 = High-/Full-Speed. 1 = Full-Speed-Only (High-Speed disabled!)
4	MTT_ENABLE	R/W	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) **Note:** The host may force Single-TT mode only. 0 = single TT for all ports. 1 = one TT per port (multiple TT's supported)

Table 4.14 USB2 Hub Configuration Data Byte 1

USB2_CFG1 (0x3006)			USB2 HUB CONFIGURATION DATA BYTE 1
BIT	**NAME**	**R/W**	**DESCRIPTION**
3	EOP_DISABLE	R/W	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected. 1 = EOP generation at EOF1 is disabled **Note:** This is normal USB operation. **Note:** This is a rarely used feature in the PC environment, existing drivers may not have been thoroughly debugged with this feature enabled. It is included because it is a permitted feature in Chapter 11 of the USB specification.
2:1	CURRENT_SNS	R/W	Over Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs) The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). 01 = Individual port-by-port. 1x = Over current sensing not supported. (must only be used with Bus-Powered configurations!)
0	PORT_PWR	R/W	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching.

Table 4.15 USB2 Hub Configuration Data Byte 2

USB2_CFG2 (0x3007)			USB2 HUB CONFIGURATION BYTE 2
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R/W	Reserved
5:4	OC_TIMER	R/W	Over Current Timer: Over Current Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 50 ns 01 = 100 ns 10 = 200 ns 11 = 400 ns

Table 4.15 USB2 Hub Configuration Data Byte 2

USB2_CFG2 (0x3007)			USB2 HUB CONFIGURATION BYTE 2
BIT	**NAME**	**R/W**	**DESCRIPTION**
3	COMPOUND	R/W	Compound Device: Allows the OEM to indicate that the hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a “Non-Removable Device”. **Note:** Declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 = No. 1 = Yes, hub is part of a compound device.
2:0	Reserved	R/W	Always read ‘0’

Table 4.16 USB2 Hub Configuration Data Byte 3

USB2_CFG3 (0x3008)			USB2 HUB CONFIGURATION BYTE 3
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved
3	PRTMAP_EN	R/W	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as Port ‘n’ on the hub is reported as Port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. ‘1’ = Port Re-Map mode. The mode enables remapping via the registers defined below. Disable the LPM to use this feature in USB2 Hub Control.
2:0	Reserved	R/W	Always read ‘0’

Table 4.17 USB2 Non-Removable Device

USB2_NRD (0x3009)			USB2 NON-REMOVABLE DEVICE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	NR_DEVICE	R/W	Non-Removable Device: Indicates which port(s) include non- removable devices. ‘0’ = port is removable, ‘1’ = port is non-removable. Informs the Host if one of the active ports has a permanent device that is nondetachable from the hub. **Note:** The device must provide its own descriptor data.) When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7= 1; Port 7 non-removable. Bit 6= 1; Port 6 non-removable. Bit 5= 1; Port 5 non-removable. Bit 4= 1; Port 4 non-removable. Bit 3= 1; Port 3 non-removable. Bit 2= 1; Port 2 non-removable. Bit 1= 1; Port 1 non removable. Bit 0 is Reserved, always = ‘0’.

Table 4.18 USB2 Port Disable for Self Powered Operation

USB2_PDS (0x300A)			USB2 PORT DISABLE FOR SELF POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PORT_DIS_SP	R/W	Port Disable Self-Powered: Disables 1 or more ports. ‘0’ = port is available, ‘1’ = port is disabled. During Self-Powered operation, when PRTMAP_EN = 1, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7= 1; Port 7 is disabled. Bit 6= 1; Port 6 is disabled. Bit 5= 1; Port 5 is disabled. Bit 4= 1; Port 4 is disabled. Bit 3= 1; Port 3 is disabled. Bit 2= 1; Port 2 is disabled. Bit 1= 1; Port 1 is disabled. Bit 0 is Reserved, always = ‘0’

Table 4.19 USB2 Port Disable for Bus Powered Operation

USB2_PDB (0x300B)			USB2 PORT DISABLE FOR BUS POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PORT_DIS_BP	R/W	Port Disable Bus-Powered: Disables 1 or more ports. '0' = port is available, '1' = port is disabled. During Bus-Powered operation, when PRTMAP_EN = 1, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7= 1; Port 7 is disabled. Bit 6= 1; Port 6 is disabled. Bit 5= 1; Port 5 is disabled. Bit 4= 1; Port 4 is disabled. Bit 3= 1; Port 3 is disabled. Bit 2= 1; Port 2 is disabled. Bit 1= 1; Port 1 is disabled. Bit 0 is Reserved, always = '0

Table 4.20 Max Power For Self Powered Operation

MAXPS (0x300C)			MAX CURRENT FOR SELF POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	MAX_PWR_SP	R/W	Max Power Self Powered: Value in 2mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. **Note:** The USB2.0 Specification does not permit this value to exceed 100mA

Table 4.21 Max Power For Bus Powered Operation

MAXPB (0x300D)			MAX POWER FOR BUS POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	MAX_PWR_BP	R/W	Max Power Bus Powered: Value in 2mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.

Table 4.22 USB2 Max Current For Self Powered Operation

USB2_HCMCS (0x300E)			USB2 MAX CURRENT FOR SELF POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	HC_MAX_C_SP	R/W	Hub Controller Max Current Self-Powered: Value in 1mA increments that the hub consumes from an upstream port (VBUS) when operating as a self- powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB2.0 Specification does not permit this value to exceed 100mA

Table 4.23 USB2 Max Current For Bus Powered Operation

USB2_HCMCB (0x300F)			USB2 MAX CURRENT FOR BUS POWERED OPERATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	HC_MAX_C_BP	R/W	Hub Controller Max Current Bus-Powered: Value in 1mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus- powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.

Table 4.24 USB2 Power-On Time Register

USB2_PWRT (0x3010)			USB2 POWER ON TIME REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	POWER_ON_TIME	R/W	Power On Time: The length of time that is takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port.

Table 4.25 USB2 Language ID High Register

USB2_LANG_ID_H (0x3011)			USB2 LANGUAGE ID HIGH REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	LANG_ID_H	R/W	USB LANGUAGE ID (Upper 8 bits of a 16 bit ID field)

Table 4.26 USB2 Language ID Low Register

USB2_LANG_ID_L (0x3012)			USB2 LANGUAGE ID LOW REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	LANG_ID_L	R/W	USB LANGUAGE ID (Lower 8 bits of a 16 bit ID field)

Table 4.27 USB2 Manufacturer String Length Register

USB2_MFR_STR_LEN (0x3013)			USB2 MANUFACTURER STRING LENGTH REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	MFR_STR_LEN	R/W	Manufacturer String Length Maximum string length is 31 characters.

Table 4.28 USB2 Product String Length Register

USB2_PRD_STR_LEN (0x3014)			USB2 PRODUCT STRING LENGTH REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PRD_STR_LEN	R/W	Product String Length Maximum string length is 31 characters.

Table 4.29 USB2 Serial String Length Register

USB2_SER_STR_LEN (0x3015)			USB2 SERIAL STRING LENGTH REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	SER_STR_LEN	R/W	Serial String Length Maximum string length is 31 characters.

Table 4.30 USB2 Manufacturer String

USB2_MAN_STRING (0x3016~0x3053)			USB2 MANUFACTURER STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	STRING	R/W	Manufacturer String. UNICODE UTF-16LE per USB 2.0 Specification The Manufacturer String is stored first starting at address 3016h and is allocated twice the number of bytes as specified in MFR_STR_LEN. The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering of your selected programming tools.

Table 4.31 USB2 Product String

USB2_PRD_STRING (0x3054~0x3091)			USB2 PRODUCT STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	STRING	R/W	Product String. UNICODE UTF-16LE per USB 2.0 Specification The Product String is stored first starting at address 3054h and is allocated twice the number of bytes as specified in PRD_STR_LEN. The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering of your selected programming tools.

Table 4.32 USB2 Serial String

USB2_SER_STRING (0x3092~0x30CF)			USB2 SERIAL STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	STRING	R/W	Serial String. UNICODE UTF-16LE per USB 2.0 Specification The Serial String is stored first starting at address 3092h and is allocated twice the number of bytes as specified in SER_STR_LEN. The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering of your selected programming tools.

4.2.1.3 USB2 Port Configuration Register

Table 4.33 Hub Port Swap Register

HUB_PRT_SWAP (0x30FA)			HUB PORT SWAP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	PRT_SWAP	R/W	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. '0' = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. '1' = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin Bit 7= '1': Port 4 DP/DM is Swapped. Bit 6= '1': Port 4 DP/DM is Swapped. Bit 5= '1': Port 4 DP/DM is Swapped. Bit 4= '1': Port 4 DP/DM is Swapped. Bit 3= '1': Port 3 DP/DM is Swapped. Bit 2= '1': Port 2 DP/DM is Swapped. Bit 1= '1': Port 1 DP/DM is Swapped. Bit 0= '1': Upstream Port DP/DM is Swapped

Table 4.34 Hub Port Remap12 Register

HUB_PRT_REMAP_12 (0x30FB)			HUB PORT SWAP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	PRT_2_MAP	R/W	0000 - Physical Port 2 is disabled 0001 - Physical Port 2 is mapped to Logical Port 1 0010 - Physical Port 2 is mapped to Logical Port 2 0011 - Physical Port 2 is mapped to Logical Port 3 0100 - Physical Port 2 is mapped to Logical Port 4 0101 - Physical Port 2 is mapped to Logical Port 5 0110 - Physical Port 2 is mapped to Logical Port 6 0111 - Physical Port 2 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value
3:0	PRT_1_MAP	R/W	0000 - Physical Port 1 is disabled 0001 - Physical Port 1 is mapped to Logical Port 1 0010 - Physical Port 1 is mapped to Logical Port 2 0011 - Physical Port 1 is mapped to Logical Port 3 0100 - Physical Port 1 is mapped to Logical Port 4 0101 - Physical Port 1 is mapped to Logical Port 5 0110 - Physical Port 1 is mapped to Logical Port 6 0111 - Physical Port 1 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CF_3 is set.

Table 4.35 Hub Port Remap34 Register

HUB_PRT_REMAP_34 (0x30FC)			HUB PORT SWAP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	PRT_4_MAP	R/W	0000 - Physical Port 4 is disabled 0001 - Physical Port 4 is mapped to Logical Port 1 0010 - Physical Port 4 is mapped to Logical Port 2 0011 - Physical Port 4 is mapped to Logical Port 3 0100 - Physical Port 4 is mapped to Logical Port 4 0101 - Physical Port 4 is mapped to Logical Port 5 0110 - Physical Port 4 is mapped to Logical Port 6 0111 - Physical Port 4 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value
3:0	PRT_3_MAP	R/W	0000 - Physical Port 3 is disabled 0001 - Physical Port 3 is mapped to Logical Port 1 0010 - Physical Port 3 is mapped to Logical Port 2 0011 - Physical Port 3 is mapped to Logical Port 3 0100 - Physical Port 3 is mapped to Logical Port 4 0101 - Physical Port 3 is mapped to Logical Port 5 0110 - Physical Port 3 is mapped to Logical Port 6 0111 - Physical Port 3 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

Table 4.36 Hub Port Remap56 Register

HUB_PRT_REMAP_34 (0x30FC)			HUB PORT SWAP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	PRT_6_MAP	R/W	0000 - Physical Port 6 is disabled 0001 - Physical Port 6 is mapped to Logical Port 1 0010 - Physical Port 6 is mapped to Logical Port 2 0011 - Physical Port 6 is mapped to Logical Port 3 0100 - Physical Port 6 is mapped to Logical Port 4 0101 - Physical Port 6 is mapped to Logical Port 5 0110 - Physical Port 6 is mapped to Logical Port 6 0111 - Physical Port 6 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value
3:0	PRT_5_MAP	R/W	0000 - Physical Port 5 is disabled 0001 - Physical Port 5 is mapped to Logical Port 1 0010 - Physical Port 5 is mapped to Logical Port 2 0011 - Physical Port 5 is mapped to Logical Port 3 0100 - Physical Port 5 is mapped to Logical Port 4 0101 - Physical Port 5 is mapped to Logical Port 5 0110 - Physical Port 5 is mapped to Logical Port 6 0111 - Physical Port 5 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value

Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

Table 4.37 Hub Port Remap7 Register

HUB_PRT_REMAP_34 (0x30FC)			HUB PORT SWAP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R	Reserved
3:0	PRT_7_MAP	R/W	0000 - Physical Port 7 is disabled 0001 - Physical Port 7 is mapped to Logical Port 1 0010 - Physical Port 7 is mapped to Logical Port 2 0011 - Physical Port 7 is mapped to Logical Port 3 0100 - Physical Port 7 is mapped to Logical Port 4 0101 - Physical Port 7 is mapped to Logical Port 5 0110 - Physical Port 7 is mapped to Logical Port 6 0111 - Physical Port 7 is mapped to Logical Port 7 1000 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

Table 4.38 USB3 Hub Control

USB3_HUB_CTL (0x3844)			USB3 HUB CONTROL
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R/W	Reserved
5:4	USB3_OC_TIMER	R/W	USB 3.0 Over Current Timer: Over Current Timer delay when operating in USB 3.0 mode. 00b: 750 ns 01b: 1000 ns 10b: 1250 ns 11b: 1500 ns
3	USB3_GANG_EN	R/W	When high, all usb3 downstream ports will have power turned on if host enables power on any of the usb3 downstream ports. When low. individual power switching is enabled. **Note:** If a port is to be disabled in GANG mode, the PRT_SEL for that port must be set to 0x0 to disable port power
2:1	Reserved	R/W	Reserved
0	PWR_SW_CTL	R/W	When set high, the USB 3.0 Downstream Facing Hub Port State Machine assumes downstream power switches are supported. When set low , the USB 3.0 Downstream Facing Hub Port State Machine assumes downstream power switches are not supported. **Note:** If USB3 Power On Time is set to 0, then this bit must also be set to 0.

4.2.1.4 USB3 Descriptors

Table 4.39 USB3 Serial String Bytes

USB3_SER_STR (0x5014)			USB3 SERIAL STRING BYTES
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_SER_BTYE	R/W	The number of bytes in the Serial string + 2 for the string length and type. For example, if there are 10 Unicode characters in the string then the contents of this register would be 2*10 + 2 or 22 bytes. This is how many bytes of memory will be moved to the string descriptor starting at address 0x50B6.

Table 4.40 USB3 Manufacturer String Bytes

USB3_MAN_STR (0x5018)			USB3 MANUFACTURER STRING BYTES
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_MAN_BYTE	R/W	The number of bytes in the Manufacturer string + 2 for the string length and type. For example, if there are 10 Unicode characters in the string then the contents of this register would be 2*10 + 2 or 22 bytes. This is how many bytes of memory will be moved to the string descriptor starting at address 0x50F6.

Table 4.41 USB3 Product String Length

USB3_PRD_STR (0x501C)			USB3 PRODUCT STRING LENGTH
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PRD_IND	R/W	The number of bytes in the Product string + 2 for the string length and type. For example, if there are 10 Unicode characters in the string then the contents of this register would be 2*10 + 2 or 22 bytes. This is how many bytes of memory will be moved to the string descriptor starting at address 0x5136.

Table 4.42 USB3 Device Descriptor VID LSB

USB3_DEV_DES_VIDL (0x5048)			USB3 DEVICE DESCRIPTOR VID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_VIDL	R/W	USB3 Vendor ID LSB

Table 4.43 USB3 Device Descriptor VID MSB

USB3_DEV_DES_VIDM (0x5049)			USB3 DEVICE DESCRIPTOR VID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_VIDM	R/W	USB3 Vendor ID MSB

Table 4.44 USB3 Device Descriptor PID LSB

USB3_DEV_DES_PIDL (0x504A)			USB3 DEVICE DESCRIPTOR PID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PIDL	R/W	USB3 Product ID LSB

Table 4.45 USB3 Device Descriptor PID MSB

USB3_DEV_DES_PIDM (0x504B)			USB3 DEVICE DESCRIPTOR PID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PIDM	R/W	USB3 Product ID MSB

Table 4.46 USB3 Device Descriptor DID LSB

USB3_DEV_DES_DIDL (0x504C)			USB3 DEVICE DESCRIPTOR DID LSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_DIDL	R/W	USB3 Device ID LSB

Table 4.47 USB3 Device Descriptor DID MSB

USB3_DEV_DES_DIDM (0x504D)			USB3 DEVICE DESCRIPTOR DID MSB
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_DIDM	R/W	USB3 Device ID MSB

Table 4.48 USB3 Descriptor Manufacturer Index

USB3_DEV_DES_MAN (0x504E)			USB3 DESCRIPTOR MANUFACTURER INDEX
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_MAN_IND	R/W	0 = No manufacturer string supported. 2 = USB3 string at index 2 is the manufacturer string.

Table 4.49 USB3 Descriptor Product Index

USB3_DEV_DES_PRD (0x504F)			USB3 DESCRIPTOR PRODUCT INDEX
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PRD_IND	R/W	0 = No product string supported. 3 = USB3 string at index 3 is the product string.

Table 4.50 USB3 Descriptor Serial Index

USB3_DEV_DES_SER (0x5050)			USB3 DESCRIPTOR SERIAL INDEX
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_SER_IND	R/W	0 = No serial string supported. 1 = USB3 string at index 1 is the serial string.

Table 4.51 USB3 Configuration Attributes

USB3_MAN_STR_LEN (0x505B)			USB3 MANUFACTURER STRING LENGTH
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	Reserved	R/W	Must always be set to 1
6	SELF_POWER	R/W	0 = Bus-Powered operation. 1 = Self-Powered operation.
5	REMOTE_WAKE	R/W	0 = Remote Wakeup not supported. 1 = Remote Wakeup supported. This value should always be 1.
4:0	Reserved	R	Reserved

Table 4.52 USB3 Hub Characteristics

USB3_HUB_DES_CHAR_L (0x50A3)			USB3 HUB CHARACTERISTICS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R/W	Reserved
4:3	OCS_MODE	R/W	00 = Global Over-Current Protection. 01 = Individual Over-Current Protection. 1X = No Over-Current Protection.
2	COMPOUND	R/W	0 = Hub is not part of a compound device. 1 = Hub is part of a compound device.
1:0	PRT_PWR_MODE	R/W	00 = Ganged Port Power Control. 01 = Individual Port Power Control. 1X = Reserved.

Table 4.53 USB3 Power On Time

USB3_HUB_DES_PWRT (0x50A5)			USB3 POWER ON TIME
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	POWER_ON_TIME	R/W	Time (in 2 ms intervals) from the time the power-on sequence begins on a port until power is good on that port. See Section 11.23.2.1 in the USB Specification.

Table 4.54 USB3 Hub Max Current

USB3_HUB_DES_CRNT (0x50A6)			USB3 HUB MAX CURRENT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	MAX_CURRENT	R/W	Hub Controller Max Current: Value in 1mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.

Table 4.55 USB3 Serial String Length

USB3_SER_STR_LEN (0x50B4)			USB3 SERIAL STRING LENGTH
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_SER_LEN	R/W	Number of Unicode characters in the serial string.

Table 4.56 USB3 Serial String

USB3_SER_STRING (0x50B6-0x50F3)			USB3 SERIAL STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_SER_STR	R/W	The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner).

Table 4.57 USB3 Manufacturer String Length

USB3_MAN_STR_LEN (0x50F4)			USB3 MANUFACTURER STRING LENGTH
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_MAN_LEN	R/W	Number of Unicode characters in the serial string.

Table 4.58 USB3 Manufacturer String

USB3_MAN_STRING (0x50F6-0x5133)			USB3 MANUFACTURER STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_MAN_STR	R/W	The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner).

Table 4.59 USB3 Product String Length

USB3_PRD_STR_LEN (0x5134)			USB3 PRODUCT STRING LENGTH
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PRD_LEN	R/W	Number of Unicode characters in the product string.

Table 4.60 USB3 Product String

USB3_PRD_STRING (0x5136-0x5173)			USB3 PRODUCT STRING
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	USB3_PRD_STR	R/W	The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner).

4.2.1.5 General Hub Configuration

Table 4.61 Pin Strap Disable

STRAP_DIS (0x5243)			PIN STRAP DISABLE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R/W	Reserved
5	PIN_STRAP_DIS	R/W	0 = Pin strapping is enabled. 1 = Pin strapping is disabled, all battery charging, non-removable and port disable options must be configured through SMBus.
4:0	Reserved	R/W	Reserved

Table 4.62 OCS Pin Select

OCS_SELECT (0x525A)			OCS GANG CONTROL
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:0	OCS_SEL	R/W	The physical pin that will be used to receive the OCS events for the ganged ports. 11h = OCS 1 Pin 12h = OCS 2 Pin 13h = OCS 3 Pin 14h = OCS 4 Pin

5 SPI Pass-through

When the SMBus Slave receives the SPI Pass-through command, it executes a SPI transaction over the SPI Master bus. The purpose of this functionality is to be able to read and write to SPI EEPROM's attached to the USB553x's SPI Master interface.

The SPI Pass-through functionality supports arbitrary SPI transactions. Please refer to the SPI flash documentation for details of commands to be used with your SPI device.

USB553xB firmware operation must be transferred to the Internal ROM prior to performing a SPI Pass-through operation. The reason for this is the SPI Pass-through operations cause transactions to be performed on the SPI interface; these transactions would interfere with external firmware execution if the firmware were to be running from the SPI ROM. The Reboot DFU command (opcode 9938h) should be used for this purpose.

The SPI Pass-through Command Opcode is 9935h. Upon receiving the SPI Pass-through Command, the USB553x interprets the contents at RAM offset 0 to have the following format:

Table 5.1 SPI Pass-through Command

RAM ADDRESS	SIZE	NAME	DESCRIPTION
0000h	1	Direction	The direction of the SPI data stage on the SPI bus for this SPI transaction. 0 = The USB553xB will write from the data field to the SPI external EEPROM. 1 = The USB553xB will read from the external SPI EEPROM to the data field.
0001h	1	Command Length	The number of bytes that the USB553xB will send as a command from the SPI Command field to the external SPI EEPROM.
0002h	8	SPI Command	This buffer holds the command that the USB553xB will transmit over its SPI Master bus for this transaction.
000Ah	1	Data Length	The amount of data to write or read to/from the external SPI EEPROM during the data stage.
000Bh	128	Data	This is the data buffer for the SPI transaction. The Data Length field determines the number of bytes the USB553xB will read/write from this buffer during the SPI transaction. When Direction=0, the USB553xB will write the contents of this buffer to the SPI EEPROM. When Direction=1, the USB553xB will read from the SPI EEPROM and place the data into this buffer.

5.0.1 Example: Fast Read 256 bytes from SPI EEPROM address F000h

1. Send Reboot DFU Command to the USB553xB to reboot to internal ROM.
2. Write the following data structure to RAM offset 0 for a Fast Read command:
   a. spi_data_direction = 1

b. spi_command_length = 5

c. spi_command =

- JEDEC spi_fast_read_opcode = 0Bh
- SPI address 23:16 = 00h
- SPI address 15:8 = F0h
- SPI address 8:0 = 00h
- Dummy byte = 00h

d. data_length = 128

3. Send the SPI Passthrough Command to the USB553xB.
4. Read 128 bytes of RAM from the USB553xB beginning at offset 0Bh. This is the data from the SPI flash.
5. Repeat the above procedure, loading the SPI Pass-through command structure with SPI address F080h for the remaining 128 bytes.

6 Extended commands

The extended commands provide access to the status of the USB553XB. From these registers a SMBus controller can see the connection status of the hub, communicate with the UCS1000, and change the SMBus address if desired. When the extended command is sent the hub will interpret the memory starting at offset 00h as follows:

Table 6.1 Memory Format for Configuration Register Access

RAM Address	Description	Notes
0000h	Command	Code of the extended command to execute.
0001h	Status	Always write 0 to this register, it will be updated after the command is executed with the status.
0002h	Data1	The first byte of data to write to or read from when executing the command.
...	...	...
0004h+N	DataN	The Nth byte of data to write to or read from when executing the command.

6.0.1 Extended Command Example

The following example shows how to read the Charger Detection register to find out what type of charger the hub has connected to:

1. First write data to the memory of the hub.

Table 6.2 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.

Table 6.2 Example SMBus Write Command

BYTE	VALUE	COMMENT
2	00h	Memory address 00**00**h.
3	03h	Number of bytes to write to memory.
4	80h	Get Port Device Status.
5	00h	Reading one data bytes.
6	1Fh	Read all ports.

2. After the data is written, execute the Configuration Register Access command.

Table 6.3 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**3Eh.
2	3Eh	Command 99**3E**h.
3	00h	Command Completion.

3. Finally, read back data starting at memory offset 04h, which is where the Data byte starts.

Table 6.4 Example SMBus Read Command

BYTE	VALUE	COMMENTS
0	5Ah	Address plus Write bit.
1	00h	Memory Address **00**04h.
2	03h	Memory Address 00**04**h.
0	59h	Address plus Read bit.
1	80h	Device sends 128 bytes of data.
2	03h	Upstream Connection Status. (SS and HS)
3	02h	Port 1 Connection Status. (HS/FS/LS Only)
4	01h	Port 2 Connection Status. (SS Only)
5	02h	Port 3 Connection Status.(HS/FS/LS Only)
6	02h	Port 4 Connection Status.(HS/FS/LS Only)

4. Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set, the SMBus Master can send a stop at any time.

6.1 Extended Commands

Below is a list of the extended commands and the code used to execute them.

Table 6.5 Extended Commands

COMMAND	CODE
Set Address	00h
Get Default Address	01h
Get Hub Info	02h
Get UCS Port Mask	03h
Port Connect Status	80h
Port Power Status	81h
Port Force Disable	82h
Port DP/DM Status	83h
UCS Byte Read	84h
UCS Byte Write	85h
UCS Block Read	86h
UCS Block Write	87h

6.1.1 Command Descriptions

6.1.1.1 Set Address (00h)

The set address command will change the SMBus address to the value in Data1 or memory address 0002h. The next SMBus read will have to account for this change in address.

Table 6.6 Set Address Byte

SET ADDR (0x00)			SMBUS ADDRESS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	DEFAULT	W	Resets to the default SMBus address.
7:0	ADDRESS	W	New SMBus Address

6.1.1.2 Get Default Address (01h)

This command will always return the default address of the USB553XB (2dh).

6.1.1.3 Get Hub Info (02h)

The command will return the status of the hub in Data1. The status byte follows the following format:

Table 6.7 Hub Information

USB2_HUB_INFO (0x02)			USB2 HUB INFORMATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	CONFIGURED	R	1 = Hub is in the configured state. 2 = Hub is in the unconfigured state.
6:0	USB2_ADDRESS	R	The address of the USB2 hub.

6.1.1.4 Get UCS Port Mask(03h)

This will return a mask of which port is assigned a UCS port controller based on the UCS device detection.

6.1.1.5 Port Connect Status (80h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port connect status byte can be interpreted as follows:

Table 6.8 Hub Information

PORT_CONNECT (0x80)			PORT CONNECT STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R	Reserved
5	USB2_SUSPEND	R	0 = Port is not suspended. 1 = Port is in the L2 Suspend State.
4	USB3_SUSPEND	R	0 = Port is not suspended. 1 = Port is in the U3 Suspend State.
3:2	Reserved	R	Reserved
1	USB2_CONNECT	R	0 = No USB2 connection detected. (HS/FS/LS) 1 = USB2 connection detected.
0	USB3_CONNECT	R	0 = No USB3 connection detected. 1 = USB3 connection detected.

6.1.1.6 Port Power Status (81h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port. A ‘1’ means the port power is enabled, a ‘0’ means the port power is disabled.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc

6.1.1.7 Port Force Disable (82h)

Data1 of the memory is the port mask and Data 2-6 is the port disable state requested.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port disable byte will be interpreted as follows:

Table 6.9 Hub Information

PORT_DISABLE (0x82)			**PORT DISABLE**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	OVERWRITE	W	If this bit is 1 then the data in bits 2:0 will be overwritten.
6:3	Reserved	W	Reserved
2	FORCE_OFF	W	0 = Port Power controlled by hub. 1 = Port Power forced off.
1	USB3_TERM_DIS	W	0 = USB3 Terminations controlled by hub. 1 = USB3 Terminations disabled.
0	USB2_TERM_DIS	W	0 = USB2 Terminations controlled by hub. 1 = USB2 Terminations disabled.

6.1.1.8 Port DP/DM Status (83h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port DP/DM status byte can be interpreted as follows:

Table 6.10 Port DP/DM Status

PORT_DPDM (0x83)			PORT DP/DM STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:2	Reserved	W	Reserved
1	FS_DM	W	0 = DM line is below the FS threshold. 1 = DM line is above the FS threshold (LS idle state)
0	FS_DP	W	0 = DP line is below the FS threshold. 1 = DP line is above the FS threshold. (FS idle state)

6.1.1.9 UCS Byte Read (84h)

The first data byte (Data1) contains the address of the UCS register to read. The second data byte (Data2) will contain the data after the command is executed.

6.1.1.10 UCS Byte Write (85h)

The first data byte (Data1) contains the address of the UCS register to write to. The second data byte (Data2) contains the data to be written.

6.1.1.11 UCS Block Read (86h)

The first data byte (Data1) contains the address of the UCS register to read. The second data byte (Data2) contains the number of bytes to read. The subsequent data bytes will be populated with the contents of the Data2 registers starting at Data1.

6.1.1.12 UCS Block Write (87h)

The first data byte (Data1) contains the address of the UCS register to write to. The second data byte (Data2) contains the number of bytes to write. The subsequent data bytes contain the data to write.

7 Revision History

Revision	Section	Changes
Revision 1.0 (06-21-13)	Initial Revision	