# ENT-AN0106

# Application Note

# SimpliPHY Architecture Advantages

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# Contents

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.1

In revision 1.1 of this document, the Voltage-Mode Line Driver diagram was updated. For more information, see Voltage-Mode Line Driver.

Revision 1.0

Revision 1.0 was the first publication of this document.

# 2 SimpliPHY Architecture Advantages

This document provides an overview of SimpliPHY Gigabit Ethernet Copper PHY architecture. It describes why this innovative design, utilizing a voltage-mode line driver and a fully adaptive digital signal processor, has allowed Microsemi Corporation to continue a leadership position in lowest-power Gigabit Ethernet PHYs. Refer to the IEEE standard 802.3 CSMA/CD Access Method and Physical Layer Specification for supporting information.

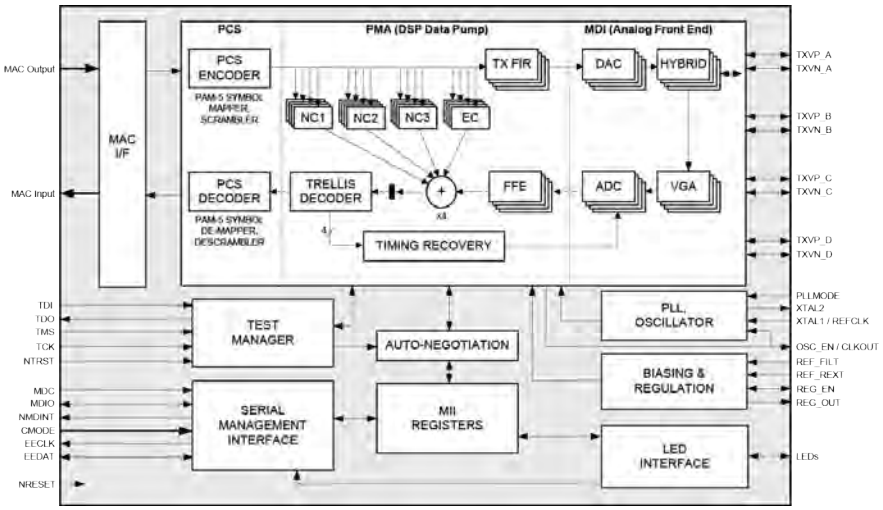
## 2.1 SimpliPHY Overview

The SimpliPHY family of 10/100/1000BASE-T PHYs all share a unique architecture with the following advantages:

- Analog Front End (AFE)
- Digital Signal Processor (DSP)
- Innovative PHY features

The following illustration shows the SimpliPHY architecture blocks.

**Figure 1 • Block Diagram**




### 2.1.1 Lowest-Power PHY Architecture

The first generation of 1000BASE-T Copper PHYs were introduced in 0.35 µ CMOS and consumed over 5 W with the largest power demand coming from the DSP. Today, Gigabit Ethernet vendors have managed to reduce that high power to less than a tenth of the original levels through reducing the area of the DSP, lowering the voltage supplies of the AFE, and reducing CMOS process geometries. In recent advanced CMOS fabrication processes, the AFE has replaced the DSP as the dominant power consumer of the entire PHY. The ability to achieve substantial power savings beyond the 0.13 µ process became more difficult because the AFE does not scale in proportion to the digital portion of the PHY. This was one of the reasons a voltage-mode line driver was chosen as the best way to ensure the lowest-power PHY in the market (regardless of the process).

## 2.2 Analog Front End (AFE)

The advantage of the SimpliPHY AFE is that it utilizes Microsemi's voltage-mode line driver and contains integrated termination resistors.

### 2.2.1 Voltage-Mode Line Driver

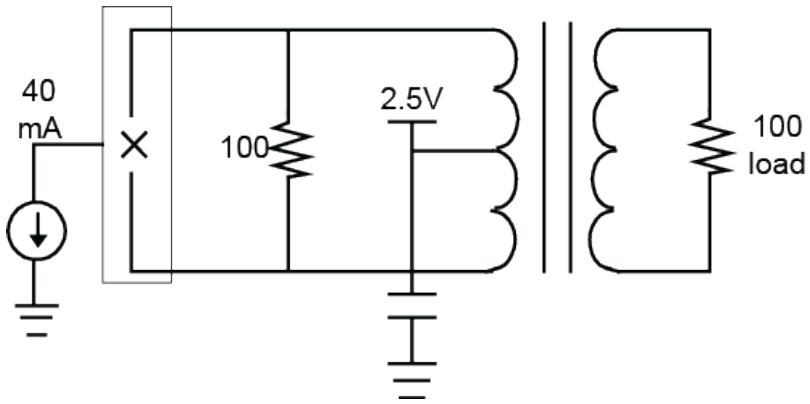
There are two architectural options for a line driver in a 1000BASE-T Copper PHY:

- Current-mode line driver
- Voltage-mode line driver

### 2.2.1.1 What is a Current-Mode Line Driver?

The current-mode line driver usually consists of a single-ended current source of approximately 40 mA. This source will pull current from the transformer from one side of the differential signal to the other to generate the pulse-amplitude-modulated (PAM) signal at the load. Since the current source is high impedance, the driver's output impedance is formed by the 100 W termination resistor, which are in parallel to the 100 W load.

**Figure 2 • Current-Mode Line Driver**

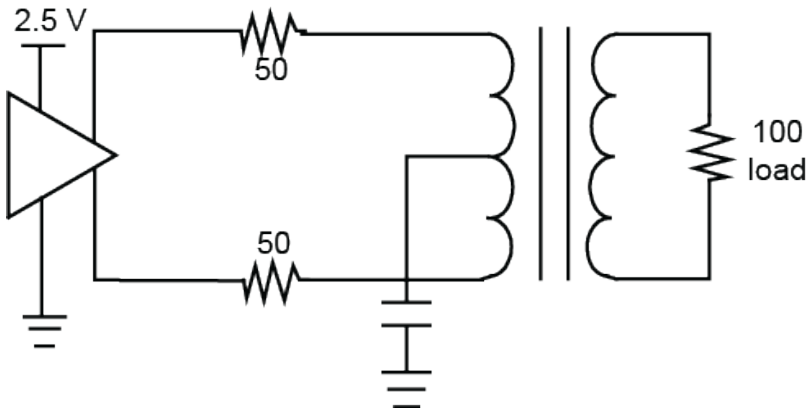



The current-mode line driver requires 40 mA (2 x 1 V/50 W=40 mA) because the impedance seen by the source is the termination impedance in parallel with the impedance of the load (100 W || 100 W = 50 W). Because the current is pulled to ground only, twice as much current is required to create the positive and negative voltages across the transformer. To generate the +1 V symbol, the 40 mA current is steered all the way to one side of the transformer and is then steered all the way to the other side in order to generate the –1 V symbol. The current is split evenly between both sides for the 0 V symbol. For current mode PHYs that use 2.5 V as their center tap voltage, the average power consumption per sub-channel is: P(avg) = 2.5 V x 40 mA = 100 mW. This translates to 400 mW per PHY for a four-channel, current-mode line driver.

### 2.2.1.2 What is a Voltage-Mode Line Driver?

The voltage-mode line driver can utilize the same board voltage as a current-mode line driver and drive the PAM signals to the required voltages at the load using less current. Because the termination and load impedances in this case are in series, the peak current drawn from the voltage-mode line driver is now I(pk) = 2 V/200 W = 10 mA.

**Figure 3 • Voltage-Mode Line Driver**



The current can also be averaged in a voltage-mode line driver, assuming the five symbols are equally weighted: I(avg) = avg(10 mA, 5 mA, 0 mA, -5 mA, -10 mA) = 6 mA. Therefore, the theoretical average power consumption of the voltage-mode line driver is: P(avg) = 2.5 V x 6 mA= 15 mW per sub-channel. This translates to 60 mW per PHY for a four-channel voltage-mode line driver, or greater than 6x power savings compared to a current-mode line driver.
It is also important to consider that because a voltage-mode line driver is a true differential output, it can generate a more balanced differential signal than a current-mode line driver, and a balanced waveform leads to better EMI prevention.

#### 2.2.1.3 Voltage-Mode Line Driver Advantages

##### 2.2.1.3.1 Lowest Power

The large difference in power between current-mode and voltage-mode line drivers is due the architecture's method of viewing the total impedance (200 W for a voltage-mode line driver versus 50 W with a current-mode line driver). The lower the impedance seen by the source, the higher the amount of power needed. Thus, even further reductions of the voltage source of the center tap of a current-mode line driver (such as 1.8 V) will still not be sufficient enough to overcome this disparity between the architectures. Because the line driver on a Gigabit Ethernet PHY is the dominant source of power, this is why voltage-mode architecture has a big advantage in powering savings over a common-mode architecture.

##### 2.2.1.3.2 Balanced Architecture Leads to Lower EMI Emission

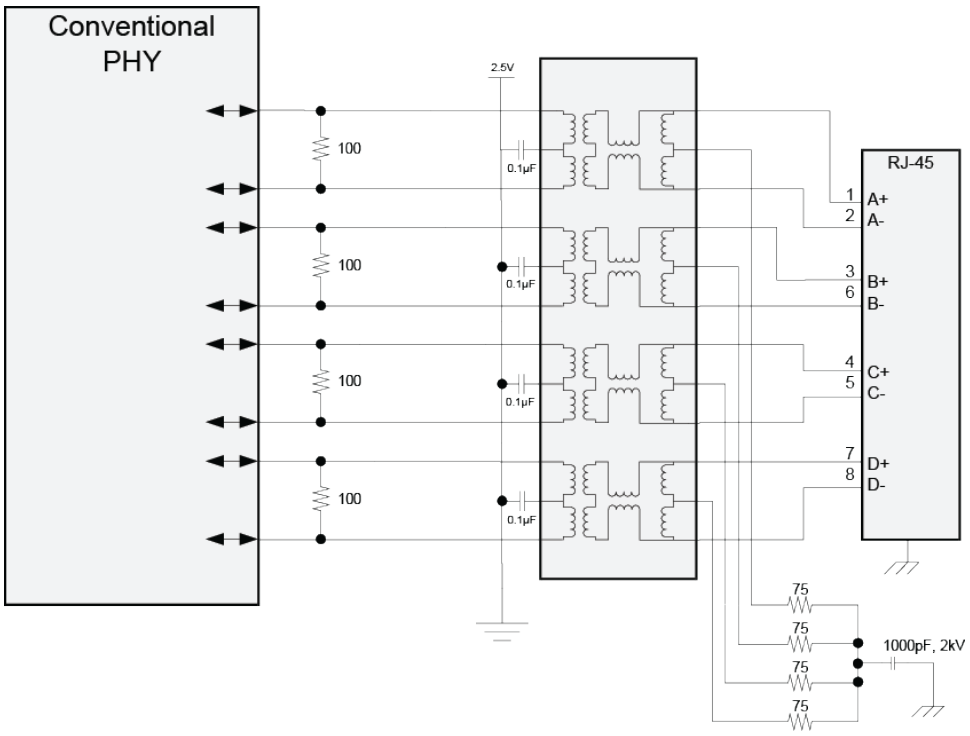
The IEEE 802.3 standard requires Ethernet PHYs to meet FCC Class A emissions, and, in applications such as PCs, it must be able to meet FCC Class B. Any imbalance in a differential waveform by a PHY could create common-mode voltages, which a transformer must then be able to rectify or else this can be seen as radiated emissions out on the cable. The better a PHY can prevent imbalances of its differential output, the less common mode is generated. Because of the difference in the way each of the architectures generate its output waveform, a voltage-mode line driver— that derives its signal from a differential output driver— inherently creates a more well-balanced waveform. This then allows for lower-cost transformers to be used in Gigabit Ethernet system designs.

##### 2.2.1.3.3 Superior ESD Protection

Because the PHY sits on edge of the system design and connects to unshielded cabling, it must be able to tolerate static discharge. The more series impedance is implemented, the better tolerance a device can withstand from a static discharge. Since a voltage-mode architecture sees its termination impedance in series, its architecture has better ESD protection by design.

### 2.2.2 Integrated Termination Resistors

In order to help simplify board designs, the traditional line driver termination resistors were integrated in the Microsemi SimpliPHY architecture in 2002. This was a first for the industry in which these resistors were a mainstay of current-mode PHY architectures dating to the time when Ethernet PHYs only offered 10BASE-T. The following illustration shows the placement of external resistors on a conventional PHY.

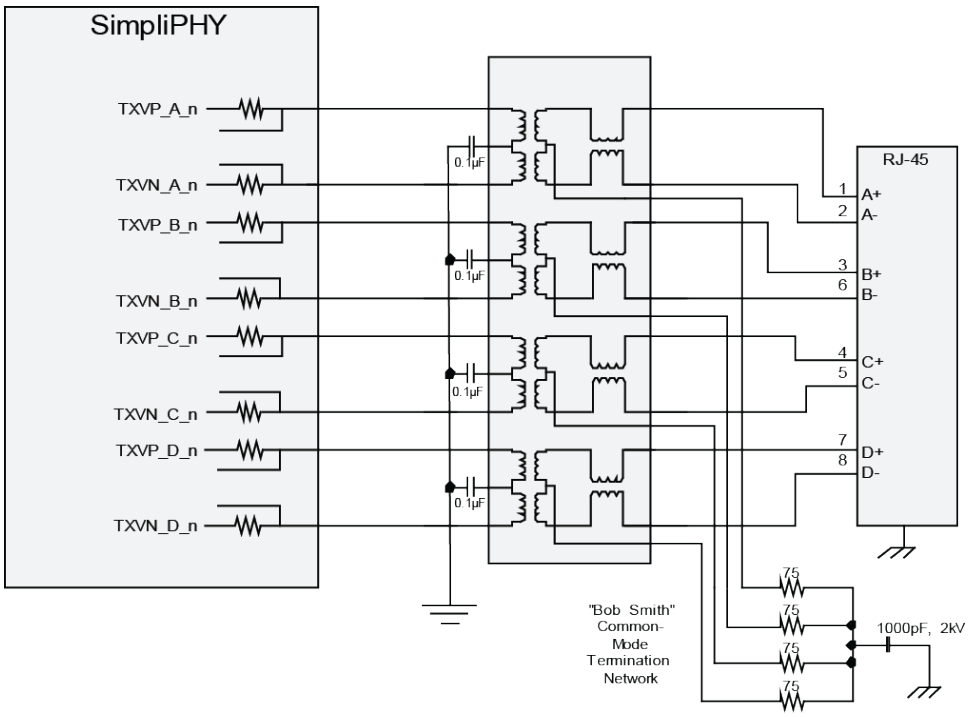



Because of the architecture of the voltage-mode line driver, integrating these resistors was a relatively simple design implementation. The integration of these resistors has several benefits:

- Easier schematic and layout design
- Eight fewer resistors per port
- Less opportunity for EMI emissions
- Savings of up to 0.25 square inches of PCB footprint

The following illustration shows a SimpliPHY device with integrated line driver resistors.

**Figure 4 • SimpliPHY with Integrated Line Driver Resistors**




The savings of PCB area on a 48-port system, for example, can add up to twelve square inches per box. The fact that this SimpliPHY feature has been so well received by the industry has forced other vendors to update their architectures to now offer a similar feature on their devices. This shows that a leading innovation such as this can help drive changes in the industry.

### 2.2.3 Analog Testability

The Microsemi SimpliPHY PHYs also include advanced analog BIST circuitry on-chip that allows extensive testing of the ATE without the need for expensive external production test equipment. This drastically reduces ATE test time and cost by eliminating expensive analog instrumentation and increasing analog test coverage, which ensures highest quality and lowest DPM (defects per million) rates, an overall benefit for Microsemi customers.

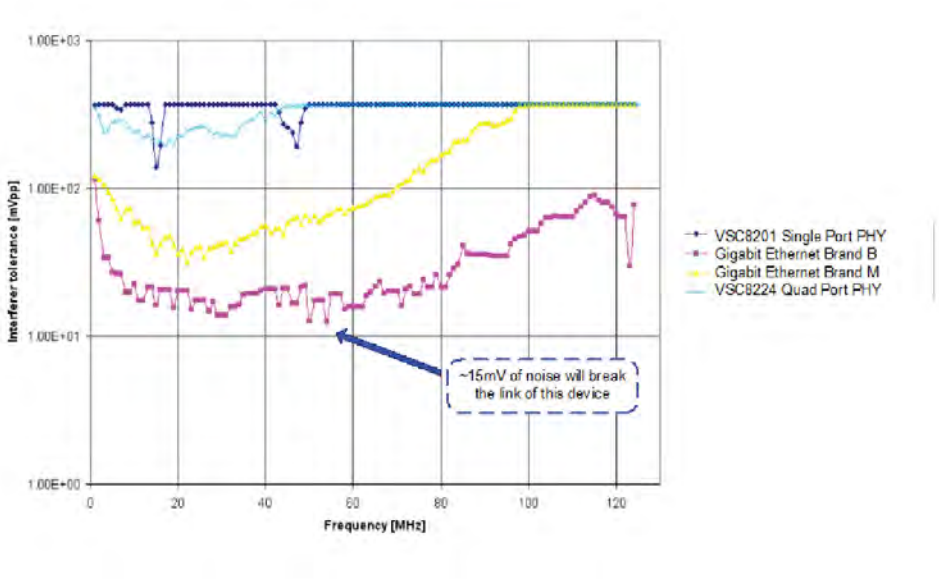
## 2.3 Digital Signal Processor (DSP)

In order to provide 1 Gbps over a copper Category 5E unshielded twisted pair cable, a Gigabit Ethernet Copper PHY must provide for a DSP equivalent of more than 250 million operations per second of digital signal processing. This level of complex processing is another reason why standard Gigabit Ethernet Copper PHYs consume a large portion of power for a multi-port Gigabit Ethernet system.

### 2.3.1 Unique Features of the Microsemi SimpliPHY DSP

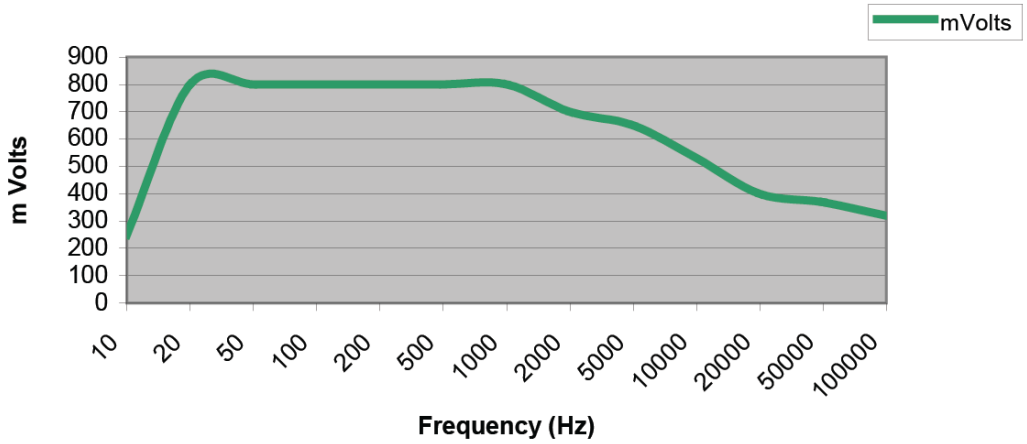
The DSP architecture utilizes a fully adaptive feed-forward equalizer (FFE). The purpose of the FFE is to compensate for frequency-dependent attenuation and dispersion (or inter-symbol interference). The filter coefficients adapt to minimize slicer errors. Together with the FFE and other proprietary circuitry, the DSP is tolerant to both cable noise and normal board power supply noise.
The following illustration shows a comparison of narrow band cable noise tolerance.

**Figure 5 • Narrow Band Tolerance**




The following illustration shows a SimpliPHY device's board power supply noise tolerance.

**Figure 6 • SimpliPHY Power Supply Noise Rejection**




## 2.3.2 Benefits of the SimpliPHY DSP

### 2.3.2.1 Correction of Cable Issues

In addition to superior noise tolerance, the DSP can correct against cable faults such as pair and polarity swaps, and has a two-pair cable downshift feature in order to interoperate with older installed cabling. It also supports Auto MDI/MDI-X in forced 10/100 speeds.

#### 2.3.2.2 VeriPHY Test Suite

The DSP also allows for the monitoring and status of cable issues with the VeriPHY test suite. VeriPHY can detect improper terminations, cable mis-wirings, and is able to pinpoint faults within the twisted pair cabling. Testing can be performed during normal 1000BASE-T data operation without having to bring down the link.

## 2.4 Innovative PHY Features

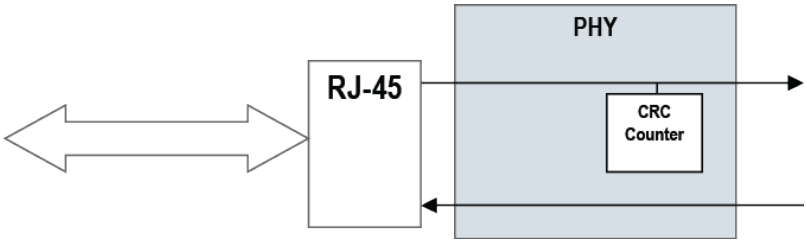
### 2.4.1 Loopbacks

In order to isolate common issues during the design phase, the SimpliPHY devices come equipped with several loopbacks to isolate the data stream for debug purposes. Each PHY contains a near-end loopback, a far-end loopback, and a connector loopback. The near-end loopback loops data from the MAC into the PHY and back to the MAC. The far-end loopback takes data coming in from the cable and returns it out on the line. The connector loopback is very similar to the near-end loopback, except an external connector is placed on the RJ-45 and the data from the MAC travels all the way to this loopback plug and back.

### 2.4.2 CRC Counters

The SimpliPHY device has the ability to count both CRC good and errored packets. This can be a useful feature for isolating issues during both design prototyping and production testing. The following illustration shows a CRC Counter.

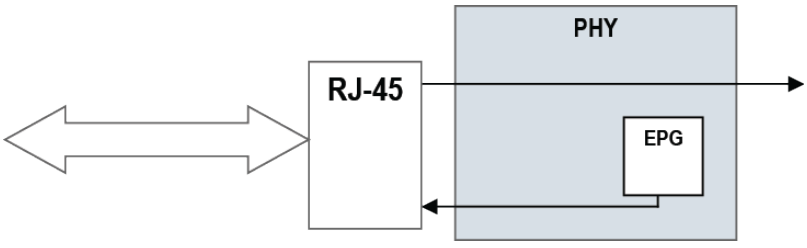
**Figure 7 • CRC Counter**




### 2.4.3 Ethernet Packet Generators

The PHY has the ability to generate IEEE compliant test packets, which aids in test development. The Ethernet packet generator (EPG) is shown in the following illustration.

**Figure 8 • Ethernet Packet Generator**




## 2.5 Conclusion

The SimpliPHY Architecture contains the Gigabit Ethernet industry's most innovative features. Not only has this design consistently allowed Microsemi to be a leader in the lowest-power devices among 1000BASE-T PHYs, but it also provides for superior performance as well as overall system BOM cost savings.

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