OS81212/4/6

Intelligent Network Interface Controller for 50 Mbit/s Automotive Networks Product Brief

Features

- Complete 50 Mbit/s synchronous network interface
- Embedded network management functions
  - Network protection mode
  - Hardware & application watchdog timer
  - Intelligent muting
  - Diagnostics
  - Fallback Operation
- IEEE MAC addressing and Ethernet channel
- Media Local Bus (MediaLB®) Port (OS81212)
  - Eases inter-chip communication and streaming
  - MediaLB 3-pin interface at speeds up to 1024xFs
- I²C™ Control Port inter-chip message exchange
- Streaming Port supports synchronous, fixed latency data exchange for a variety of serial audio formats including time-division multiplex (TDM) and pulse density modulation (PDM)
- SPI Port supports asynchronous and control packets (OS81212/4)
- General Purpose I/O (GPIO) Port
- Remote control and configuration for operation without a local External Host Controller.
  - I²C (master) message tunneling
  - GPIO port control
- Operating voltages 3.3 V/1.8 V
- Available in 56-pin (OS81212) and 48-pin (OS81214/6) QFN packages with exposed pad
- -40 to +125 °C junction temperature

Conformity

This document applies to hardware revision B2B

Applications

- Automotive infotainment network nodes including instrument cluster, amplifier, headrest speakers, microphones, acoustic processing units, and rear seat entertainment.

General Description

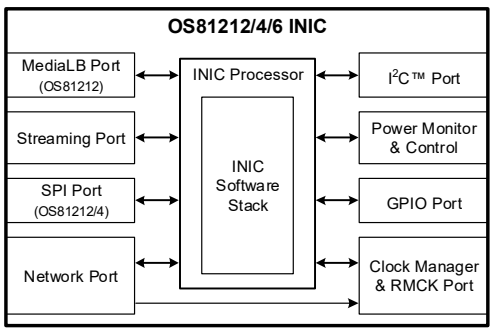
The OS81212/4/6 is a highly integrated *Intelligent Network Interface Controller* (INIC) for 50 Mbit/s INICnet-based automotive networks with a transformer-less balanced media physical layer (bPHY) optimized for unshielded twisted pair (UTP) copper wire.

The INIC provides encapsulation of all low-level functions necessary to develop a network-compliant device, significantly simplifying network implementation in a node. Integration of the *INIC Software Stack* into the INIC provides network-compliant real-time behavior. The *INIC Software Stack* significantly relieves the External Host Controller (EHC) from real-time processing tasks. Supervision of the application is also provided, including a protection mode that is entered when an application is not present (i.e. start-up) or the EHC malfunctions. This protection mode prevents application malfunctions from influencing the integrity of the network and the system.

When an EHC is engaged, a message-based interface, as opposed to a register-based interface, is available for communication with INIC. A unified and centralized network management software stack (UNICENS) is available for the EHC to build a complete, lean, system solution.

The INIC conforms to the ISO 21806 standard developed by the International Organization for Standardization (ISO®).

FIGURE: OS81212/4/6 BLOCK DIAGRAM



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1.0 PINOUT

FIGURE 1-1: OS81212 PIN DIAGRAM

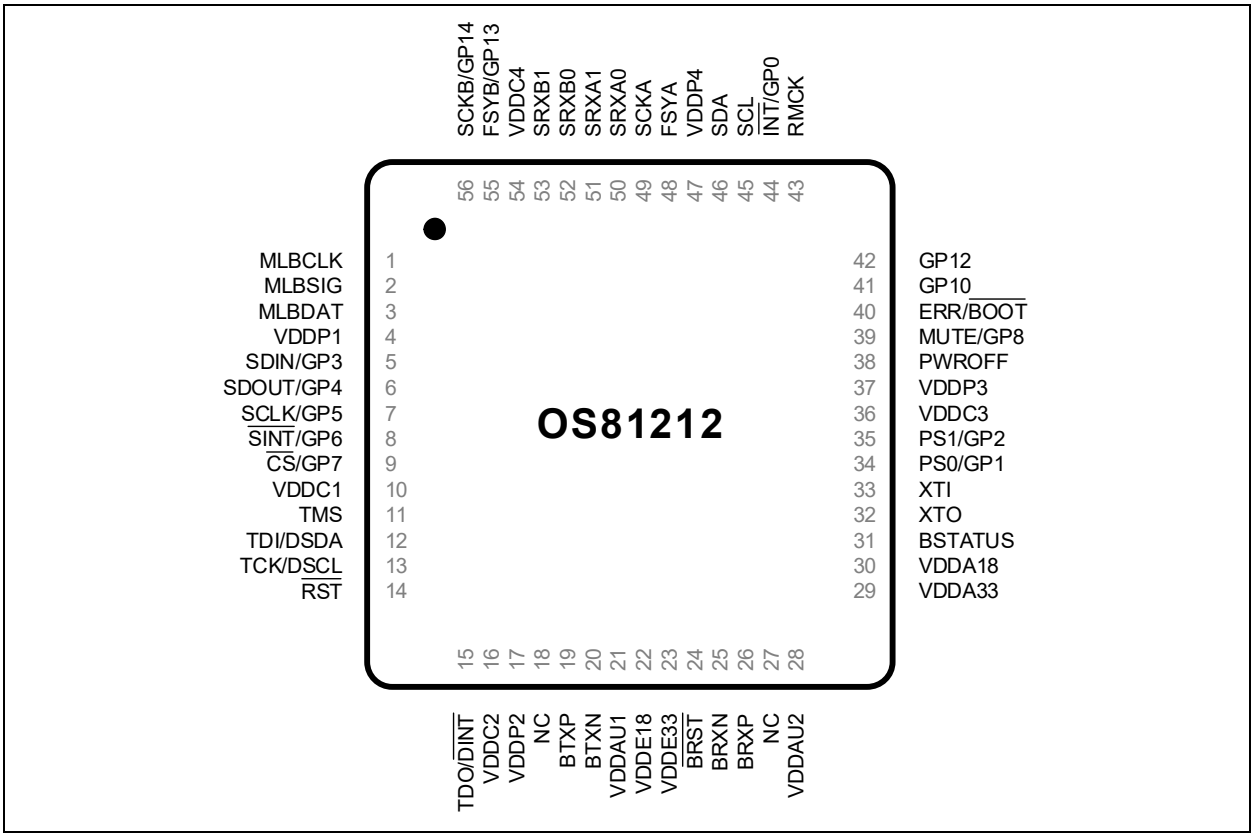


FIGURE 1-2: OS81214 PIN DIAGRAM

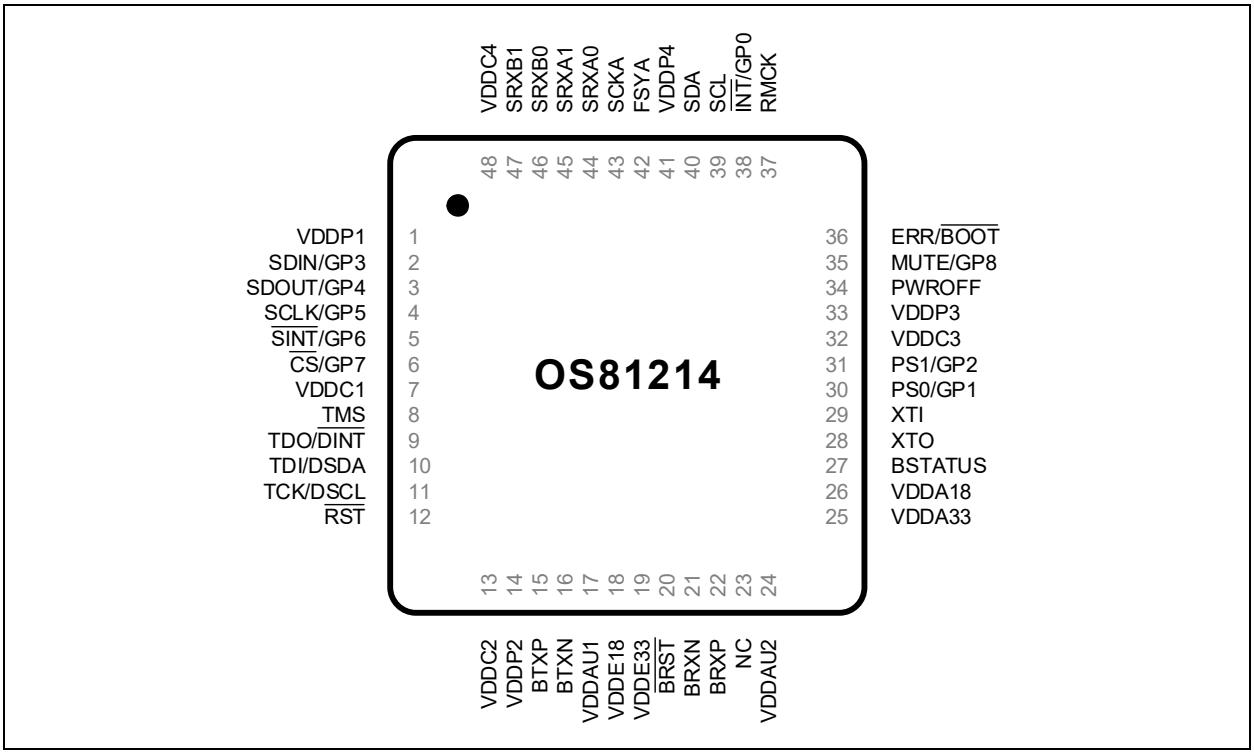


FIGURE 1-3: OS81216 PIN DIAGRAM

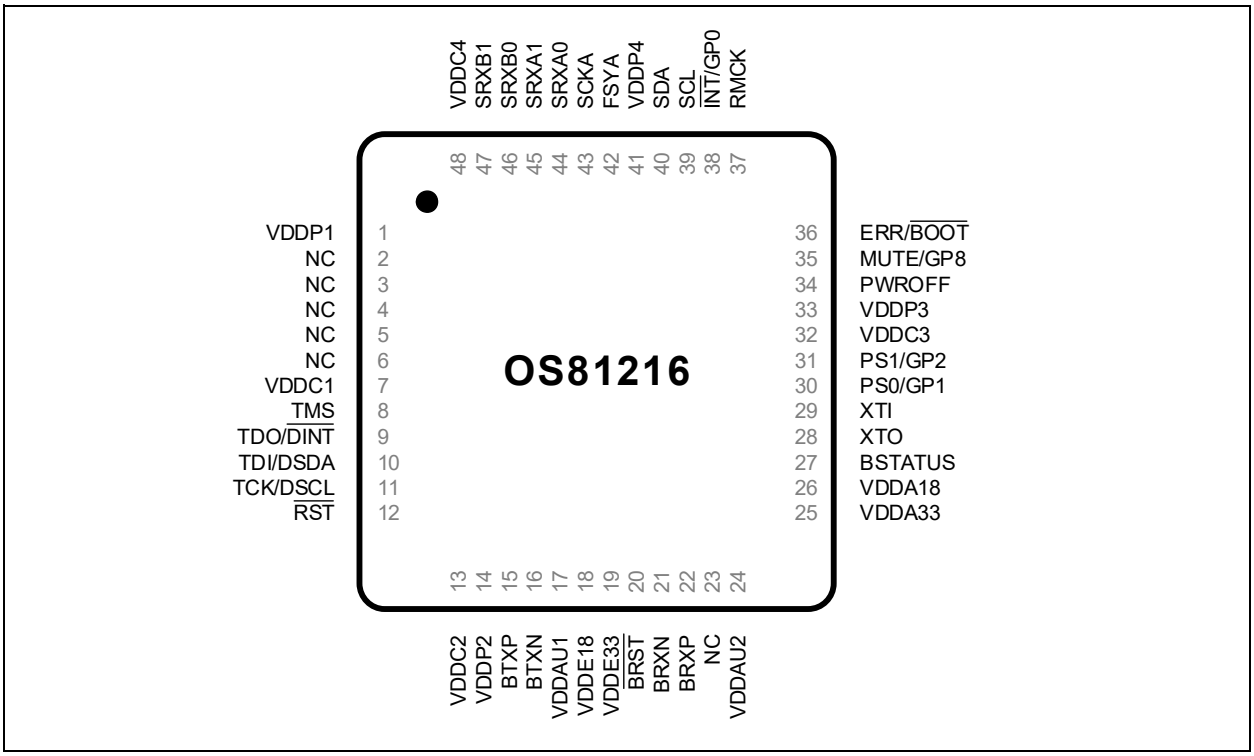


TABLE 1-1: OS81212/4/6 PIN ALLOCATION TABLE

OS81212 Pin	OS81214 Pin	OS81216 Pin	Name	Type	HW Port	Description
1	-	-	MLBCLK [2]	D_{OUT}	MediaLB	Singled-ended Clock line for MediaLB 3-pin Interface
2	-	-	MLBSIG [2]	$D_{I/O}$	MediaLB	Singled-ended Signal line for MediaLB 3-pin Interface
3	-	-	MLBDAT [2]	$D_{I/O}$	MediaLB	Singled-ended Data line for MediaLB 3-pin Interface
4	1	1	VDDP1			3.3 V periphery power supply (digital)
5	2	-	SDIN	D_{IN}	SPI	Data In (MOSI - Master Out, Slave In)
			GP3	$D_{I/O}$	GPIO	General Purpose Input/Output 3
-	-	2	NC			No Connect. This pin must be left open and floating.
6	3	-	SDOUT	D_{OUT}	SPI	Data Out (MISO - Master In, Slave Out)
			GP4	$D_{I/O}$	GPIO	General Purpose Input/Output 4
-	-	3	NC			No Connect. This pin must be left open and floating.
7	4	-	SCLK	D_{IN}	SPI	Clock
			GP5	$D_{I/O}$	GPIO	General Purpose Input/Output 5
-	-	4	NC			No Connect. This pin must be left open and floating.
8	5	-	$\overline{SINT}$	D_{OUT}	SPI	Interrupt (active low)
			GP6	$D_{I/O}$	GPIO	General Purpose Input/Output 6
-	-	5	NC			No Connect. This pin must be left open and floating.
9	6	-	$\overline{CS}$	D_{IN}	SPI	Chip Select (active low)
			GP7	$D_{I/O}$	GPIO	General Purpose Input/Output 7
-	-	6	NC			No Connect. This pin must be left open and floating.
10	7	7	VDDC1			1.8 V core power supply (digital)

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

TABLE 1-1: OS81212/4/6 PIN ALLOCATION TABLE (CONTINUED)

OS81212 Pin	OS81214 Pin	OS81216 Pin	Name	Type	HW Port	Description
11	8	8	TMS [1]	D_{IN}	JTAG	Test Mode Select
-	9	9	TDO [1]	D_{OUTZ}	JTAG	Test Data Output
			$\overline{DINT}$ [1]	D_{OUTD}		Debug Interrupt (active low)
12	10	10	TDI [1]	D_{IN}	JTAG	Test Data Input
			DSDA [1]	$D_{I/OD}$		Debug Data
13	11	11	TCK [1]	D_{IN}	JTAG	Test Clock Input
			DSCL [1]	$D_{I/OD}$		Debug Clock
14	12	12	$\overline{RST}$	D_{IN}		Hardware Reset Input (active low). (Pull-up resistor to **VDDPn** supply should be used when not driven high by an external device. A series resistor should be used in lieu of the pull-up when always driven by an external device.)
15	-	-	TDO [1]	D_{OUTZ}	JTAG	Test Data Output
			$\overline{DINT}$ [1]	D_{OUTD}		Debug Interrupt (active low)
16	13	13	VDDC2			1.8 V core power supply (digital)
17	14	14	VDDP2			3.3 V periphery power supply (digital)
18	-	-	NC			No Connect. This pin must be left open and floating.
19	15	15	BTXP	$A_{I/O}$	Network	Positive (differential) bPHY network transmitter output
20	16	16	BTXN	$A_{I/O}$	Network	Negative (differential) bPHY network transmitter output
21	17	17	VDDAU1			3.3 V continuous power supply (analog)
22	18	18	VDDE18			1.8 V bPHY power supply (analog)
23	19	19	VDDE33			3.3 V bPHY power supply (analog)
24	20	20	$\overline{BRST}$[1]	$A_{I/O}$	Network	Hardware Reset Input (active low) for the Balanced Media Physical Layer. When asserted, the transmitter output is disabled. A pull-up resistor to **VDDPn** is required.
25	21	21	BRXN	$A_{I/O}$	Network	Negative (differential) bPHY network receiver input
26	22	22	BRXP	$A_{I/O}$	Network	Positive (differential) bPHY network receiver input
27	23	23	NC			No Connect. This pin must be left open and floating.
28	24	24	VDDAU2			3.3 V continuous power supply (analog)
29	25	25	VDDA33			3.3 V power supply (analog)
30	26	26	VDDA18			1.8 V power supply (analog)
31	27	27	BSTATUS	D_{OUT}	Network	bPHY Network Activity Status Output used during wake-up: - Driven low when a valid signal is detected - Driven high to **VDDAUn** when a qualified signal is not present
32	28	28	XTO	$A_{I/O}$		Crystal Oscillator Output
33	29	29	XTI	$A_{I/O}$		Crystal Oscillator Input or External CMOS Clock Input
34	30	30	PS0	D_{IN}		External Power Management Status Bit 0
			GP1	$D_{I/O}$	GPIO	General Purpose Input/Output 1
35	31	31	PS1	D_{IN}		External Power Management Status Bit 1
			GP2	$D_{I/O}$	GPIO	General Purpose Input/Output 2

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

TABLE 1-1: OS81212/4/6 PIN ALLOCATION TABLE (CONTINUED)

OS81212 Pin	OS81214 Pin	OS81216 Pin	Name	Type	HW Port	Description
36	32	32	VDDC3			1.8 V core power supply (digital)
37	33	33	VDDP3			3.3 V periphery power supply (digital)
38	34	34	PWROFF [1]	D_{OUTD}		External Power Management Power-Down Indicator. This pin is driven low by INIC after initialization. When high, indicates that the INIC Processor is ready to be shut down. A pull-up resistor is required when used. If not used, this pin may be left unconnected.
39	35	35	MUTE [1]	D_{OUTD}		Mute Indicator Output. A pull-up resistor is required when used. If not used, this pin may be left unconnected.
			GP8	$D_{I/O}$	GPIO	General Purpose Input/Output 8
40	36	36	ERR	D_{OUT}		Error Indicator Output
			$\overline{BOOT}$ [1]	D_{IN}		Configuration Pin. This pin is attached to the configuration/debug header and used by the Microchip INICkit Tool [3] to load initial configuration data into INIC. May also be connected to the EHC to allow in-system configuration of the INIC.
41	-	-	GP10	$D_{I/O}$	GPIO	General Purpose Input/Output 10
42	-	-	GP12	$D_{I/O}$	GPIO	General Purpose Input/Output 12
43	37	37	RMCK	D_{OUT}	RMCK	Recovered Master Clock Output
44	38	38	$\overline{INT}$ [1]	D_{OUTD}	I^2C	Interrupt (active low). Indicates a service request from the EHC when the Control Port is operating as an I^2C slave.
			GP0	$D_{I/O}$	GPIO	General Purpose Input/Output 0
45	39	39	SCL [1]	$D_{I/OD}$	I^2C	Clock
46	40	40	SDA [1]	$D_{I/OD}$	I^2C	Data
47	41	41	VDDP4			3.3 V periphery power supply (digital)
48	42	42	FSYA	$D_{I/O}$	Streaming	Frame Sync for Streaming Port A
49	43	43	SCKA	$D_{I/O}$	Streaming	Bit Clock for Streaming Port A
50	44	44	SRXA0	$D_{I/O}$	Streaming	Data I/O Signal 0 for Streaming Port A
51	45	45	SRXA1	$D_{I/O}$	Streaming	Data I/O Signal 1 for Streaming Port A
52	46	46	SRXB0	$D_{I/O}$	Streaming	Data I/O Signal 0 for Streaming Port B
53	47	47	SRXB1	$D_{I/O}$	Streaming	Data I/O Signal 1 for Streaming Port B
54	48	48	VDDC4			1.8 V core power supply (digital)
55	-	-	FSYB	$D_{I/O}$	Streaming	Frame Sync for Streaming Port B
	-	-	GP13	$D_{I/O}$	GPIO	General Purpose Input/Output 13
56	-	-	SCKB	$D_{I/O}$	Streaming	Bit Clock for Streaming Port B
	-	-	GP14	$D_{I/O}$	GPIO	General Purpose Input/Output 14
ePAD	ePAD	ePAD	GND			The exposed paddle on the bottom side of the QFN package is the primary ground for the OS81212/4/6 and must be connected to ground on the PCB for proper operation.

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

2.0 BASIC APPLICATION INFORMATION

The OS81210 and OS81212/4/6 INICs are part of the OS8121x 50 Mbit/s INICnet product family that support point-to-point, simplex daisy chain, and ring topologies through an integrated balanced media physical layer (bPHY). The integrated *INIC Software Stack* can independently run the network and manage the low-level protocols such as startup, shutdown, error reporting, or Plug-and-Play node positioning. Alternatively, INIC can operate in conjunction with an External Host Controller (EHC) managing the mid- and high-level functions. Additionally the OS81210 provides power management capabilities and industry standard application interfaces such a USB 2.0, MediaLB 3-Pin, Streaming Port, I^2C Port, SPI port, and GPIOs.

The OS81210 is optimized for high performance head unit applications with USB 2.0 or HSIC high-speed communication.

The OS81212 is targeted for audio / video streaming data applications with the dual Streaming Ports and MediaLB interface. It can operate with an EHC or it can exist remotely on the network.

The OS81214 is targeted for audio data applications using the Streaming Port or packets over the SPI Port. It can operate with an EHC or it can exist remotely on the network.

The OS81216 INIC is targeted for remotely configured microphone applications (without a local EHC).

FIGURE 2-1: OS8121x PRODUCT FAMILY OVERVIEW

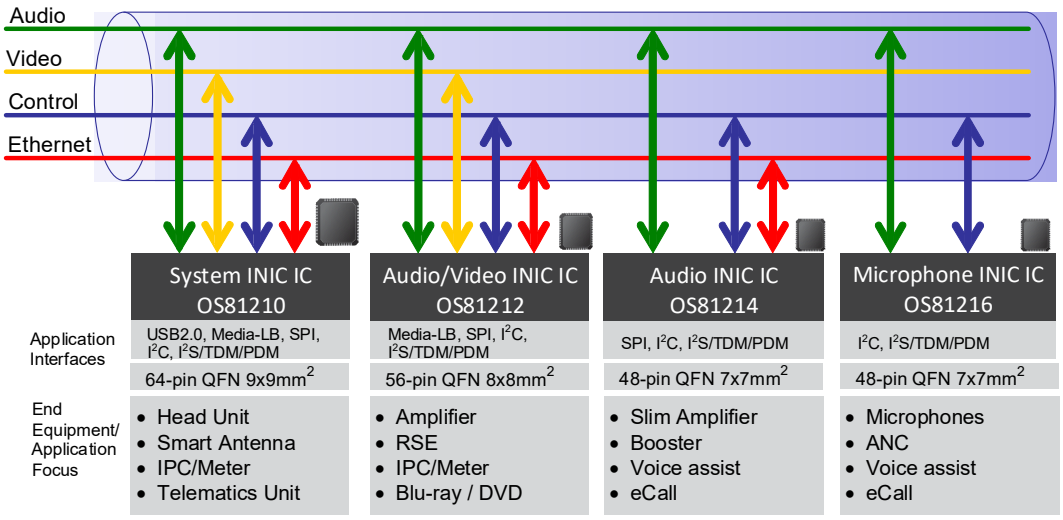
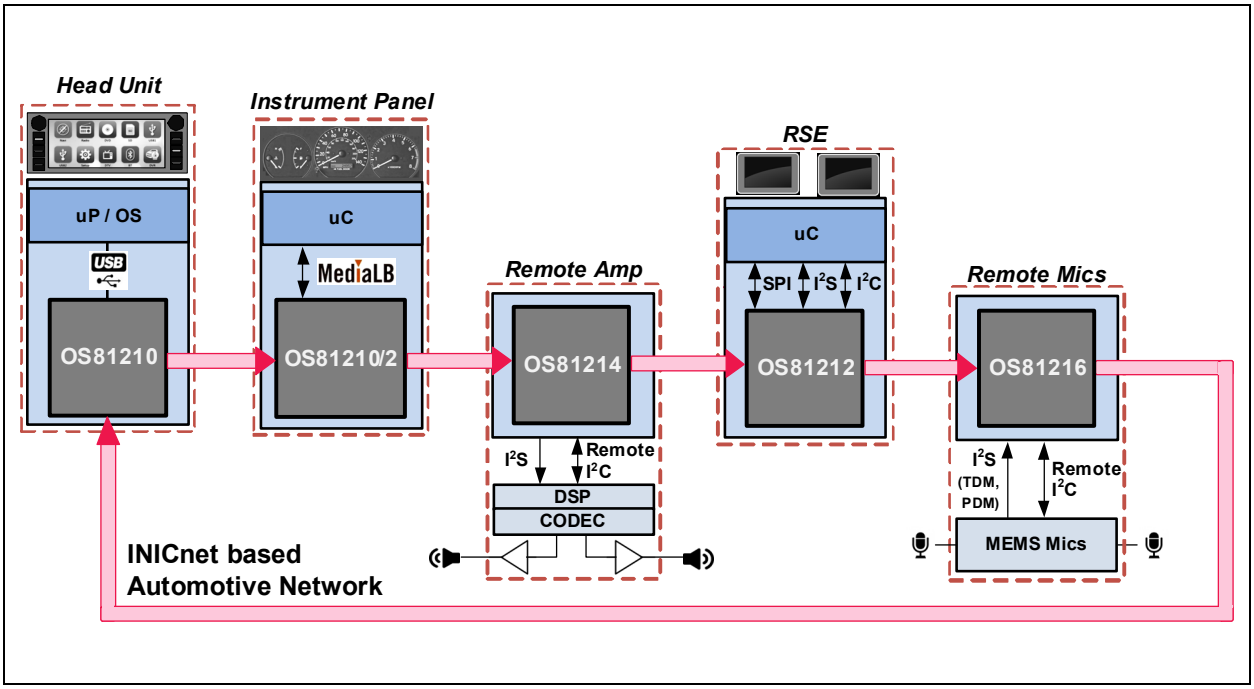


Figure 2-2 depicts an example 50 Mbit/s INICnet application. Using a combination of OS81210 and OS81212/4/6 INICs, a system supporting audio, video, and packet data applications can be easily configured. The Head Unit INIC can communicate with an operating system (such as a GNU/Linux, QNX, Android Auto, etc.) to manage the network and control the remote nodes. The asynchronous channel on the INIC can be used for high-speed routing of application packet data such as graphics images, system information, or software downloads. The EHC can access both synchronous and packet data through the OS81210 USB interface. An Instrument Panel can be implemented with control and Ethernet packets sent over the OS81210/2 MediaLB Port. Without a local EHC, the microphones are configured remotely over I^2C. Only a single INIC streaming pin is used to source a mono PDM bit stream from a MEMS microphone to the network. As shown in the Remote Amp, the amplifier is remotely controlled and configured. Synchronous audio data is routed over the network and is sourced/sinked through I^2S to CODECs or DSPs. The Rear Seat Entertainment (RSE) can route synchronous streams or asynchronous data such a IP packets over the network Ethernet Channel.

FIGURE 2-2: BASIC APPLICATION DIAGRAM



3.0 PACKAGING INFORMATION

3.1 Package Marking

FIGURE 3-1: OS81212 TOP MARKING

The package designators are:
- xx - Device Identifier
  - **OS81212AF** - Solderable Flank QFN
- rrr - Product Revision Code
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- nnn - Tracking Number
- cc - Country of Origin Abbreviation (optional - up to 2 characters)
- e3 - Pb Free Symbol

FIGURE 3-2: OS81214 TOP MARKING

The package designators are:
- xx - Device Identifier
  - **OS81214AF** - Solderable Flank QFN
- rrr - Product Revision Code
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- nnn - Tracking Number
- cc - Country of Origin Abbreviation (optional - up to 2 characters)
- e3 - Pb Free Symbol

FIGURE 3-3: OS81216 TOP MARKING

The package designators are:

- xx - Device Identifier
  - **OS81216AF** - Solderable Flank QFN
- rrr - Product Revision Code
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- nnn - Tracking Number
- cc - Country of Origin Abbreviation (optional - up to 2 characters)
- e3 - Pb Free Symbol

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	[X]	-	rrr	-	vvvvvv	[ss]	-	[xxx]
Device	Grade	Package Type	Tape and Reel Flag		Product Revision Code		Firmware Revision Code	Firmware Service Release		Special Feature Code

Device	OS81212	=	50 Mbit/s Automotive Intelligent Network Interface Controller with MediaLB
	OS81214	=	50 Mbit/s Automotive Intelligent Network Interface Controller (no MediaLB)
	OS81216	=	50 Mbit/s Automotive Intelligent Network Interface Controller (no MediaLB, SPI)
Grade	A	=	All Features
Package Type	F	=	QFN with solderable terminals
Tape and Reel Flag (optional)	Blank	=	Standard Packaging (Tube/Tray)
	R	=	Tape and Reel
Product Revision Code	rrr	=	3 character code specifying product revision
Firmware Revision Code	vvvvvv	=	6 character code specifying firmware revision
Firmware Service Release (optional)	ss	=	2 character code specifying service release
Special Feature Code (optional)	xxx	=	3 character code for special requirements

Examples:

a) OS81212AF-rrr-vvvvvv-xxx
56-pin solderable terminal QFN package

b) OS81212AFR-rrr-vvvvvv-xxx
56-pin solderable terminal QFN package, Tape and Reel

c) OS81214AF-rrr-vvvvvv-xxx
48-pin solderable terminal QFN package

d) OS81214AFR-rrr-vvvvvv-xxx
48-pin solderable terminal QFN package, Tape and Reel

e) OS81216AF-rrr-vvvvvv-xxx
48-pin solderable terminal QFN package

f) OS81216AFR-rrr-vvvvvv-xxx
48-pin solderable terminal QFN package, Tape and Reel

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