

Component Placement Checklist for LAN89730

Information Particular for the 56-pin QFN Package

LAN89730 QFN Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXP, pin 3) as close to the LAN89730 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXN, pin 2) as close to the LAN89730 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
3. Place the 49.9 Ω RX termination pull-up (RXP, pin 6) as close to the LAN89730 as possible.
4. Place the 49.9 Ω RX termination pull-up (RXN, pin 5) as close to the LAN89730 as possible.

LAN89730 QFN Magnetics:

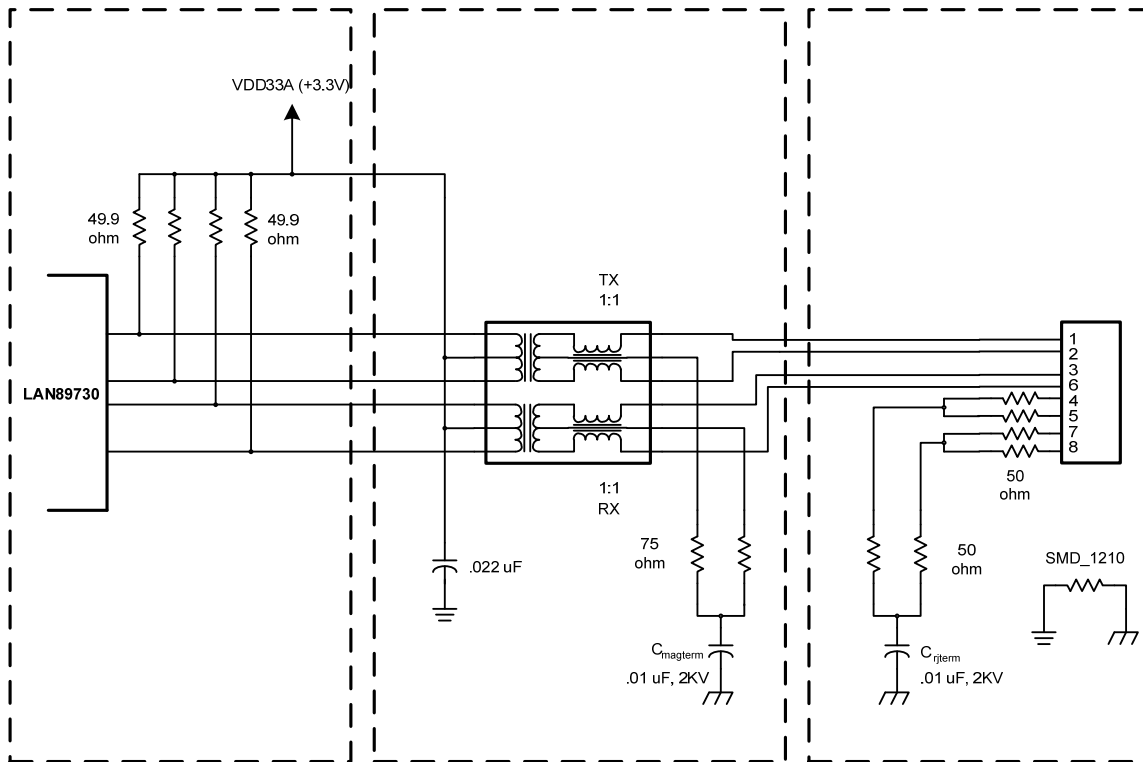
1. Place the 0.022 μ F TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.
2. Place the 75 Ω cable side center tap termination resistors and the 1000 pF, 2KV capacitor (C_{magterm}) cap as close to the magnetics as possible.



RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN89730 QFN as close together as possible.
2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN89730 QFN.
3. Select and place the magnetics as to set up the best routing scheme from the LAN89730 QFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.
4. Place the Unused Wire Pair termination resistors and the 1000 μ F, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.
5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.





Locate the four 49.9 ohm differential terminations close to the LAN89730

Locate these two resistors and two caps close to the magnetics

Locate all these components close to the RJ45 connector

Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TXP & TXN signals placed close to the LAN89730 for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

+3.3V Power Supply Connections:

1. Place the (5) VDD33IO decoupling capacitors for the LAN89730 QFN as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.
2. Place the (3) VDD33A decoupling capacitors for the LAN89730 QFN as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

VDD12CORE:

1. VDD12CORE (pin 50) requires a 0.01 μ F bypass capacitor and a low ESR 1.0 μ F bulk capacitor placed as close as possible to pin 50.
2. The other VDD12CORE (pin 21) only requires a 0.01 μ F bypass capacitor placed as close as possible to pin 21.
3. Place the VDD12PLL decoupling capacitor for the LAN89730 QFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.
4. Place the VDD12USBPLL decoupling capacitor for the LAN89730 QFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

Ground Connections:

1. There are no component placement issues associated with the LAN89730 QFN ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible. The exposed die paddle (pin 57) ground on the bottom of the LAN89730 will be connected immediately to this solid digital ground plane.



Crystal Connections:

1. Place the 25 MHz crystal and the associated 15 – 33 μ F capacitors as close together as possible and as close to the LAN89730 QFN (XI, pin 18 & XO, pin 19) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)
2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.

EEPROM Interface:

1. There are no component placement issues associated with the EEPROM Interface.

EXRES Resistor:

1. Place the EXRES resistor as close to pin 7 of the LAN89730 QFN as possible.

USBRBIAS Resistor:

1. Place the USBRBIAS resistor as close to pin 16 of the LAN89730 QFN as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN89730 QFN.

MII Interface:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.



HSIC Interface:

1. The HSIC interface is only recommended for intra-board interconnect. The connection should be point-to-point. Connectors and cables are not recommended.
2. The LAN89730 and the USB Host must be placed in such a manner that the resultant overall routing of the HSIC_DATA (pin 10) & the HSIC_STROBE (pin 11) lines are a minimum of 2.0 cm and a maximum of 10.0 cm.

Configuration Straps:

1. There are no component placement issues associated with the Configuration Straps of the LAN89730 QFN.

Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.
2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.

