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DOCUMENT DESCRIPTION
Routing Checklist for the LAN9221I, 56-pin QFN Package

 	SMSC 80 Arkay Drive Hauppauge, New York 11788	
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Routing Checklist for LAN9221I

Information Particular for the 56-pin QFN Package

LAN9221I QFN Phy Interface:

1. The traces connecting the transmit outputs (TPO+, pin 45) & (TPO-, pin 44) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
2. The traces connecting the receive inputs (TPI+, pin 48) & (TPI-, pin 47) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. The VDD33A power supply should be routed as a mini-plane and can be routed on an internal power plane layer.
5. The union of the 10.0Ω resistor supplying VDD33A to the Transmit & Receive Channel center taps of the magnetics and the $0.022\ \mu\text{F}$ capacitor, should be routed as a mini-plane.

LAN9221I QFN Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.
2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

+3.3V Power Supply Connections:

1. Route the (1) VDD33REG pin of the LAN9221I QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. In addition, route the (1) VDD33REG decoupling capacitor for the LAN9221I QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
3. Route the (3) VDD33A pins of the LAN9221I QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
4. In addition, route the (3) VDD33A decoupling capacitors for the LAN9221I QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. Route the (4) VDDVARIO pins of the LAN9221I QFN directly into a solid, +1.8V to +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. In addition, route the (4) VDDVARIO decoupling capacitors for the LAN9221I QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.8V/+3.3V & digital ground plane) for each cap.

VDD18CORE:

1. The VDD18CORE pin 37 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap associated with it.
2. The VDD18CORE pin 2 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it.
3. The two VDD18CORE pins 2 & 37 must then be connected together with a short, heavy, wide trace (or a mini-plane) on the PCB. Be sure to use multiple vias as necessary.

VDD18A:

1. The VDD18A pin 53 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap associated with it.
2. VDD18A (pin 53) must then be connected to VDD18CORE with a short, heavy, wide trace (or a mini-plane) on the PCB. Be sure to use multiple vias as necessary.
3. **Do Not**, under any circumstances, use VDD18CORE to supply other circuits or devices. The internal voltage regulator is designed to supply internal logic of the LAN9221I only.

Ground Connections:

1. The single digital ground pin (pin 57, EDP) on the LAN9221I QFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 16 power vias in a 4x4 grid.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.
2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

EEPROM Interface:

1. There are no critical routing instructions for the EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

EXRES Resistor:

1. The EXRES resistor (pin 50) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-ups/Pull-down connections.

CPU Interface

1. Good, general design practices should be adhered to ensure proper operation.
2. Follow recommended processor design guidelines to ensure proper operation.
3. Follow recommended interpair spacing guidelines within data bus byte lanes, address bus and control group signals.
4. Follow recommended intrapair spacing guidelines between data bus byte lanes, address bus and control group signals.
5. As with any high-speed design interface, it is the design engineer's responsibility to review the PCB routing for specification adherence. The design engineer should review all timing relationships as put forth in the selected processor's data sheet and the LAN9221I QFN data sheet and make certain that any PCB routing does not add significant timing delays. These timing relationships can be found in the Host Bus System Timing section of the LAN9221I QFN data sheet.

Internal Pull-up / Pull-down Augmentation:

1. There are no critical routing instructions for with the extra external pull-ups or pull-downs required by the LAN9221I when operating at lower than +3.0V on the VDDVARIO.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN9221 QFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.
2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.
3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.
4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.
5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.