# PIC24FJ128GA306 to PIC24FJ128GL306 Migration and Performance Enhancement Guide

## INTRODUCTION

The PIC24FJ128GL306 device family includes many new features and a few minor changes from the PIC24FJ128GA306 device. In order to offer easy migration with minimal effort, most of the features in PIC24FJ128GL306 are backward-compatible with the features in PIC24FJ128GA306, including the enhanced features.

The code developed for the PIC24FJ128GA306 devices can be ported to the PIC24FJ128GL306 family devices after making the appropriate minimal changes, only if applicable, as described in this document. The PIC24FJ128GL306 family devices feature many improvements and new capabilities over the PIC24FJ128GA306 devices while maintaining backward compatibility, such as:

- ECC Flash Memory with Fault Injection
- ICSP™ Write Inhibit Feature
- Enhanced Security Features with CodeGuard™ Security
- Improved FRC Accuracy by Using Active Clock Tuning
- New Integrated Segmented LCD Module with Core-Independent Animation Feature and Support for Increased Number of LCD Segments
- New Capture/Compare/PWM/Timer (MCCP) Asynchronous Modules which are Capable of Operating at a Higher Clock than the CPU Clock
- Improved Serial Peripheral Interface (SPI) Module with $I^2S$ Interface Support and an Operating Frequency up to 16 MHz
- An Enhanced $I^2C$ Module, Supporting PMBus™ Communication and SMBus 3.0 Voltage Specification
- An Enhanced Real-Time Clock and Calendar (RTCC) Module with a Timestamp Anti-Tamper Feature
- New Deadman Timer (DMT)
- New Configurable Logic Cell (CLC) Module
- Improved 12-Bit Analog-to-Digital Converter (ADC) with Higher Conversion Rate

This migration and performance enhancement guide discusses several enhancements, changes and application migration considerations related to the PIC24FJ128GL306 family devices.

The following are a few minor migration considerations:

- Some Peripherals are Added/Moved to the Peripheral Pin Select (PPS) Mapping to Facilitate Board Design Flexibility and Easy Migration
- VBAT Mode is Supported through Emulation, which Needs to be Implemented Using Minimal External Components to Achieve the Same Functionality
- Increased Run-Time Self-Programming (RTSP) Page and Row Sizes with Changes in Methodology, and Changes in Erasing/Programming Times
- Changes to the Alternate Interrupt Vector Table (AIVT)
- Interrupt Register Changes
- I/O Port Analog/Digital Selection and Change Notification Control Register Changes
- Device Configuration Register Updates

| **Note:** | Most of these differences can be easily handled with minor code changes. |
|---|---|

The following are the new peripherals, or existing peripherals, that offer enhanced features while maintaining backward compatibility:

- Deadman Timer (DMT)
- Multiple Capture/Compare/PWM (MCCP)
- Configurable Logic Cell (CLC)
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit ($I^2C$)
- Real-Time Clock and Calendar (RTCC)
- Liquid Crystal Display (LCD)

In order to optimize the offerings, the following peripherals are defeatured:

- Input Capture (MCCP offers all the features of IC along with some enhancements):
- Output Compare (MCCP offers all the features of OC along with some enhancements)
- Digital Signal Modulator (DSM)
- Enhanced Parallel Master Port (EPMP)
- Charge Time Measurement Unit (CTMU)

Each section of this document describes one peripheral or major feature of the PIC24FJ128GL306 device family.

For more information on new or modified modules, refer to the "*PIC24FJ128GL306 Family Data Sheet*" (DS30010198).

Table 1 gives an overview on the migration impact.

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**TABLE 1: OVERVIEW ON MIGRATION IMPACT**

| Modules | PIC24FJ128GL306 | PIC24FJ128GA306 | Compatibility Impact |
|---|---|---|---|
| Flash Memory | 128 Kbytes with ECC | 128 Kbytes | No migration impact<br>(Refer to Flash Program Memory for new feature) |
| Oscillator | Enhanced | — | No migration impact<br>(Refer to Oscillator Configuration for new feature) |
| Interrupt | Enhanced | — | No migration impact<br>(Refer to Interrupt Controller for new feature) |
| **Analog Peripherals** | | | |
| ADC Channels | 17 Channels | 16 Channels | No migration impact |
| Segmented LCD | Up to 256 (32 x 8) Segments | Up to 240 (30 x 8) Segments | No migration impact |
| Enhanced LCD Animation Features | Yes | No | No migration impact<br>(Refer to Liquid Crystal Display (LCD) for new feature) |
| **Digital Peripherals** | | | |
| CLC | 4 | No | No migration impact<br>(Refer to Configurable Logic Cell (CLC) for new feature) |
| PWM/IC/OC/CCP | 5 x MCCP<br>(one with six outputs, four with two outputs) | 7 x IC, 7 x OC | MCCPs serve as ICs and OCs<br>(Refer to Capture/Compare/PWM/Timer Modules (MCCP) for new feature) |
| DMT | Yes | No | No migration impact<br>(Refer to Deadman Timer (DMT) for new feature) |
| $I^2C$ | Yes | Yes | No migration impact<br>(Refer to Inter-Integrated Circuit ($I^2C$) for new feature) |
| SPI | Yes | Yes | No migration impact<br>(Refer to Serial Peripheral Interface (SPI) for new feature) |
| RTCC | Yes | Yes | No migration impact<br>(Refer to Real-Time Clock and Calendar (RTCC) with Timestamp for new features) |
| UART | Yes | Yes | No migration impact |
| Timers | Yes | Yes | No migration impact |
| Comparator | Yes | Yes | No migration impact |
| HLVD | Yes | Yes | No migration impact |
| CRC | Yes | Yes | No migration impact |
| VBAT | Emulated | Yes | Emulated VBAT on PIC24FJ128GL306<br>(Refer to VBAT Emulation for new feature) |
| Deep Sleep | Retention Sleep | Yes | Achieve comparable low Sleep current by using Retention Sleep mode, while getting the benefit of retaining full RAM content |
| PMP | No | Yes | To optimize the offerings, PMP is defeatured on PIC24FJ128GL306 |
| CTMU | No | Yes | To optimize the offerings, CTMU is defeatured on PIC24FJ128GL306 |
| DSM | No | Yes | To optimize the offerings, DSM is defeatured on PIC24FJ128GL306 |


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## Topics Covered



# FLASH PROGRAM MEMORY

The Flash program memory module on the PIC24FJ128GL306 devices has several enhancements and new features. This section details the high-level improvements and includes the following topics:

- Error Correcting Code (ECC)
- ICSP™ Write Inhibit
- Customer OTP Memory
- Unique Device ID (UDID)
- CodeGuard™ Security
- Run-Time Self-Programming (RTSP)

## Error Correcting Code (ECC)

Error Correcting Code (ECC) is an integral part of the Flash memory controller. ECC can determine the presence of single bit errors and double-bit errors in the Flash memory. ECC cannot be disabled.

To test Fault handling, an ECC error can be generated. Both single and double-bit errors can be generated for testing. For more details, refer to **Section 6.4 "Error Correcting Code (ECC)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## ICSP™ Write Inhibit

ICSP Write Inhibit is an access restriction feature that, when activated, restricts access to all of Flash memory. Once activated, ICSP Write Inhibit permanently prevents ICSP Flash programming, read and erase operations, and cannot be deactivated. This feature is intended to prevent alteration of Flash memory contents with behavior similar to One-Time-Programmable (OTP) devices. This feature helps to protect the Flash and implement secure immutable boot function in any secure applications. For more details, refer to **Section 6.5 "Flash OTP by ICSP™ Write Inhibit"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## Customer OTP Memory

PIC24FJ128GL306 family devices provide 256 bytes of One-Time-Programmable (OTP) memory, located at addresses: 801700h through 8017FEh. This memory can be used for persistent storage of application-specific information that cannot be erased by reprogramming the device. For more details, refer to **Section 27.8 "Customer OTP Memory"** in the *"PIC24FJ128GL306 Family Data sheet"* (DS30010198).

## Unique Device ID (UDID)

All PIC24FJ128GL306 family devices are individually encoded during final manufacturing with a Unique Device ID (UDID). The UDID cannot be erased by a bulk erase command or any other user-accessible means. For more details, refer to **Section 27.2 "Unique Device Identifier (UDID)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## CodeGuard™ Security

PIC24FJ128GL306 family devices offer additional security features as compared to the PIC24FJ128GA306 devices. CodeGuard™ security provides code protection and write protection for each of the Flash memory segments.

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The size of the Boot Segment (BS) and General Segment (GS) will depend on the BSLIM[12:0] bits setting. The BSLIM[12:0] bits define the number of pages for the Boot Segment, with each page containing 1024 IW. The smallest Boot Segment size is one page. Additional security has been added to the configuration data, which are called the Configuration Segment (CS). For more information, refer to **Section 27.5 "Program Verification and Code Protection"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## Run-Time Self-Programming (RTSP)

For the PIC24FJ128GL306 family, the Flash row and erase block sizes differ from sizes for the PIC24FJ128GA306. The program memory data can be written in rows of 128 instructions (384 bytes) at a time and erased in blocks of 1024 instructions (3072 bytes) at a time. For more details, refer to **Section 6.2 "RTSP Operation"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

The Run-Time Self-Programming (RTSP) changes between the PIC24FJ128GA306 and PIC24FJ128GL306 devices are listed in Table 2.

**TABLE 2: RTSP CHANGES BETWEEN PIC24FJ128GA306 AND PIC24FJ128GL306 DEVICES**

| Parameters | PIC24FJ128GA306 | PIC24FJ128GL306 |
|---|---|---|
| Smallest Program Memory Word Program Size | One word – One instruction or three bytes | An even/odd pair of words – Two instructions or six bytes |
| NVMOP[3:0] Bits (NVMCON[3:0]) Setting | **If ERASE = 1:**<br>1111 = Memory bulk erase operation<br>1101 = Erase General Segment<br>0011 = No operation<br>0010 = Memory page erase operation<br>0001 = No operation<br>0000 = Erase a single Configuration register byte<br>**If ERASE = 0:**<br>1111 = No operation<br>1101 = No operation<br>0011 = Memory word program operation<br>0010 = No operation<br>0001 = Memory row program operation<br>0000 = Program a single Configuration register byte | 1111 = Reserved<br>1110 = Chip erase user memory (does not erase Device ID, customer OTP or executive memory)<br>. . .<br>0100 = Reserved<br>0011 = Memory page erase operation<br>0010 = Memory row program operation<br>0001 = Memory double-word program operation<br>0000 = Reserved |
| Location of Program Memory Latches for RTSP | Same addresses as the program memory locations to be programmed | Dedicated write latches, located at addresses from 0xFA0000 to 0xFA0100 in configuration memory space |
| Method of Specifying the Program Memory Row/Word or Configuration Register to be Written by RTSP Operation | The destination address of the most recent Table Write instruction defines the row or word to be written | The NVMADR/NVMADRU registers specify the location to program in Flash memory |


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## INTERRUPT CONTROLLER

For the PIC24FJ128GL306 family, the Alternative Interrupt Vector Table (AIVT) location is dynamic and depends on the device security settings. The total user code memory for the PIC24FJ128GL306 family can be split into the Boot Segment and General Segment. The size of the segments is determined by the BSLIM[12:0] Configuration bits.

The AIVT begins at the start of the last page of the Boot Segment. For more details, refer to **Section 8.1.1 "Alternate Interrupt Vector Table"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## OSCILLATOR CONFIGURATION

This section includes the following topics:

- Phase-Locked Loop (PLL) Module
- System Clock Divider
- Reference Clock Output (REFO) Module
- FRC Active Clock Tuning

### Phase-Locked Loop (PLL) Module

In addition to the 96 MHz PLL output, the PIC24FJ128GL306 family devices have additional PLL options, allowing a wider range of input frequencies. The multiplier ratios can be selected as 4x, 6x or 8x without a clock prescaler. For more information, refer to **Section 9.7 "Oscillator Modes"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

### System Clock Divider

For PIC24FJ128GA306 devices, only the FRC clock can be divided. The division factor is specified by the RCDIV[2:0] bits (CLKDIV[10:8]). For PIC24FJ128GL306 family devices, any clock source can be selected for the division. The clock source is chosen by the RCDIV[2:0] bits (CLKDIV[10:8]) and the division factor is selected in the special OSCDIV and OSCFDIV registers. For more information, refer to **Section 9.0 "Oscillator Configuration"** in the "*PIC24FJ128GL306 Family Data Sheet*" (DS30010198).

### Reference Clock Output (REFO) Module

The REFO module on the PIC24FJ128GL306 devices has several enhancements and new features. It allows a variety of clock sources and provides more flexible coefficients for the clock division. This Reference Clock Output is controlled by the REFOCONL/REFOCONH registers. Setting the ROEN bit (REFOCONL[15]) makes the clock signal available on the REFO pin. The RODIV[14:0] bits (REFOCONH[14:0]) enable the selection of different clock divider options. The ROSEL[3:0] bits (REFOCONL[3:0]) determine which clock source is used for the Reference Clock Output. For more information, refer to **Section 9.11 "Reference Clock Output"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

### FRC Active Clock Tuning

The PIC24FJ128GL306 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning using a SOSC with a crystal oscillator to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. New bits are added to the OSCTUN register to control the clock tuning feature. For more information, refer to **Section 9.6 "FRC Active Clock Tuning"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## LOW POWER

This section provides a brief summary of the new low-power features in the PIC24FJ128GL306 devices. For more detailed information, see **Section 10.0 "Power-Saving Features"** in the "*PIC24FJ128GL306 Family Data Sheet*" (DS30010198).

### Sleep Modes

PIC24FJ128GL306 devices have a new Retention Sleep mode. Behavior in Sleep is controlled by the RETEN and VREGS bits of the RCON register, providing four different Sleep modes (summarized in Table 3).

**TABLE 3: LOW-POWER SLEEP MODES**

| RETEN | VREGS | Mode | Relative Power |
|---|---|---|---|
| 0 | 0 | Sleep | A Few µA Range |
| 0 | 1 | Fast Wake-up | 100 µA Range |
| 1 | 0 | Retention Sleep | Less than 1 µA |
| 1 | 1 | Fast Retention | A Few µA Range |

For the typical and maximum Sleep current information, refer to **Section 30.0 "Electrical Characteristics"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

### Low-Power Brown-out Reset (LPBOR)

The PIC24FJ128GL306 devices have a Low-Power BOR that can be used when the main BOR is disabled. This behavior is controlled by the DNVPEN Configuration bit (FPOR[3]).

For more information, refer to the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## I/O PORTS

This section provides a brief summary of the new features in the PIC24FJ128GL306 I/O module. For more detailed information, see **Section 11.0 "I/O Ports"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

The key differences between PIC24FJ128GA306 devices and PIC24FJ128GL306 devices include:

- In PORTA, RA0 is an Additional Pin
- Interrupt-on-Change (IOC)/Input Change Notification (CN)

### Interrupt-on-Change (Input Change Notification)

PIC24FJ128GL306 devices have an Interrupt-on-Change (IOC) feature that replaces the Input Change Notification feature of the PIC24FJ128GA306 devices. On the PIC24FJ128GL306 devices, the IOC registers are organized by port. The new IOC feature also allows control over edge selection (rising, falling or both). The register changes are summarized in Table 4.

For more information, refer to **Section 11.3 "Interrupt-on-Change (IOC)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

**TABLE 4: INTERRUPT-ON-CHANGE REGISTERS**

| Functions | PIC24FJ128GA306 | PIC24FJ128GL306 |
|---|---|---|
| Pull-up | CNPUx(1) | IOCPUy(2) |
| Pull-Down | CNPDx(1) | IOCPDy(2) |
| Enable | CNENx(1) | — |
| Enable Positive Edge | — | IOCPy(2) |
| Enable Negative Edge | — | IOCNy(2) |
| Flag | — | IOCFy(2) |

**Note 1:** 'x' refers to the Change Notification register number (e.g., CNPD1).
**2:** 'y' refers to the PORT letter (e.g., IOCPUA).

## CAPTURE/COMPARE/PWM/TIMER MODULES (MCCP)

This section provides a brief summary of the new MCCP modules in the PIC24FJ128GL306 family devices, which provide the functionality of three different peripherals of earlier PIC24F devices. These modules can operate in one of three major modes:

- Output Compare/PWM (OC)
- Input Capture (IC)
- General Purpose Timer (TMR)

The module is provided in two different forms, distinguished by the number of PWM outputs that the module can generate. Multiple output modules (MCCPs) can provide up to six outputs. All other features of the modules are identical.

The PIC24FJ128GL306 devices have five MCCP modules. Table 5 shows the possible maximum number of timers, input capture and output compare peripherals available on the PIC24FJ128GA306 and PIC24FJ128GL306 family devices.

**TABLE 5: MAXIMUM NUMBER OF PERIPHERALS FOR PIC24FJ128GA306 AND PIC24FJ128GL306 FAMILIES**

| PIC24FJ128GA306 | PIC24FJ128GL306 |
|---|---|
| 7 x OC | 5 x MCCP |
| 7 x IC | 5 x MCCP |
| 5 x TMR | (5 x TMR) + (5 x MCCP) |


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## General Purpose Timer

The MCCP can be used as a 32-bit general purpose timer or two 16-bit timers. Both 16-bit timers can generate an interrupt and one timer can also provide a trigger to other peripherals.

Setting the T32 bit configures the MCCP module as a single 32-bit timer. Table 6 shows the features comparison between previous TMR modules and the new MCCP module in Timer mode.

**TABLE 6: COMPARISON BETWEEN DEDICATED TMR MODULE AND MCCP IN TIMER MODE**

| Features | TMR Module | MCCP Module |
|---|---|---|
| Number of 16-Bit Timers per Module | 1 | 2 |
| Number of 32-Bit Timers per Module | 2 | 1 |
| Trigger to Other Module | Matches the Timer Rollover | Can be Configured at a Different Time than the Timer Rollover |
| Clock Synchronization | Synchronous Only (except Timer1) | Asynchronous or Synchronous |
| Clock Source and Maximum Clock Frequency | Clocked from CPU Clock Only; Frequency is Limited by CPU Clock | If the Module is Clocked from REFO, then it can be Any Clock Source and Frequency is Not Limited by CPU Clock |

## Output Compare (PWM)

The MCCP offers new features, such as 32-bit operation and a variety of output modes. Table 7 shows the features comparison between the previous OC module and the new MCCP module in PWM mode.

**TABLE 7: COMPARISON BETWEEN DEDICATED OC MODULE AND MCCP MODULE IN PWM MODE**

| Features | OC Module | MCCP Module |
|---|---|---|
| Number of PWM Outputs | 1 | Two for MCCP1; Six for MCCP2-5 |
| Motor Control and Switching Applications | Not Supported | Supported (DC, BLDC Motors, Half and Full-Bridge Switches) |
| Dead-Time Control | Not Supported | Supported |
| Number of Modules for 32-Bit Operation | 2 | 1 |
| Clock Source and Maximum Clock Frequency | Clocked from CPU Clock Only; Frequency is Limited by CPU Clock | If Module is Clocked from REFO, then it can be Any Clock Source and Frequency is Not Limited by CPU Clock |

## Input Capture

The MCCP module can also be used as an input capture module in 16-bit or 32-bit mode. It is different from the previous dedicated peripheral, where two IC modules were required for 32-bit operation. In Input Capture mode, the MCCP module can be asynchronous and work from any clock source if it is used with the REFO module.

For more information, refer to **Section 14.0 "Capture/Compare/PWM/Timer Modules (MCCP)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) module on the PIC24FJ128GL306 devices significantly differs from the SPI module on the PIC24FJ128GA306 devices while maintaining capability. The changes are related to the Special Function Registers (SFRs), SPI clock generation, data width, Enhanced Buffering mode operation, interrupts and audio protocol support. For more information, refer to **Section 15.0 "Serial Peripheral Interface (SPI)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

The major changes in the SPI module features between the PIC24FJ128GA306 and PIC24FJ128GL306 devices are listed in Table 8.

**TABLE 8: SPI PERIPHERAL COMPARISON**

| Parameters | PIC24FJ128GA306 | PIC24FJ128GL306 |
|---|---|---|
| Data Width | Fixed to 8 or 16 Bits | Variable Width from 2 to 32 Bits |
| Enhanced Buffering Mode Data FIFO Depth | Fixed to 8 Words (8 or 16 bits) | 16 Words for Data, Up to 8 Bits, 8 Words for Data, Up to 16 Bits, 4 Words for Data, Up to 32 Bits |
| Master Mode Baud Rate Generator Settings | Primary, PPRE[1:0] (SPIxCON1[1:0]) and Secondary, SPRE[2:0] (SPIxCON[4:2]) | SPIxBRGL Register |
| Audio Protocol Interface Mode | Not Supported | Supported |
| Clock Source | Peripheral Clock | Peripheral Clock or REFO Module Clock |
| Interrupts | One Common Interrupt | General, TX Done and RX Done |
| Speed | 10 MHz | 16 MHz |

## INTER-INTEGRATED CIRCUIT ($I^2C$)

The Inter-Integrated Circuit ($I^2C$) module on the PIC24FJ128GL306 devices has a selectable data hold time to improve the SMBus and PMBus™ support. Also, interrupts are added on Start/Stop conditions. For more information, refer to **Section 16.0 "Inter-Integrated Circuit ($I^2C$)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

Table 9 summarizes the PIC24FJ128GL306 device-specific differences for the $I^2C$ registers.

**TABLE 9: SFR DIFFERENCES FOR PIC24FJ128GL306 $I^2C$ MODULE**

| SFRs | Differences from PIC24FJ128GA306 |
|---|---|
| I2CxCONL | The I2CxCON register is renamed as I2CxCONL in the PIC24FJ128GL306 devices and the IPMIEN bit is renamed as STRICT. |
| I2CxCONH | The I2CxCONH register does not exist on the PIC24FJ128GA306 devices. In the PIC24FJ128GL306 devices, it contains the bits: PCIE, SCIE, BOEN, SDAHT, SBCDE, AHEN and DHEN. These bits enable/disable interrupts on Stop/Start conditions, select the data hold time and control the address/data hold feature. |
| I2CxSTAT | The ACKTIM status bit has been added to the I2CxSTAT register. |


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## LIQUID CRYSTAL DISPLAY (LCD)

The Liquid Crystal Display is a new module with many new features added while maintaining backward compatibility.

The key differences between PIC24F128GA306 devices and PIC24F128GL306 devices include:

- Increased Segments (up to 256).
- In register LCDREG, BIAS[2:0] and MODE13 are unimplemented. However, display contrast can be adjusted using LCDCST[2:0] in the LCDREF register.
- In Charge Pump mode, LCDBIAS0 can be directly grounded; a capacitor need not be connected.
- Core-Independent Automatic Display Features:
  - Dual display memory used to display two different display contents
  - Blink mode of individual pixels or the complete pixels
  - Blanking of individual pixels or the complete pixels
  - Timing schedule can be changed without core intervention, based on user configurations

## REAL-TIME CLOCK AND CALENDAR (RTCC) WITH TIMESTAMP

This section provides a brief summary of the new features in the PIC24FJ128GL306 Real-Time Clock and Calendar (RTCC) module. For more detailed information, see **Section 19.0 "Real-Time Clock and Calendar (RTCC) with Timestamp"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

The RTCC is mostly unchanged, except for a few key features:

- Timestamp
- Improved Calibration Options
- Changes to SFRs

### Timestamp Registers

The Timestamp registers record the time and date of an external trigger event. The Timestamp registers can be updated by the RTCC module during Sleep modes.

### Calibration

The PIC24FJ128GL306 RTCC peripheral provides an increased range of clock control, enabling the use of the following clock sources:

- 32.768 kHz Crystal Oscillator
- 31 kHz Low-Power RC (LPRC) Oscillator
- External 50 Hz or 60 Hz Powerline Frequency

Coarse frequency division is controlled by the DIV[15:0] bits (RTCCON2H[15:0]) and fine control is provided by the FDIV[4:0] bits (RTCCON2L[15:11]).

### Registers

RTCC registers have been modified and expanded to accommodate the new features. Table 10 shows the control register differences. Table 11 shows how the time data stored in the PIC24FJ128GA306 SFRs line up with the SFRs in the PIC24FJ128GL306 devices. Table 11 only shows the changes for the current time, but the same alignment change applies to the Alarm and Timestamp registers.

**TABLE 10: RTCC CONTROL**

| Function | PIC24FJ128GA306 | PIC24FJ128GL306 |
|---|---|---|
| RTCC Configuration | RCFGCAL | RTCCON1L |
| Alarm Configuration | ALCFGRPT | RTCCON1H |
| Calibration | RCFGCAL | RTCCON2L |
| Power Control Clock Source | — | RTCCON3L |
| Status | RCFGCAL | RTCSTATL |

**TABLE 11: RTCC DATE/TIME SFRs**

| Data | PIC24FJ128GA306 SFR Bits | PIC24FJ128GL306 SFR Bits |
|---|---|---|
| Year | YEAR[7:0] | DATEH[15:8] |
| Month | MTHDY[12:8] | DATEH[4:0] |
| Day | MTHDY[5:0] | DATEL[13:8] |
| Weekday | WKDYHR[10:8] | DATEL[2:0] |
| Hour | WKDYHR[5:0] | TIMEH[13:8] |
| Minute | MINSEC[14:8] | TIMEH[6:0] |
| Second | MINSEC[6:0] | TIMEL[14:8] |

## CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLC) is a new module. It allows the application to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. For a complete overview of the CLC peripheral, refer to **Section 21.0 "Configurable Logic Cell (CLC)"** in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## DEADMAN TIMER (DMT)

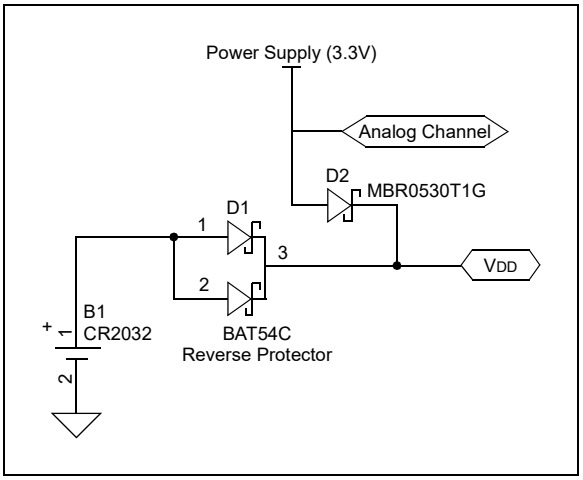
The Deadman Timer (DMT) is a new module. The primary function of the DMT is to interrupt the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer. The DMT is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

A DMT is typically used in mission-critical and safety-critical applications, where any single failure of software functionality and sequencing must be detected. For a complete overview of the DMT peripheral, refer to **Section 26.0 "Deadman Timer (DMT)**" in the *"PIC24FJ128GL306 Family Data Sheet"* (DS30010198).

## VBAT EMULATION

VBAT mode can be easily emulated in PIC24FJ128GL306 with minimal external components. Figure 1 shows a diagram for the VBAT emulation.

**FIGURE 1: VBAT EMULATION**




An analog channel can be configured to sense the main power supply. In case of loss in the power supply, the device can be put into Sleep mode.

For more details on VBAT Emulation, refer to application note, AN3329 – *"VBAT Emulation Using PIC24F eXtreme Low-Power Microcontrollers"* (DS00003329).

| **Note:** | Refer to the "*PIC24FJ128GL306 Family Data Sheet*" (DS30010198) for changes in electrical specifications. |
|---|---|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## GLOSSARY

# APPENDIX A: REVISION HISTORY

## Revision A (April 2019)

This is the initial version of this document.

## Revision B (July 2020)

Updated sections, **"Liquid Crystal Display (LCD)"** and **"VBAT Emulation"**, and corrected the LCD description in the **"Glossary"**.


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ISBN: 978-1-5224-6387-0

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