AN3361

Designing an IEEE® 802.3af/at/bt PoE System Based on PD692x0/PD69208

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a Power over Ethernet (PoE) Power Source Equipment (PSE) system, based on Microchip's PD69208T4, PD69204T4, or PD69208M PoE Managers and PD69210, PD69220 or PD69200 PoE Controllers. This document enables designers to integrate PoE capabilities (as specified in IEEE® 802.3af, IEEE 802.3at, IEEE 802.3bt, and PoH standards) into an Ethernet switch.

The Microchip family of PSE Controllers include the PD69210, PD69220, and PD69200. The PD69210 is recommended for all new designs. The PD69200 and PD69220 are available for existing designs.

The PD69208T4 and PD69208M devices are 8-port, mixed-signal, high-voltage PoE drivers. The PD69204T4 device is a 4-port, mixed-signal, high-voltage PoE driver. The PD69208T4 or PD69204T4 device supports up to type-4, 90W power while the PD69208M supports up to type-3 PSE, 60W. Any combination of PD69208T4, PD69204T4, and PD69208M and any combination of 2-pair and 4-pair in the same system is possible and supported.

The PD69210, PD69220, and PD69200 Controllers when paired with the Microchip PD69208T4, PD69204T4, or PD69208M Managers are part of a PoE PSE system. This system enables designers to integrate enhanced mode PoE capabilities, as specified in IEEE 802.3af, IEEE 802.3at, IEEE 802.3bt, and PoH standards, into an Ethernet switch. Using a single PD692x0 Controller, up to a 48-logical port switch can be implemented, either 4-pair or 2-pair, using up to 12 PD69208 Managers. Any combination of PD69208M, PD69208T4, and PD69204T4 can be implemented.

The chip-set supports PoE Powered Device (PD) detection, power-up, and protection according to IEEE standards, and the legacy/pre-standard PD detection. It provides PD real-time protection through the mechanisms, such as overload, under-load, over-voltage, over- temperature, and short-circuit, and enables operation in a standalone mode. It also executes all real-time functions as specified in IEEE 802.3at/bt high-power and Power Over HDBaseT (PoH) standards, including PD detection, and classification; using Multiple Classification Attempts (MCA).

Microchip offers complete Evaluation Boards (EVBs). For an Evaluation Board recommendation or access to device data sheets or related application notes, please consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe.

Firmware (without the boot section), GUI, and API are available on Microchip's Software Library.

For technical support, consult your local Embedded Solutions Engineers or go to microchipsupport.force.com/s/.

Features

- A single PD692x0 Controller supports up to 48 2-pair or 4-pair logical ports.
- IEEE 802.3af-2003 standard compliant (Type 1)
- IEEE 802.3at-2009 standard compliant (Type 2)
- IEEE 802.3bt-2018 standard compliant (Type ¾)
- Power over HD BaseT standard compliant (60W/ 95W)
- Configurable standard/reduced capacitor detection mode
- Supports pre-standard PD detection
- Single DC voltage input (44 V_{DC}–57 V_{DC})
- Up to five event classification
- Voltage monitoring/protection
- Low power dissipation
- Internal sense resistor (0.1Ω)
- Internal MOSFET with low RDS_ON (approximately 0.24Ω)
- Internal power on reset
- 6 kV 1.5 µs × 50 µs immunity per ITU-T k.21 2018
- Includes reset input from hosting system
- Four direct Manager address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- On-chip thermal protection
- Built-in 3.3 V_{DC} and 5 V_{DC} regulators
- Emergency power management supporting sixteen configurable power banks
- Can cascade up to 12 PoE devices (48 logical ports in four pairs configuration)
- Supports 2-pair or 4-pair connection
- Wide temperature range: –40 °C to 85 °C
- PD69210, PD69220 MSL1
- PD69208, PD69204, and PD69200 MSL3
- RoHS compliant
- Supports I^2C and UART communication and software update

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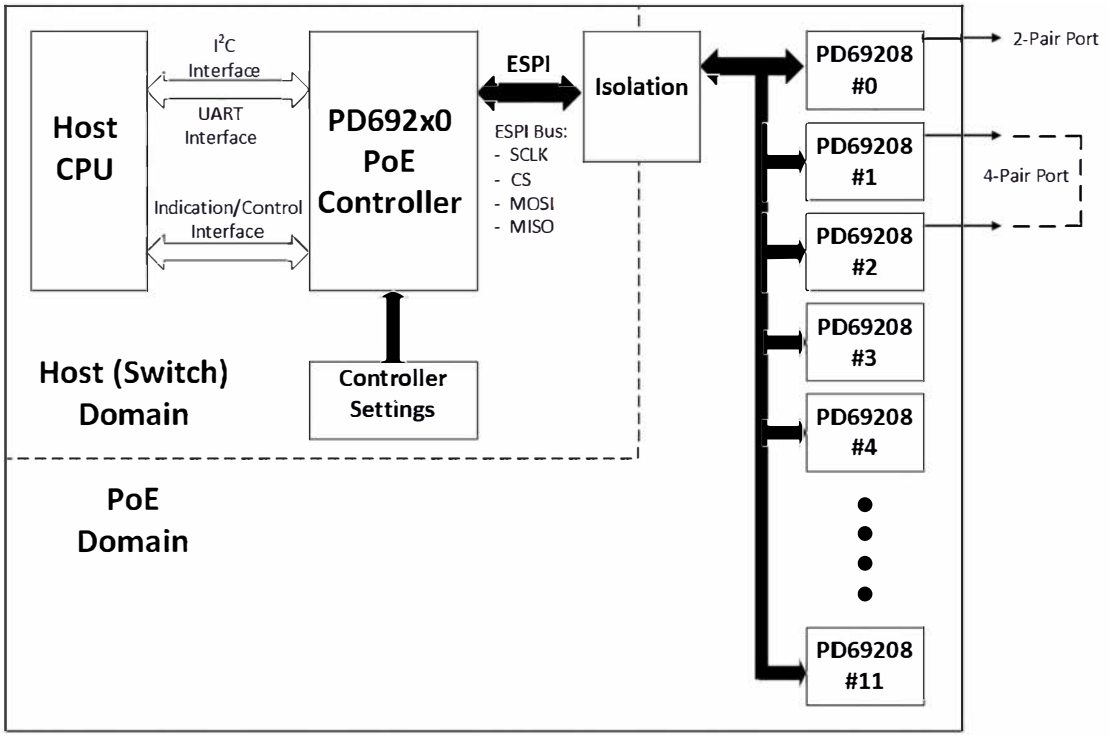
1. Functional Descriptions

A typical application includes the following blocks.

- PoE circuit for 48 logical ports, either 4-pair or 2-pair, based on up to twelve PD69208 Managers per single PD692x0 Controller. See the following figure.
- Controller circuit, used to initialize, control, and monitor each of the PD69208 through an internal Enhanced Serial Peripheral Interface (ESPI) isolated bus. The PoE controller communicates with the host CPU through a non-isolated UART or an I^2C interface.
- Isolation circuit for ESPI bus.

These blocks are shown in the following figure.

Figure 1-1. 48 2p or 4p Logical Port Configuration Block Diagram



1.1 Communication Interfaces

There are two communication interfaces: An interface between the host CPU and the PoE controller and an interface between the PoE controller and PoE managers.

Communication between the host CPU and the local PoE controller is performed through a UART or an I^2C interface. The host CPU issues commands, utilizing a dedicated serial communication protocol to the PoE controller. For more information, see the *PD692x0 Serial Communication Protocol User Guide* or the *PoE Host Software Communication API IEEE 802.3af-at-bt User Guide*. This interface does not require isolation.

Communication between the PoE controller and the PoE managers is through the ESPI bus with1500 V_{RMS} isolation. This interface is a standard SPI. The PoE controller converts the serial communication protocol to ESPI communication and sends it through isolated ESPI lines to the appropriate PD69208. Isolation is a basic requirement of IEEE PoE standards. The isolation circuit is comprised of a digital isolator. Consult Microchip for choice of isolator as we have pricing arrangements for the digital isolator. Each side of the isolator circuitry is fed by a separate power supply.

Additionally, there are several signals connected between the host CPU and the PoE controller for control and indication functions.

1.1.1 Host–PoE Controller Communication Management

UART (set to 19200 bps) or I²C (up to 400 KHz) communication between the host CPU and PoE controllers are managed by setting the PD69210 address, pin number 13 (I2C_ADDR) or the PD69220/ PD69200 address, and pin number 22 (I2C_ADDR), as shown in the following figure and table.

Figure 1-2. PD692x0 Communication Management

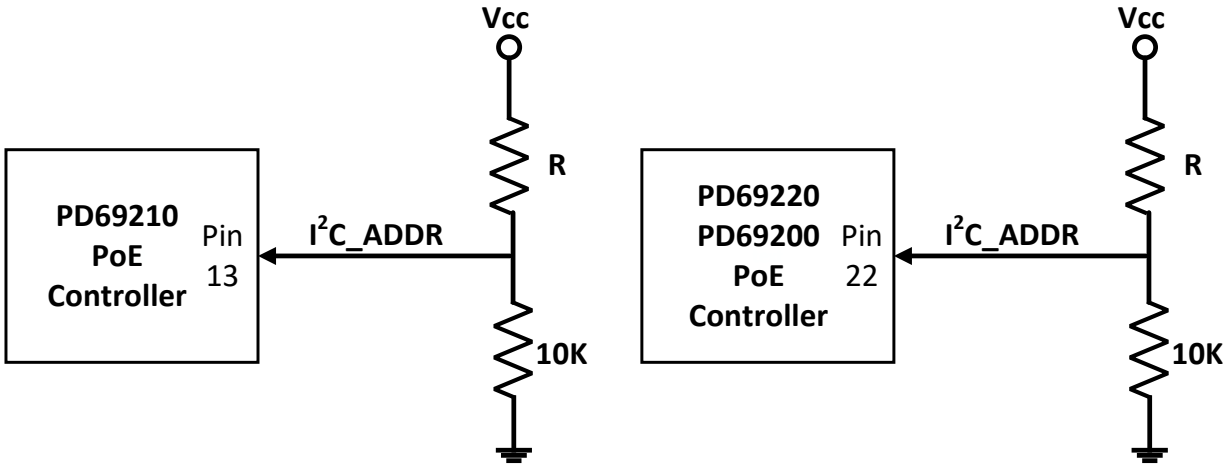


Table 1-1. Serial Communication Configuration

I²C Address	Address (Hex)	PD69210 R (KΩ 1%) Pin 13	PD69220 R (KΩ 1%) Pin 22	PD69200 R (KΩ 1%) Pin 22
#0	UART	N.C.	N.C.	N.C.
#1	0x4	147	147	97.6
#2	0x8	86.6	86.6	53.6
#3	0xC	57.6	57.6	35.7
#4	0x10	43.2	43.2	25.5
#5	0x14	34	34	19.1
#6	0x18	26.7	26.7	14.7
#7	0x1C	22.1	22.1	11.3
#8	0x20	18.2	18.2	8.87
#9	0x24	15.4	15.4	6.81
#10	0x28	13	13	5.23
#11	0x2C	11	11	3.92
#12	0x30	9.31	9.31	2.80
#13	0x34	7.87	7.87	1.87
#14	0x38	6.49	6.49	1.02
#15	0x3C	5.49	5.49	0.324

1.1.2 Host–PoE Controller Pin Connections

For UART communication, the PoE controller Rx is the data receiving pin and must be connected to the host Tx that is the data transmission. By the same logic, the PoE controller Tx must be connected to the host Rx. A pull-up resistor is required on the UART communication line.

For I^2C, a pull-up resistor is required on the I^2C communication lines (pins 21 and 22 for PD69210; pins 20 and 21 for PD69200/PD69220).

The PD692x0 requires the host to support I^2C clock stretch.

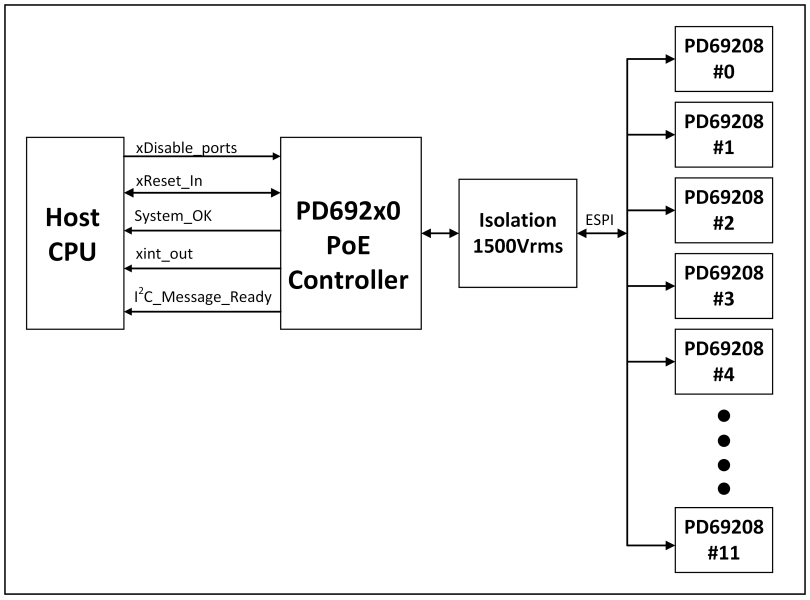
Table 1-2. Host-PoE Controller Pin Connections

Interface	Function	PD69210 Controller	PD69220 PD69200 Controller
UART	UART receive from a host	16	11
UART	UART transmit to host	15	12
I^2C	SDA I^2C bidirectional data	21	21
I^2C	SCL I^2C bidirectional clock	22	20

1.1.3 Host–PoE Controller Control Signals

Control signals are single hardware lines that run between the host CPU and the PoE controller, as shown in the following figure.

Figure 1-3. Control and Indication Signals



xDisable_ports: Control signal driven by the host CPU disables all PoE ports. When the PoE controller detects a low-level voltage at the PD69220/PD69200 pin 31 or PD69210 pin 4, it sends a disable command through the ESPI bus to all PoE manager ports.

xReset: Control signal driven by the host CPU resets the PoE controller and all PoE managers. When the PoE controller detects a low-level voltage at PD69200/PD69220 pin 19 or PD69210 pin 26, it enters the Reset mode and all of its output pins switch to the Tri-State mode. When xReset returns to high, the PoE controller initializes and sends a `RESET` command to the PoE managers through the ESPI bus. xReset is also used by the PoE controller watchdog to reset itself. Therefore, the host must drive a reset using an open-drain output and a 10 KΩ pull-up. A 47 nF filter capacitor must be connected between this pin to GND/FGND, close to the device. If the host drives the reset pin from a push-pull output, then a 1.5 KΩ resistor must be located between the host's output and the PD692x0 xReset_In.

The shortest reset pulse from the host that is required for the PD692x0 application is 150 µs. The controller can generate self-reset. In this case, the xRESET pin is driven low by the controller for about 100 µs. The required shortest reset pulse in this case is 300 µs.

As required by the application, the PoE controllers can reset themselves and it is not recommended to connect the xReset signal to the common reset signal of the whole system, to prevent whole system reset when the PD692x0 resets itself.

xSYS_OK: Signal is generated by the PoE controller, indicating that the main input voltage is within range. This pin is determined by a 15-byte serial communication protocol.

xINT_OUT: Interrupt output indication. This line is asserted low when a preconfigured event is in progress. The host configures the event that should generate an interrupt through 15-bytes protocol. When this event occurs, the xINT_OUT pin is asserted. This pin is active low.

xI2C_MESSAGE_READY: I^2C message ready for reading by the host. The controller asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I^2C read cycle only when the message is ready. This pin is active low. After the host reads the data from the controller, this pin is asserted to high.

1.1.4 ESPI Bus

The PoE PD692x0 controllers features a 1 Mbps ESPI for each of the PoE managers. The ESPI bus consists of a Master Out/Slave In (MOSI) that provides communication from the PoE controller to the PD69208 and a Master In/Slave Out (MISO) that provides communication from the PD69208 to the PoE controller. SCK is the serial clock generated by the controller. Chip Select (CS) is utilized by the PoE controller to transmit data simultaneously to all PD69208 ICs, while only the chosen PoE manager responds.

1.2 Powering

The following sections describe powering.

1.2.1 Supply

The PoE controller requires stable, filtered power for its operation coming from the host (3_3V_iso), so a number of decoupling capacitors are included in the design (C56, C71, C92 for PD69200/PD69220 and C13, C15, C16, C17 for PD69210). The expected current consumption of the PoE controller circuitry must be below 20 mA.

Additionally, for the PD69210 the 1.2V VDD_CORE voltage requires decoupling capacitors. These are capacitors C12, C14 and must be layout close to pin 29.

1.2.2 Main Supply

The PoE system operates within a range of 44 V_{DC} to 57 V_{DC} (IEEE 802.3at/bt V_{MAIN} range is 50 V_{DC} to 57 V_{DC}). To comply with UL SELV regulations, the maximum output voltage must not exceed 60 V_{DC}.

1.2.3 Hot-Swap Circuit

The hot-swap circuit is crucial for applications where DC hot plug is present because the absence of such a circuit causes the DC voltage to oscillate (ring), which leads to application malfunctions. The selected MOSFET is rated for 80A and the RDS is 10 mΩ.

1.2.4 Grounds

Several grounds are utilized in the system: PoE domain analog, PoE domain digital, chassis, and host domain floating.

Digital and analog grounds are the same ground, electrically. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

The power supplies' AGND ground connector enables the current a path back to the power supply. The ground connection must be capable of carrying all current back to power supplies.

The chassis ground is connected to the switch’s chassis ground. This ground plane should be 1500 V_{RMS} isolated from PoE circuitry.

The PoE controller relates to the host domain floating ground, which is isolated from the PoE domain grounds.

1.2.5 5 V_{DC} and 3.3 V_{DC} Regulators

Each PD69208 has a 5 V_{DC} and a 3.3 V_{DC} regulator for internal IC circuitry and can provide up to 6 mA to be utilized for powering components in the PoE domain. The 5V is powered from V_{MAIN} by an internal regulator and the 3.3V is powered from the 5V with another internal regulator. To minimize time between the 5V and 3.3V rise during the first system power up, a 4.7 µF capacitor must be placed between those pins (pin 20 and pin 22).

An external boost transistor can be added to the 5 V_{DC} regulator's output (instead of R1007) to increase the current, as shown in Figure 4-8. The transistor can provide a total of 30 mA to the PoE controller and to other circuits in the PoE domain, if needed. This total current is the sum of 5V and 3.3V currents. All external components in this circuitry should also be isolated from the switch circuitry by 1500 V_{RMS}.

Using a boost transistor reduces the internal heat generated by the PD69208.

1.2.6 Clock

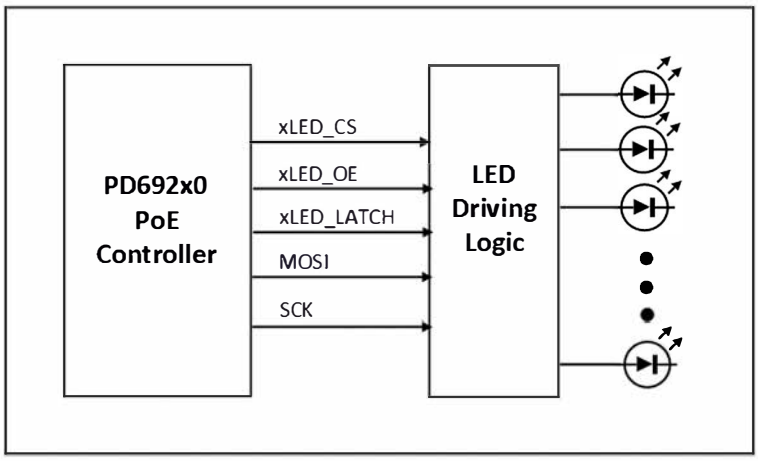
The PoE controllers run at 47.972 MHz, facilitated by an internal clock.

1.3 LED Support

LED support for port status indication is accomplished by utilizing the ESPI bus (SCK and MOSI), xLED_CS, xLED_OE, and xLED_Latch signals. Bus behavior is 1 MHz synchronous serial communication (clock and data) in one direction (write only) that transmits the status up to 48 logical ports.

The following figure shows the SPI bus and LED support.

Figure 1-4. SPI Bus and LED Support



1.4 Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended that each power supply be capable of generating a logic signal, indicating its operate/fail status. For more information, see Figure 1-5.

The following table lists the pins used for emergency power management.

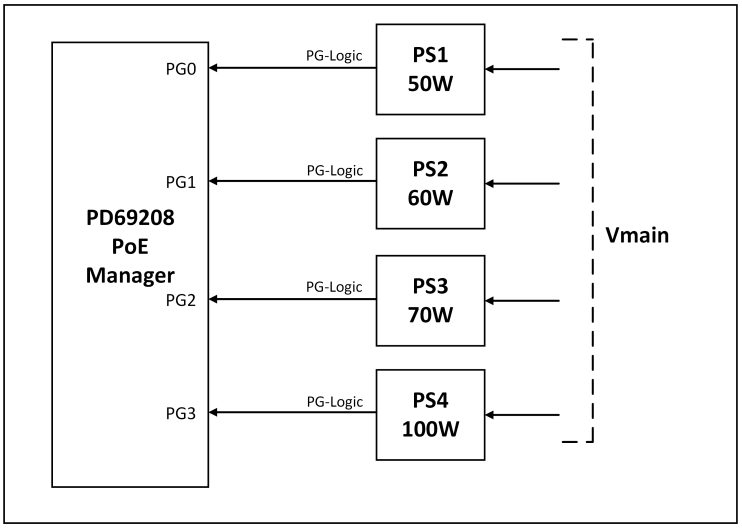
Table 1-3. Emergency Power Management Pins

PD69208 Pin Number	Signal	Description
56	PG0	Power Good 0
41	PG1	Power Good 1
46	PG2	Power Good 2
47	PG3	Power Good 3

The PoE circuit allocates power to the system in 16 power levels (power banks) programmed by users. Power bank values are based on each supplies' available power and on the state of the logic signals PG[0..3] coming from power supplies. If PG pin is not used, the pin must be connected to GND or V_{DD}.

The following figure shows the connections between the logic signals of the power supplies and the PoE manager.

Figure 1-5. Power Good



Note: The system V_{MAIN} capacitor should hold the voltage from dropping for 5 µs until the emergency power management reacts.

1.5 PoE Manager Circuitry

The PD6920x performs a variety of internal operations and PoE functions, requiring a minimal number of external components. The PoE manager number with its related components for an 8-port 2-pair configuration is shown in Figure 4-7. For 48 2-pair ports, this is circuitry is duplicated six times.

1.5.1 Reference Current Source

The reference for internal voltages within the PD69208 is set by a precision resistor (R51), 28.7 kΩ 1%. In a PoH and IEEE 802.3bt system, the resistor precision must be 0.1%.

1.5.2 Sense Resistors

The PD6920x provides an internal sense resistor of 100 mΩ. This resistor is utilized to measure port current.

1.5.3 Front-End Components

A front-end, per-line capacitor is required. The capacitor value can be between 22 nF and 220 nF. Using 220 nF is recommended to improve the PSE immunity to 50 Hz/60 Hz noise. All other components such as reverse diode, port protection, sense resistor, and switching MOSFET are internal.

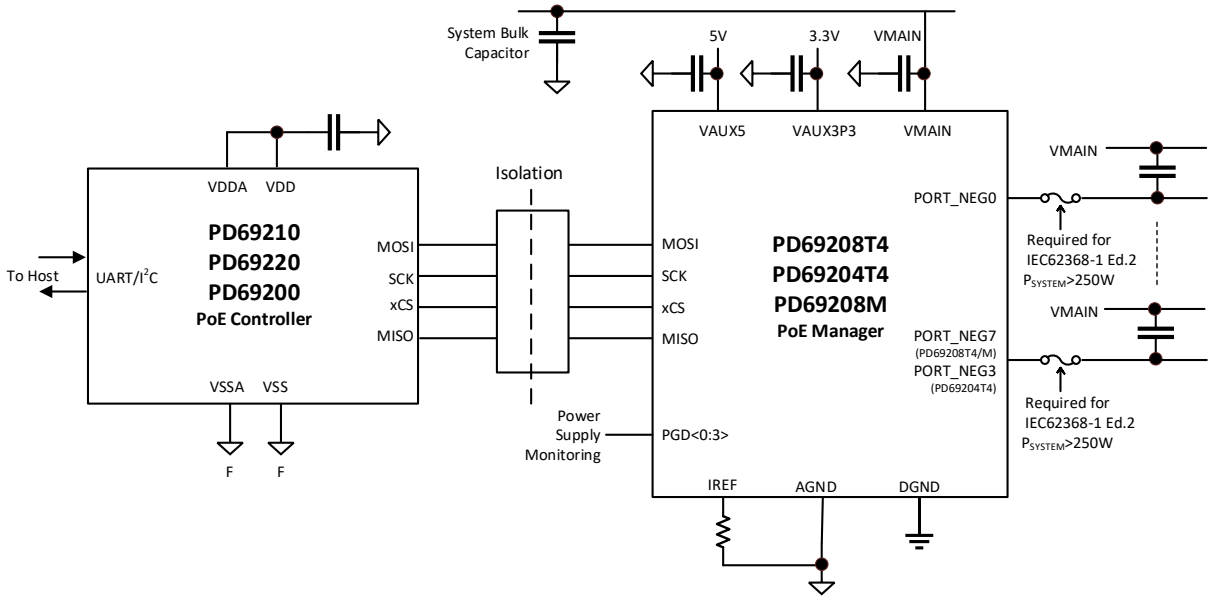
All IEEE 802.3bt/at/af standards contain a safety requirement stating the PoE PSE must be classified as a Limited Power Source (LPS) in accordance with IEC 60950-1 and/or IEC 62368-1. In December 2020, the IEC 60950-1 standard was formally withdrawn, and the LPS requirements were governed solely by the scope of IEC 62368-1 for IEEE 802.3af/af/bt. IEC 62368-1 Edition 2 was enforced in December 2020. Compliance to IEC 62368-1 Ed.2 LPS requirements involved the addition of a per port fuse for systems with a total power supply greater than 250W. IEC 62368-1 Edition 3 was enforced in January 2023. The per-port fuse may not be required in IEC 62368-1 Edition 3.

See *AN3527 Compliance to Limited Power Source Requirements* for more details.

Microchip has a special pricing arrangement for a fuse that is intended to be used in IEEE 802.3bt/at that is IEC 62368-1 Ed.2 compliant. Consult your local Microchip Client Engagement Manager or Embedded Solutions Engineer for details on this offering.

The following figure shows the front-end components of the PD69208 Manager.

Figure 1-6. 8-Port Front-End Components



1.6 Line Transformer

A line transformer that is dedicated to PoE (with the desired PoE current for the specific applications in mind) must be used.

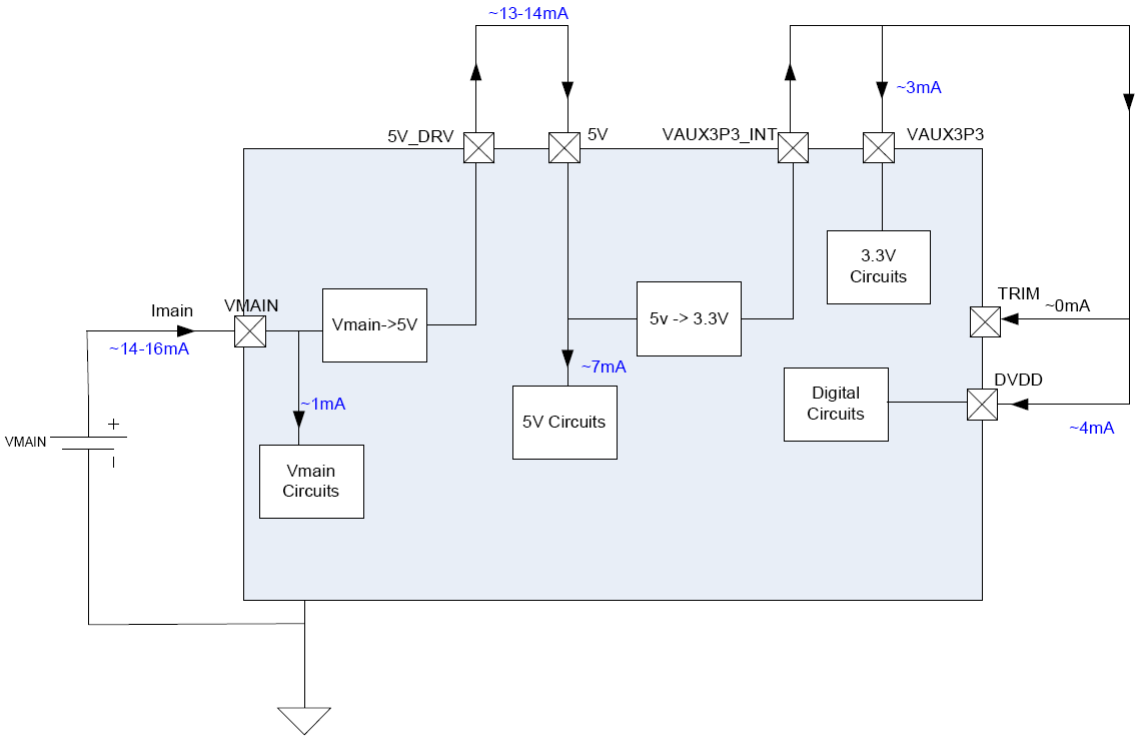
2. PD69208 5V and 3.3V Power Supply Connection Options

The following 5V and 3.3V power supply connection options are available for the PD69208.

- 5V internal/3.3V internal
- 5V external using NPN transistor/3.3V internal
- 5V external/3.3V internal
- 5V external/3.3V external (two external parallel regulators)
- 5V external/3.3V external (two external serial regulators)

The following connection is a default design, as shown in Figure 4-7. Using this connection, PD69208 internally regulates the V_{MAIN} voltage (~54 V) into 5V, and the 5V is regulated into 3.3V.

Figure 2-1. 5V Internal/3.3V Internal



The following connection is a default design, as shown in Figure 4-8. This connection externally generates 5V and reduces internal heat generated by PD69208.

Figure 2-2. 5V External Using NPN Transistor/3.3V Internal

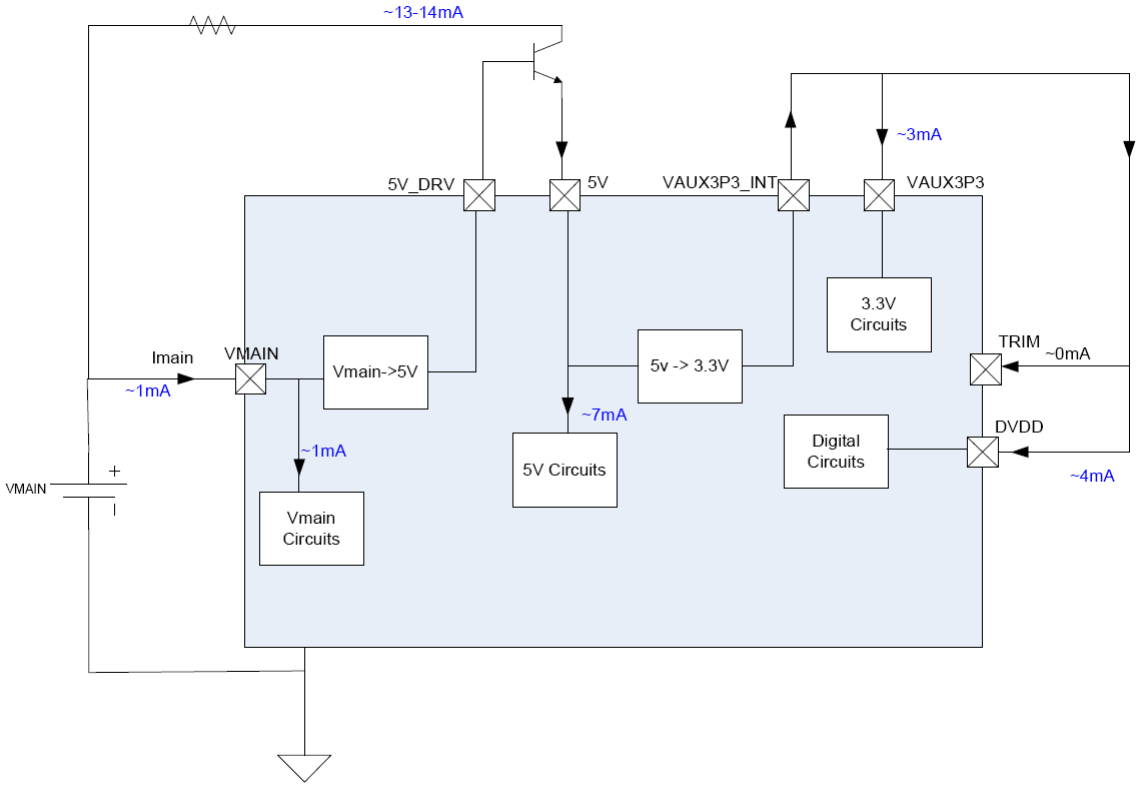


Figure 2-3. 5V External/3.3V Internal

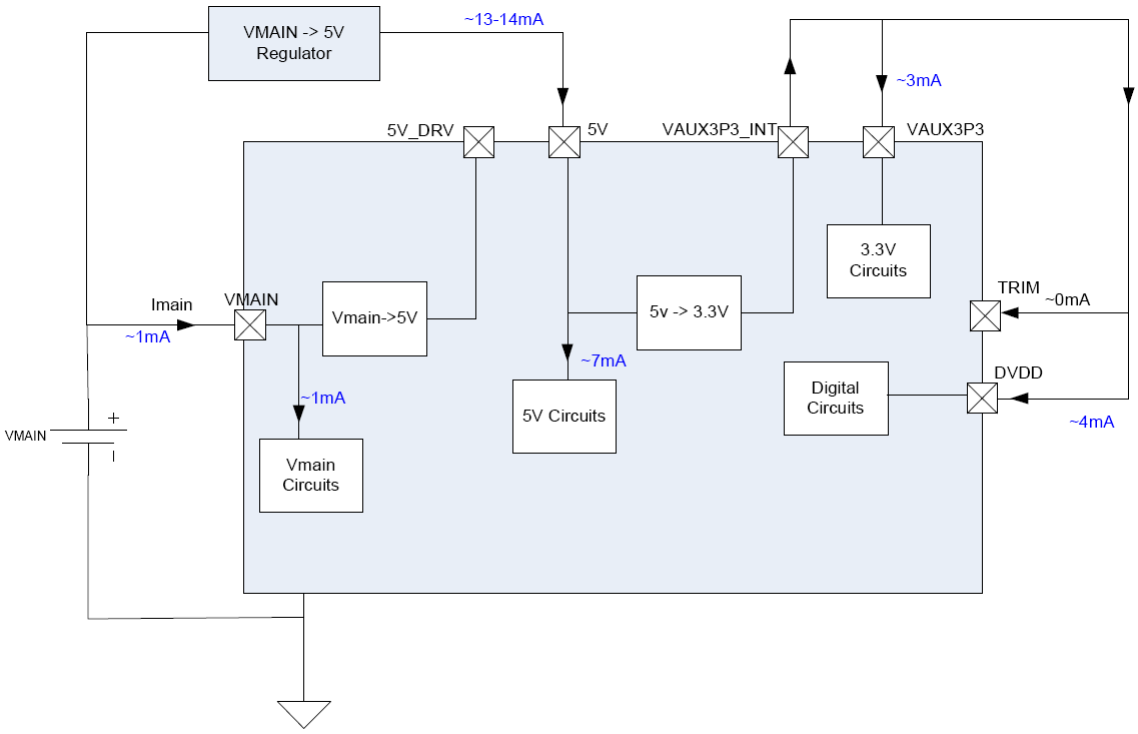


Figure 2-4. 5V External/3.3V External (Two External Parallel Regulators)

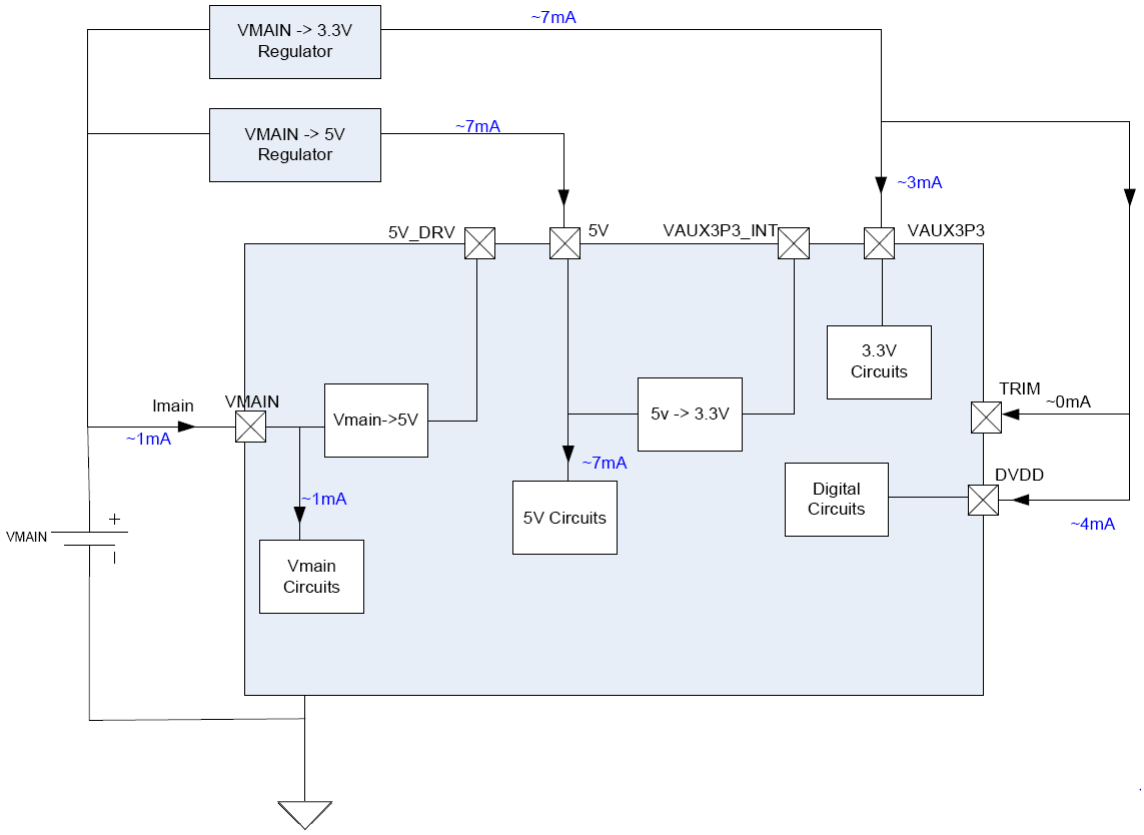
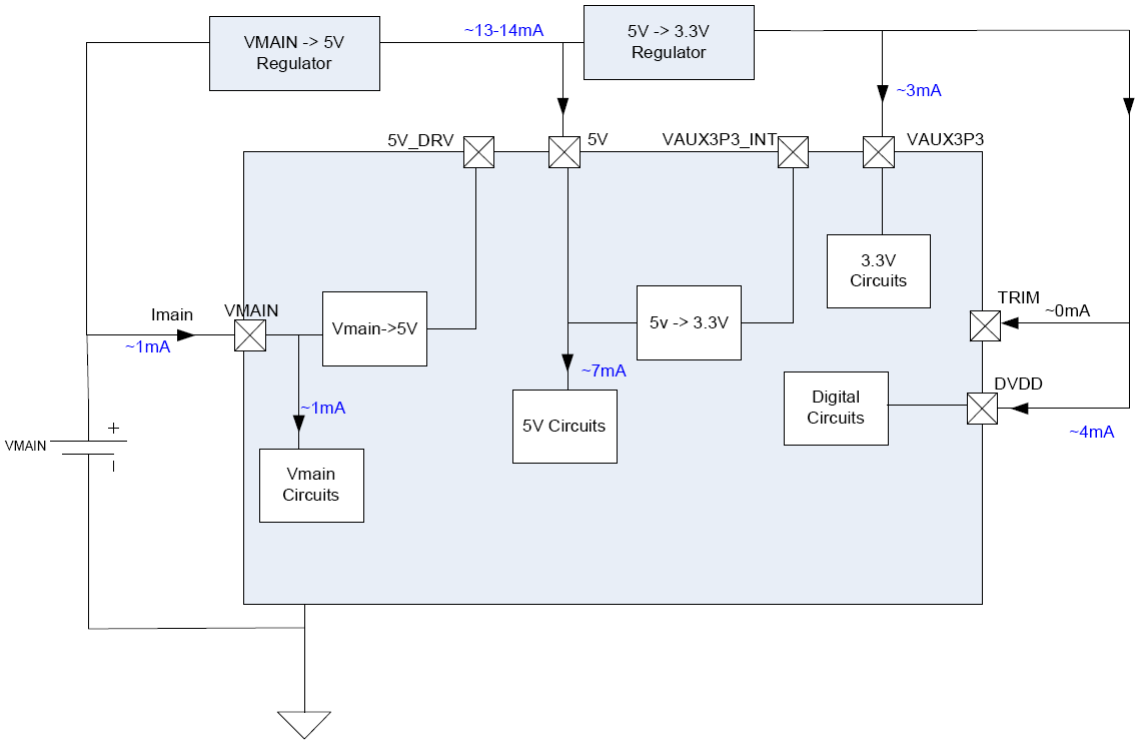


Figure 2-5. 5V External/3.3V External (Two External Serial Regulators)



3. 4-Pair Ports for IEEE 802.3bt

This section describes the basic steps to configure PSE systems to support IEEE 802.3bt 4-pair applications based on the PD692x0 PoE Manager and PD69208M-PD69208T4 PoE manager.

3.1 Background

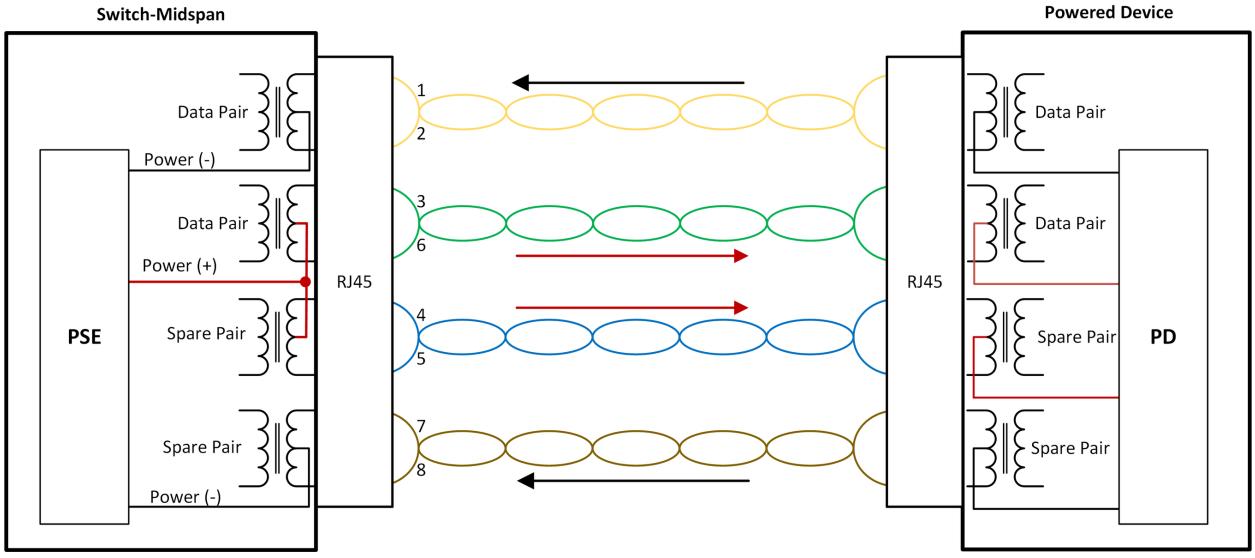
The IEEE 802.3af standard described PSE power of 15W over 2-pair and the IEEE 802.3at standard described PSE power of 30W over 2-pair. To increase the maximum PoE power supplied by the PSE to the PD, 4-pairs ports utilizing all four pairs of the structured RJ45 wiring are used.

The IEEE 802.3bt-2018 standard, introduced the “Type 3” and "Type 4" PSE/PD capable of supporting 60W/90W output power using two PSE ports on all wires of the RJ45 cable.

The PD69208M supports up to 30W per 2-pair or 60W per 4-pair (Type 3). The PD69208T4 supports up to 45 W per 2-pair or 90W per 4-pair (Type 3 or Type 4).

The “Data Pair” is defined as “Alternative A” at the PSE side and “Mode A” at the PD side. The “Spare Pair” is defined as “Alternative B” at the PSE side and “Mode B” at the PD side, as shown in the following figure.

Figure 3-1. PoE 4-Pair Architecture



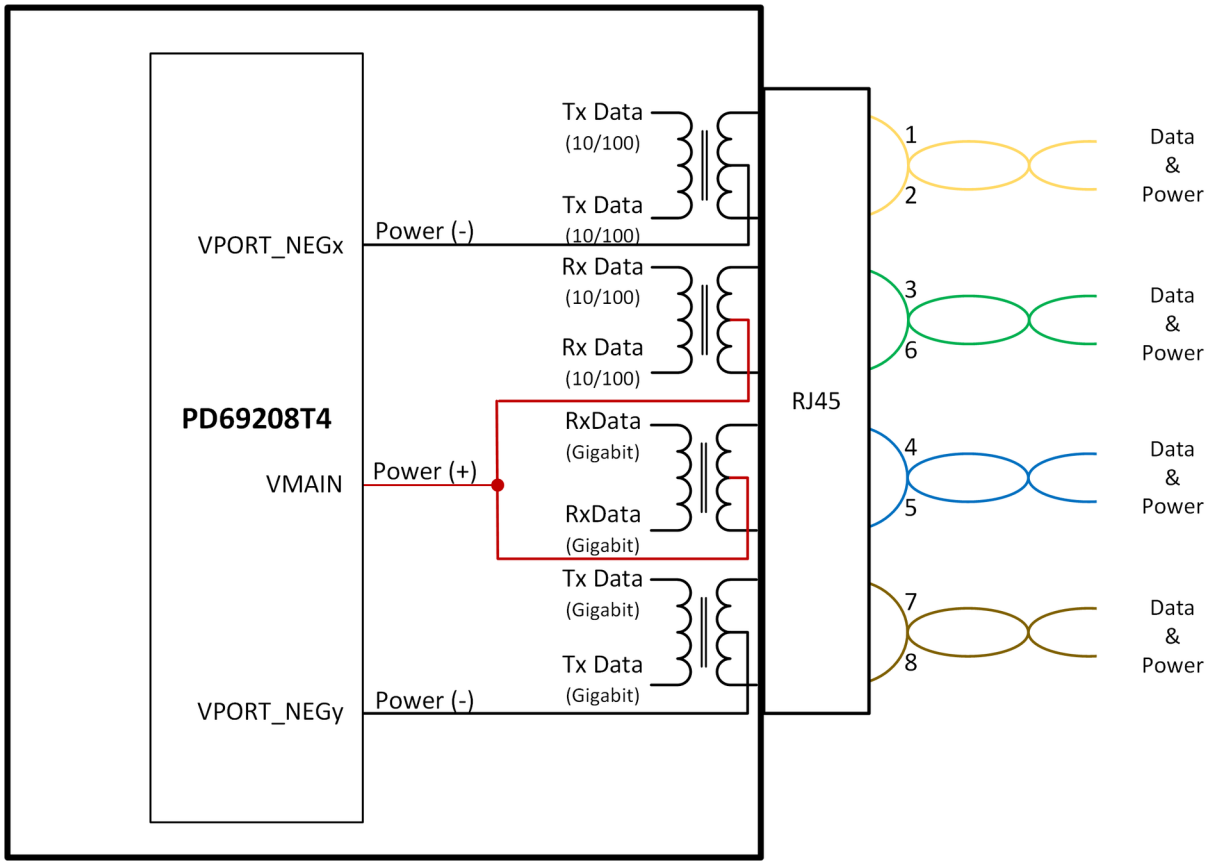
3.2 Hardware Setup

The following sections describe how to set up the hardware.

3.2.1 PSE

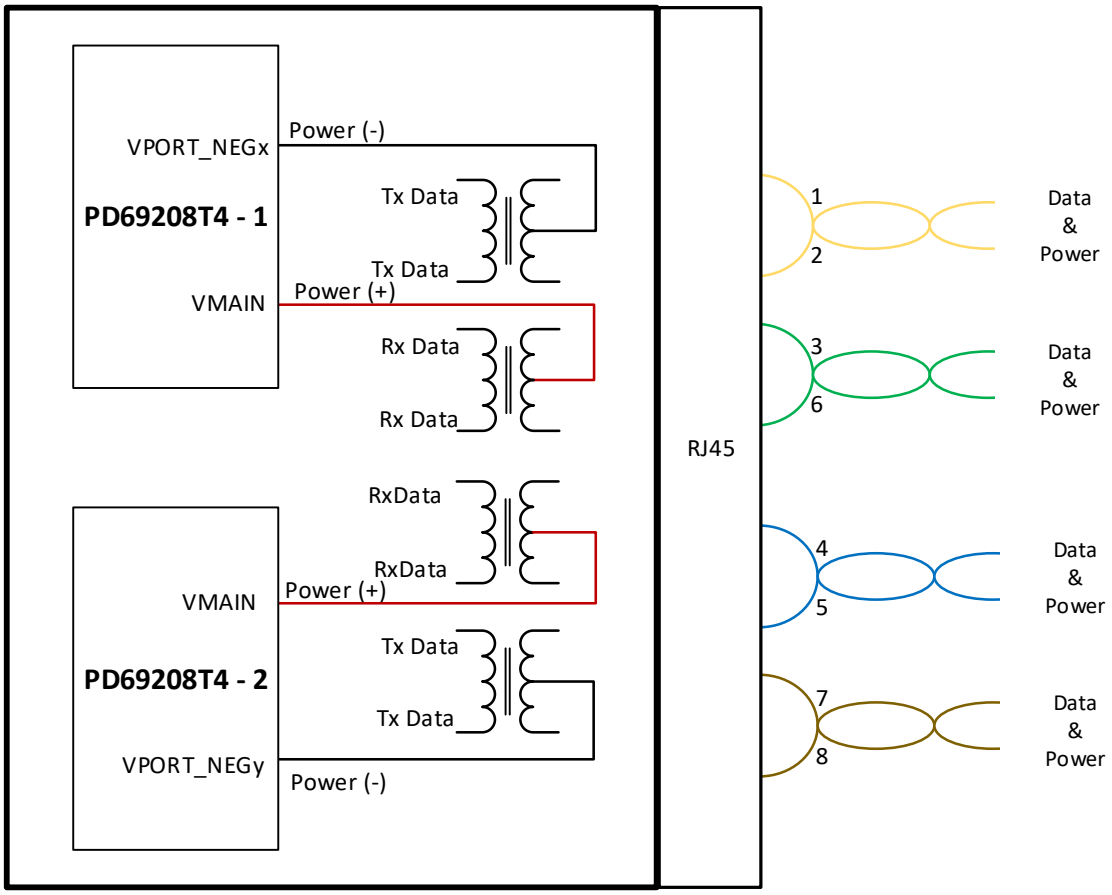
There are different ways to physically implement 4-pair powering. The system designer must consider heating effect, PCB lay-out, and so on, before making the decision. In one configuration, all the 4-pair come from a single PD69208 IC. This makes the PCB layout simpler. The following figure shows this configuration.

Figure 3-2. Single Manager 4-Pair Implementation



An alternative configuration is to take the first 2-pair from one PD69208 IC and the second 2-pair from a second PD69208 IC. Microchip recommends using different ICs to minimize heating of the ICs. There are many ways to implement 4-pair powering by using two PD69208 ICs. Microchip suggests taking the first 2-pair from Alternative A of IC1 and the second 2-pair from Alternative B of IC2 (and vice versa). This is shown in the following figure.

Figure 3-3. Dual Manager 4-Pair Implementation



3.2.2 Polarity

Type 4 is limited to a fixed polarity, that is, the IEEE 802.3bt strictly defines the connection of the positive V_{MAIN} voltage and return (PORT_NEG) paths to the physical pairs. For Type 3 applications, the standard is flexible, allowing a variety of connection options, as listed in the following table.

Table 3-1. Allowed Polarity

Pair Set	TIA/EIA 568-A	TIA/EIA 568-B	Alternative	Type 3			Type 3 Type 4
1–2	Green	Orange	Data (Alt A)	PORT_NEGx	VMAIN	VMAIN	PORT_NEGx
3–6	Orange	Green		VMAIN	PORT_NEGx	PORT_NEGx	VMAIN
4–5	Blue	Blue	Spare (Alt B)	PORT_NEGy	PORT_NEGy	VMAIN	VMAIN
7–8	Brown	Brown		VMAIN	VMAIN	PORT_NEGy	PORT_NEGy

3.2.3 PD Side

The following figures show how to physically connect 4-pair ports to a Signal Signature PD, and how to physically connect to a Dual Signature PD.

Figure 3-4. PD 4-Pair SSPD Implementation

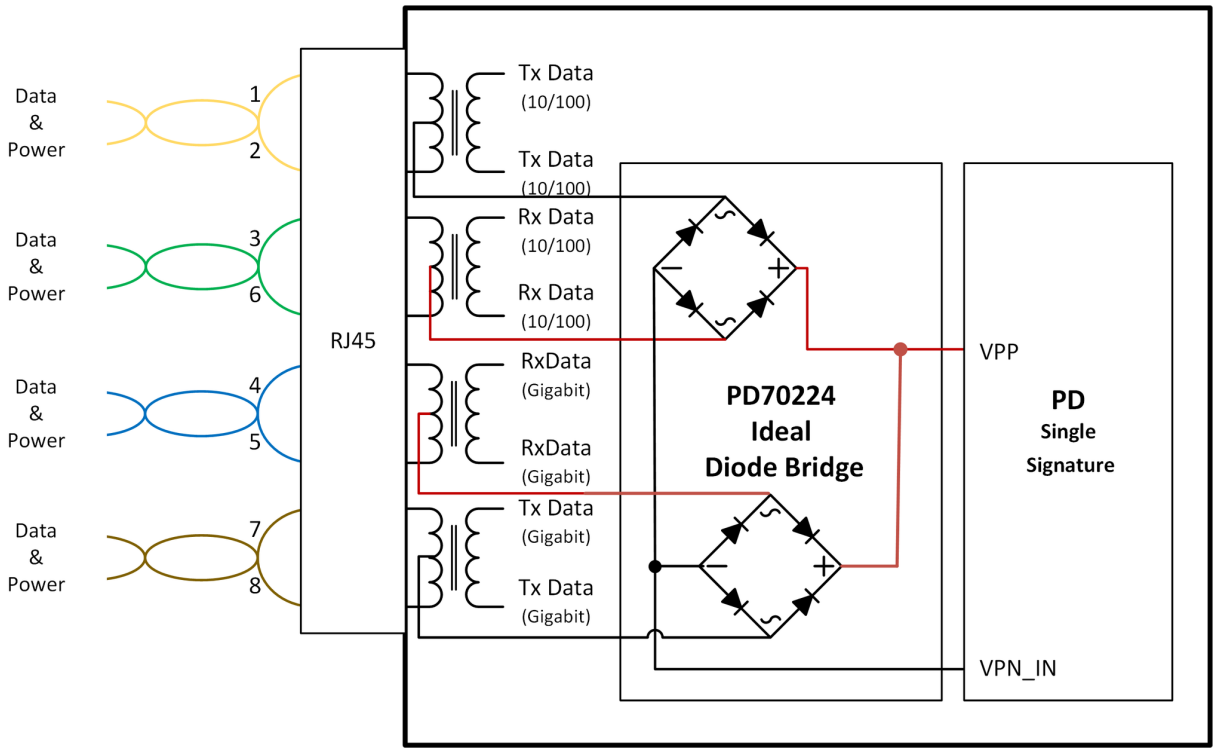
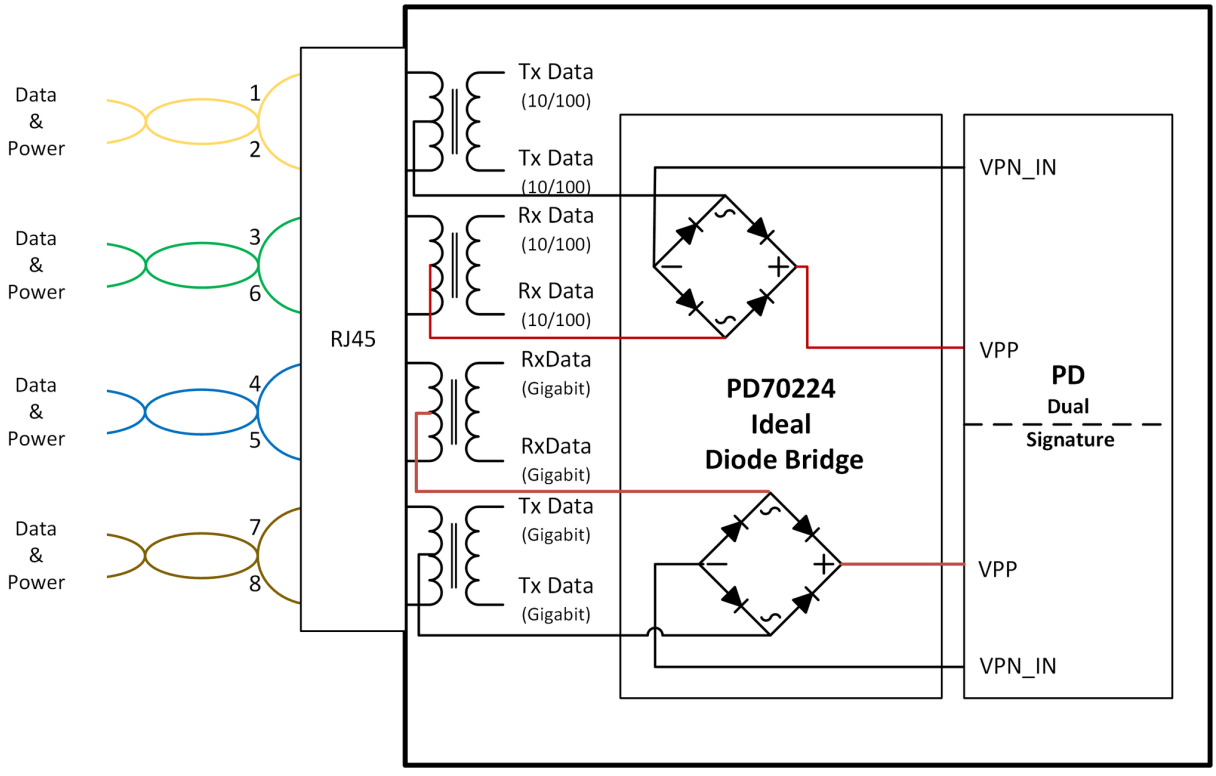


Figure 3-5. PD 4-Pair DSPD Implementation



3.3 Controller Setup

One logical port is implemented by utilizing two physical ports of the PD69208M/T4 PoE manager, as described in the previous section. Each physical 2-pair port delivers a maximum of 30W/45W of power, enabling delivery of 60W/90W over 4 pairs. The 4 pairs, which are two physical ports, are considered as one logical port by the PoE firmware. Each of the two physical ports drives separate 2 pairs, which are connected together inside the PD after the diode bridges, as shown in Figure 3-4, or can be separated to implement a dual signature PD architecture, as shown in Figure 3-5

The ports are managed by PD692x0 with certain rules. The PD692x0 device can support up to 48 logical 4-pairs ports (96 physical ports).

The host must set command values in the port conversion matrix (temporary matrix) according to the PCB layout. Programming this matrix sets the internal port numbering arrangement with respect to the host system port numbering. This matrix feature gives the designer flexibility in laying out PCB traces. The command supports a mix of 4-pair/2-pair configurations, and any combination of AF, AT, and BT power levels. The command supports up to 48 logical ports (0 to 47) and up to 96 physical ports (0 to 95). Port count starts from 0 in system and in device. Device numbering is based on SPI address settings (the lowest address that responds to MCU messaging is treated as the first device). The automatic device search is performed after any MCU Reset. Physical port numbering must be calculated based on the number of valid PoE device addressing and the number of supported ports on each device.

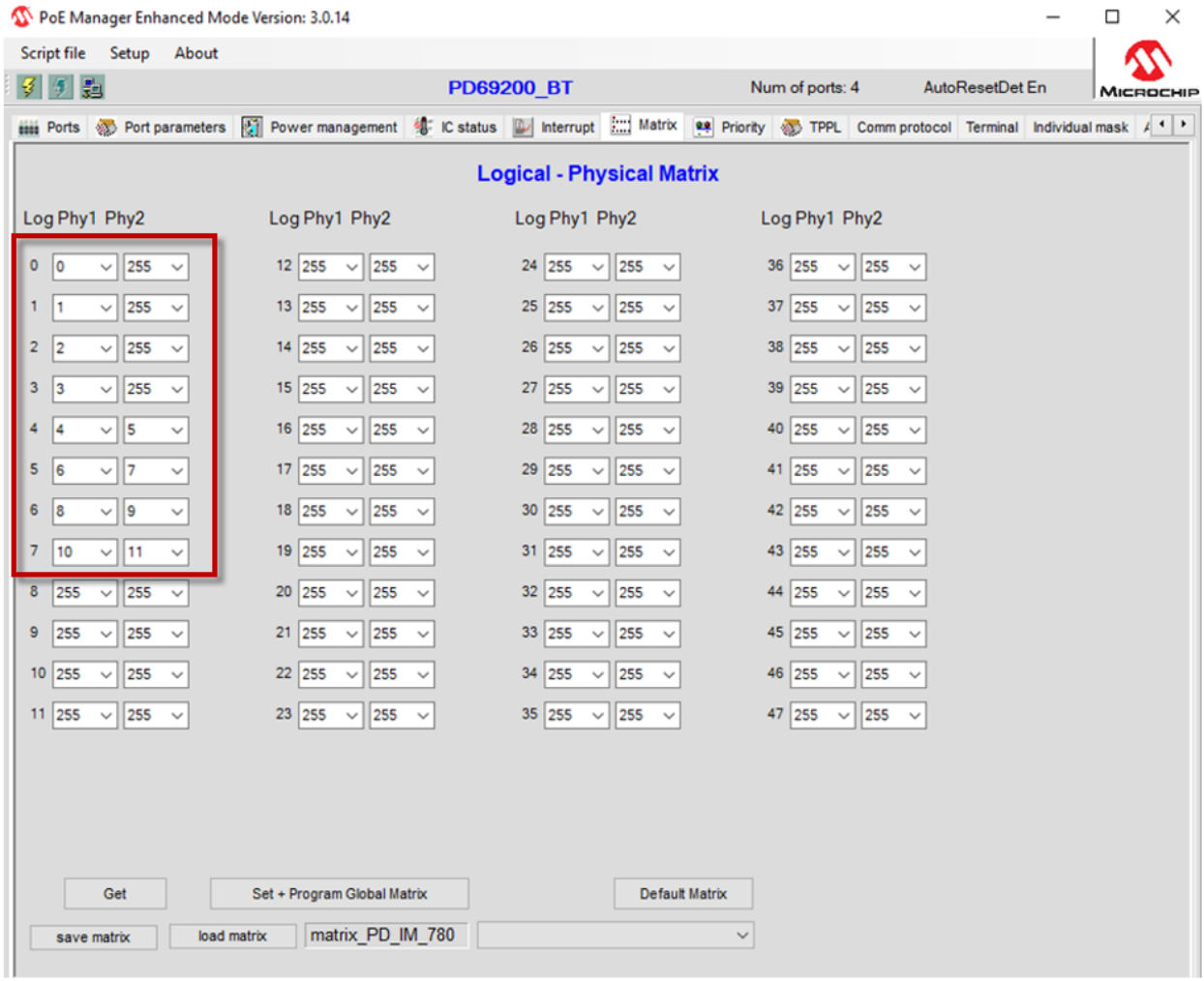
The following instructions describe how to define a 4-pair port using Microchip's GUI or communication protocol commands by using direct UART or I^2C commands to the PD692x0 device, according to the communication protocol.

3.3.1 Set Temporary Matrix

Firmware (without the boot section), GUI, and API are available on Microchip’s Software Library.

Set the port matrix in the **Matrix** tab on the GUI. Set port matrix to program the physical ports with respect to the logical numbering. Ensure that no physical port is set to two separate logical ports. The following figure shows an example, where ports 0, 1, 2, and 3 are set as 2-pair ports utilizing physical ports 0, 1, 2, and 3. Ports 4–8 are set as 4-pair ports utilizing physical ports 4+5, 6+7, 8+9, 10+11.

Figure 3-6. Set Temporary Matrix via GUI



You can set the matrix by using direct I²C or UART commands `Set temporary Matrix` command, as listed in the following table. For detailed description about how to set the matrix, see the *PD692x0 Serial Communication Protocol User Guide* available on Microchip's Software Library.

Table 3-2. Set Temporary Matrix via I²C or UART

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x05	0x43	Val	Val	Val	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command		Channel	Tmp Matrix	CH Num	Physical Number A	Physical Number B	N	N	N	N	N	N

3.3.2 Program Temporary Matrix as Active Matrix

The matrix is not loaded as the working matrix until it is set as the active matrix. To program the temporary matrix as the active matrix, press **Set+Program Global Matrix** in the **Matrix** tab on the GUI or use the `Program Global Matrix` command. This is shown in the following figure and table.

Figure 3-7. Load Temporary Matrix via GUI

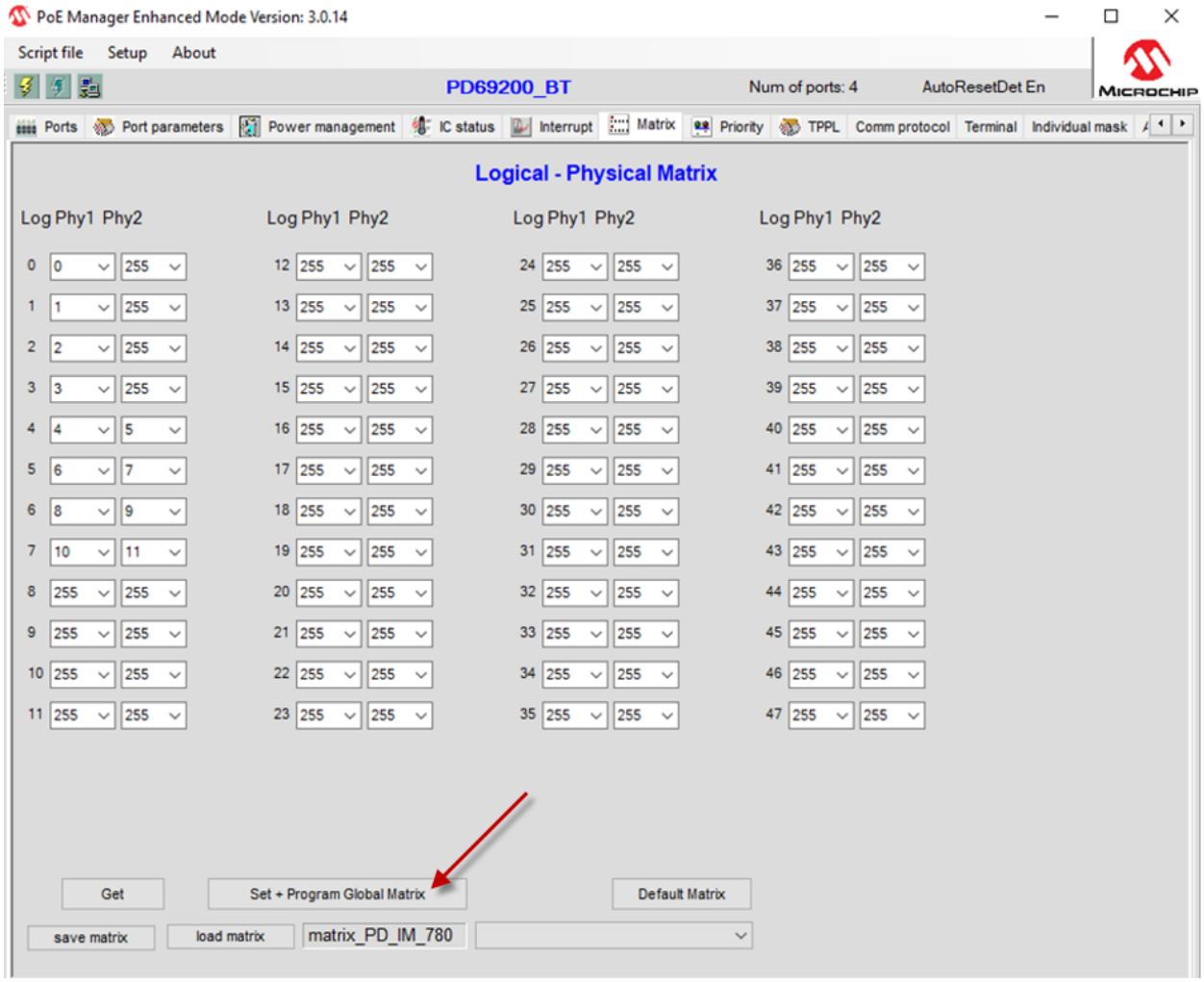


Table 3-3. Load Temporary Matrix via I²C or UART (Program Global Matrix Command)

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x07	0x43	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command		Global	Tmp Matrix	N	N	N	N	N	N	N	N	N

This command causes temporary matrix values to be copied into the active working matrix. Upon completion of this command and successful matrix validation, the active matrix is updated, PD692x0 software is restarted, and the status of PoE ports is refreshed according to the new matrix. During this flow, ports are disconnected.

3.3.3 Set Port Power Level

To set the port power level, use the **Port Parameter** tab on the GUI or use the `Set BT port Parameters` command. This is shown in the following figure and table. For details about each field, see the *PD692x0 Serial Communication Protocol User Guide* available on Microchip's Software Library.

Figure 3-8. Set Power Levels via GUI

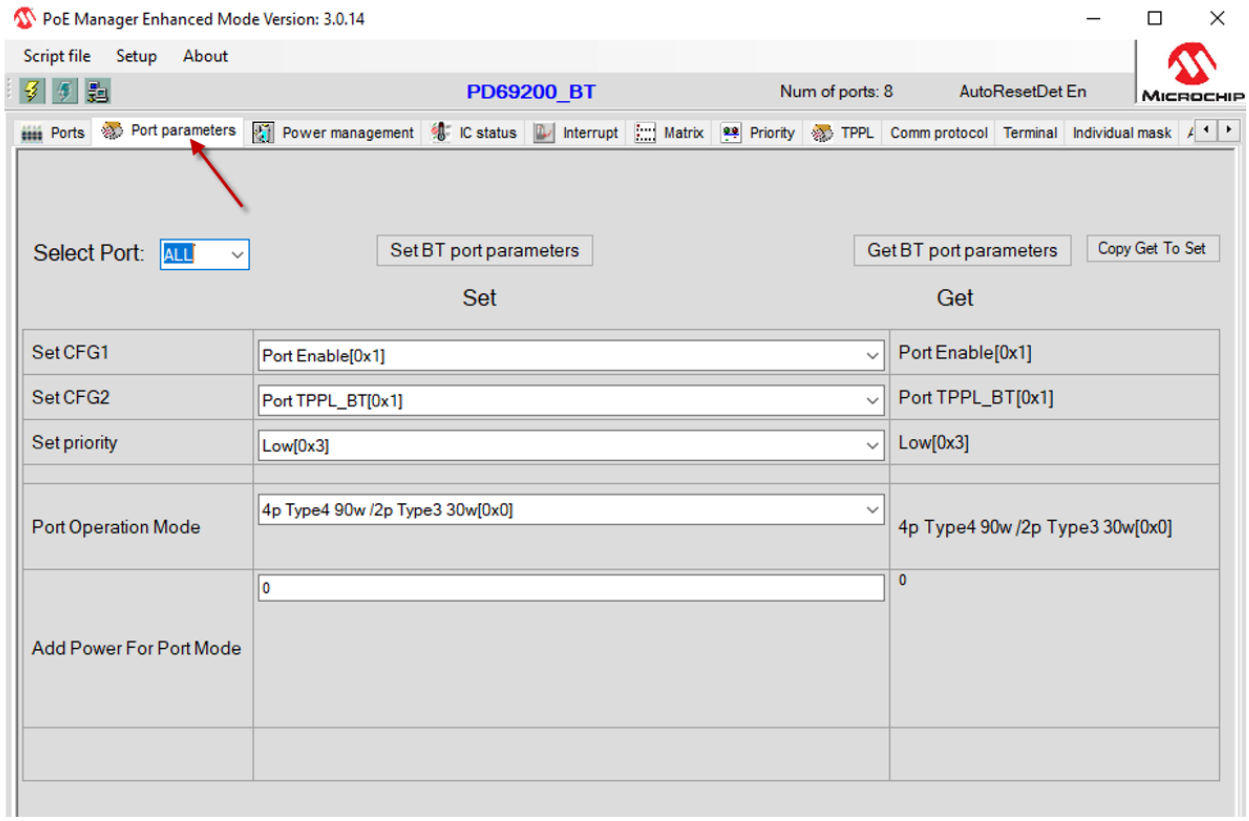


Table 3-4. Set Power Levels via I²C or UART (Set BT Port Parameters Command)

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x05	0xC0	Val	Val	Val	Val	Val	0x4E	0x4E	0x4E	0x4E
Command	—	Channel	BT Port Config1	Port Num	Port Mode CFG1	Port Mode CFG2	Port Oper-ation Mode	Add Power for Port Mode	Priority	N	N	N

This command can set various configuration parameters of a single port or apply the configuration to all system ports.

The command can enable/disable port operation, enable/disable legacy capacitor support, set the power limit, set the priority, and set the PM mode of the BT port.

3.3.4 Save System Settings

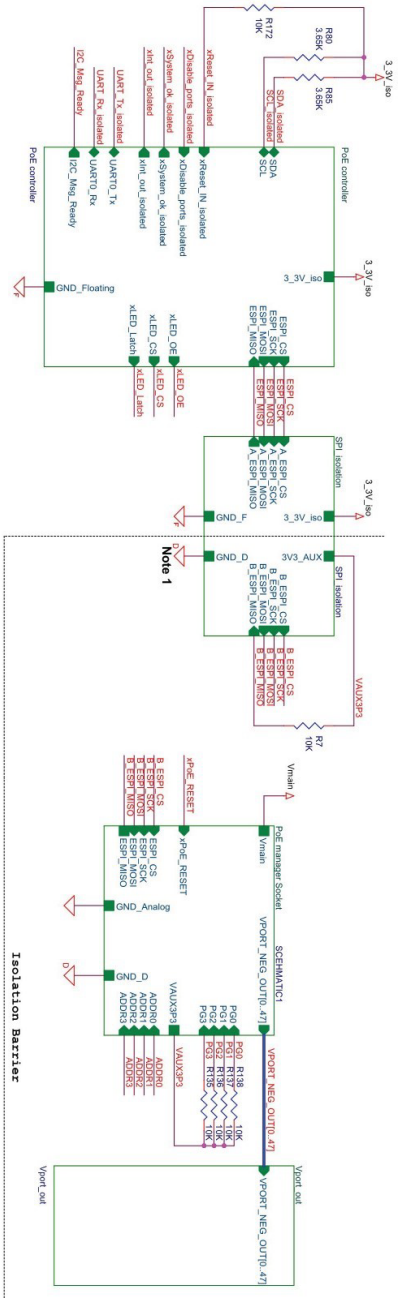
This command saves the current user value to the non-volatile memory, and the user value turns default after any reset. For details about each field, see the *PD692x0 Serial Communication Protocol User Guide* available in the Microchip Software Library.

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x01	##	0x06	0x0F	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Program	—	E2	SaveConfig	N	N	N	N	N	N	N	N	N

4. Schematics

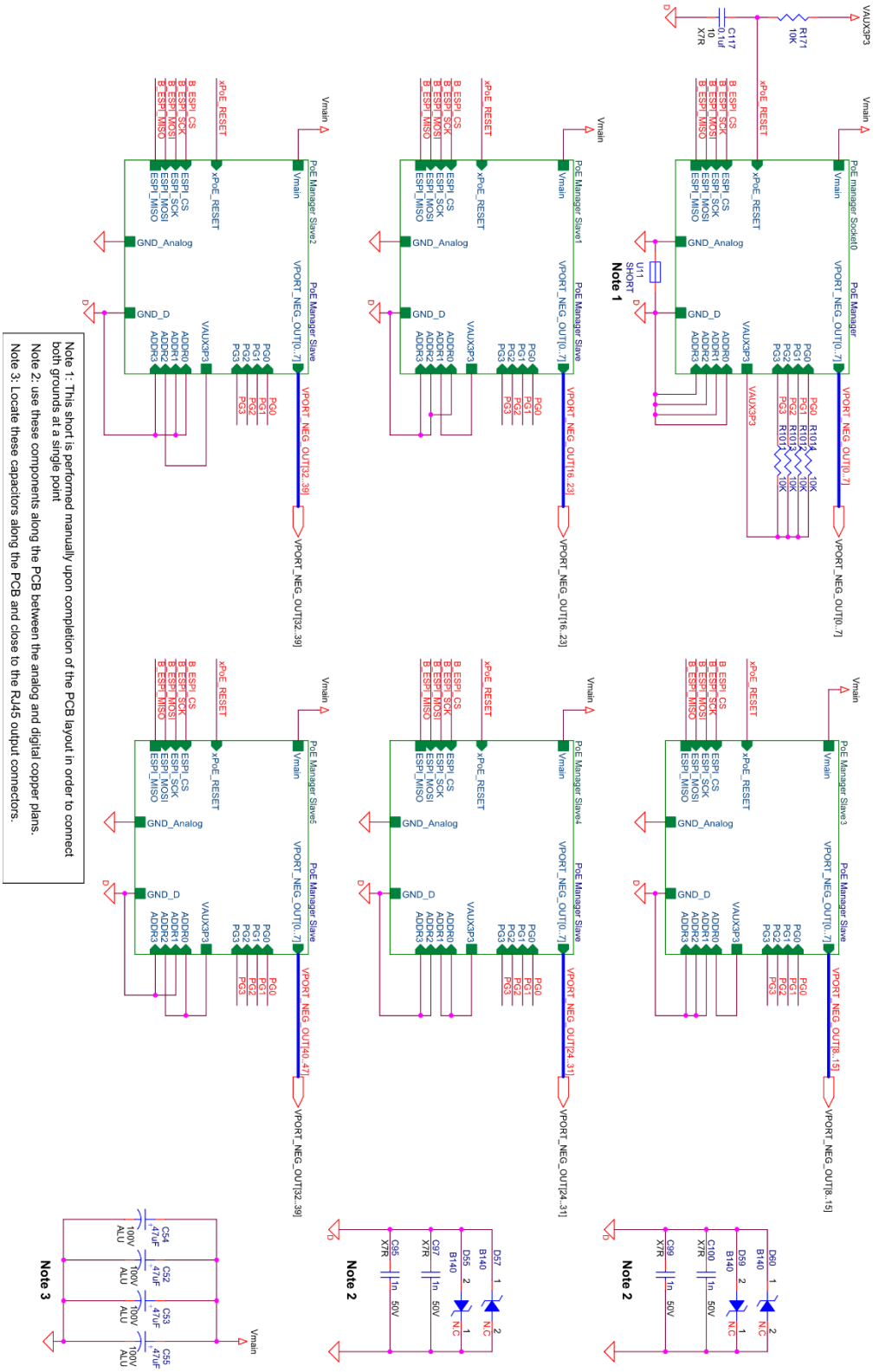
The following section shows the detailed device-level schematic and BOM of a 48-physical port system based on six PD69208 managers and a single PD69200, PD69210, or PD69220 controller. These 48 physical ports may be configured as 48 2-pair ports or 24 4-pair ports. This schematic meets 1 kV basic surge requires, as defined in EN 61000-4-5:2014. For a higher level of surge protection, such as ITU-T k.21-2018, request *AN3378 Surge Protection 8-Port PSE PoE Manager* PD69208T4/M/4T4.

Figure 4-1. 48-Port System Main Blocks



The following figure shows the six PD69208 PoE manager circuitries. For descriptions and more information, see 6.3.4. VMAIN Capacitors.

Figure 4-2. 48-Port PoE Manager Blocks



The following figure shows the PD69210 PoE controller circuitry. In an actual circuit design, either the PD69220/ PD69200 controller block or the PD69210 controller block is used. PD69210 is recommended for all new designs. PD69200 and PD69220 are available for existing designs.

Figure 4-3. PD69210 Controller Circuitry

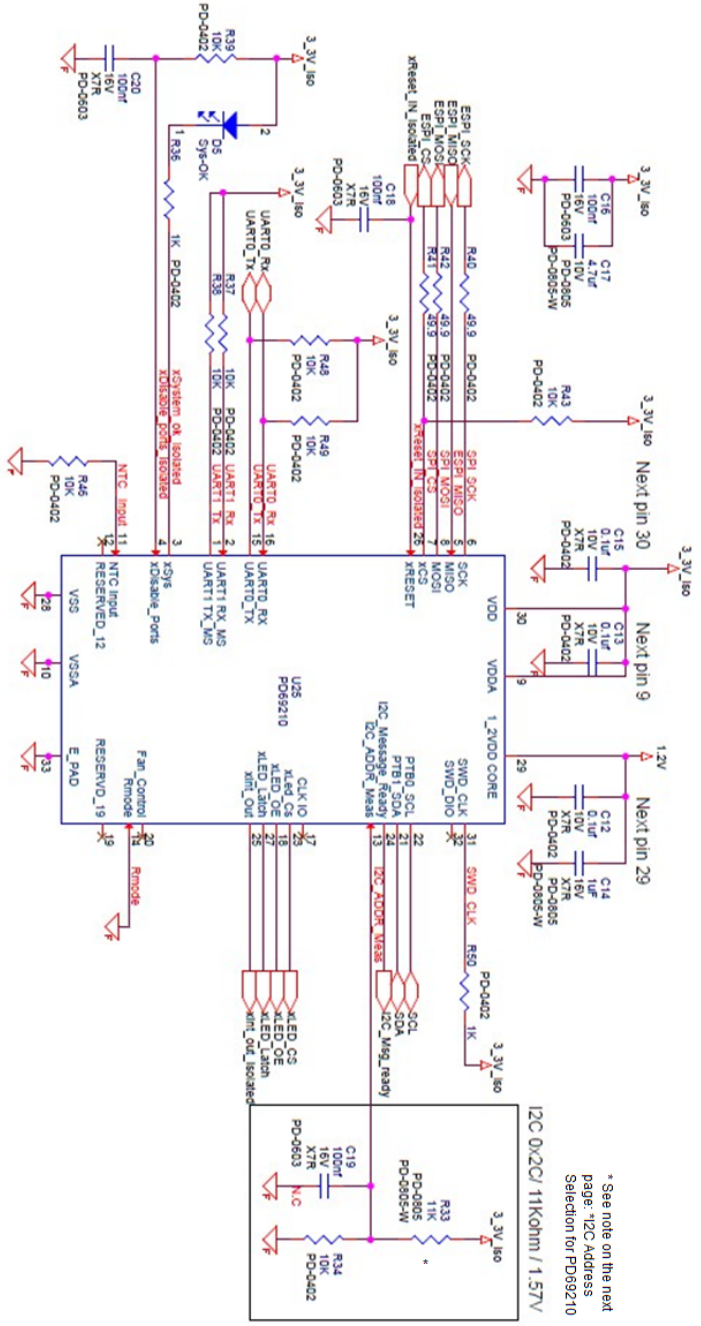


Figure 4-4. I²C Address Selection for PD69210

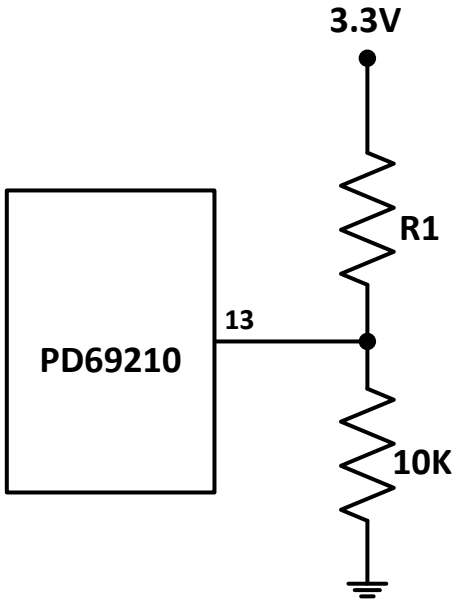


Table 4-1. I²C Address Selection for PD69210

I²C Address Hexadecimal	R1–KΩ (1%)
UART	N.C.
0×4	147
0×8	86.6
0×C	57.6
0×10	43.2
0×14	34
0×18	26.7
0×1C	22.1
0×20	18.2
0×24	15.4
0×28	13
0×2C	11
0×30	9.31
0×34	7.87
0×38	6.49
0×3C	5.49

The following figure shows the PD69220 and PD69200 PoE controller circuitry. In an actual circuit design, either the PD69220/PD69200 controller block or the PD69210/PD39210 controller block is used. PD69210 is recommended for all new designs. PD69200 and PD69220 are available for existing designs.

Figure 4-5. PD69220 and PD69200 PoE Controller Circuitry

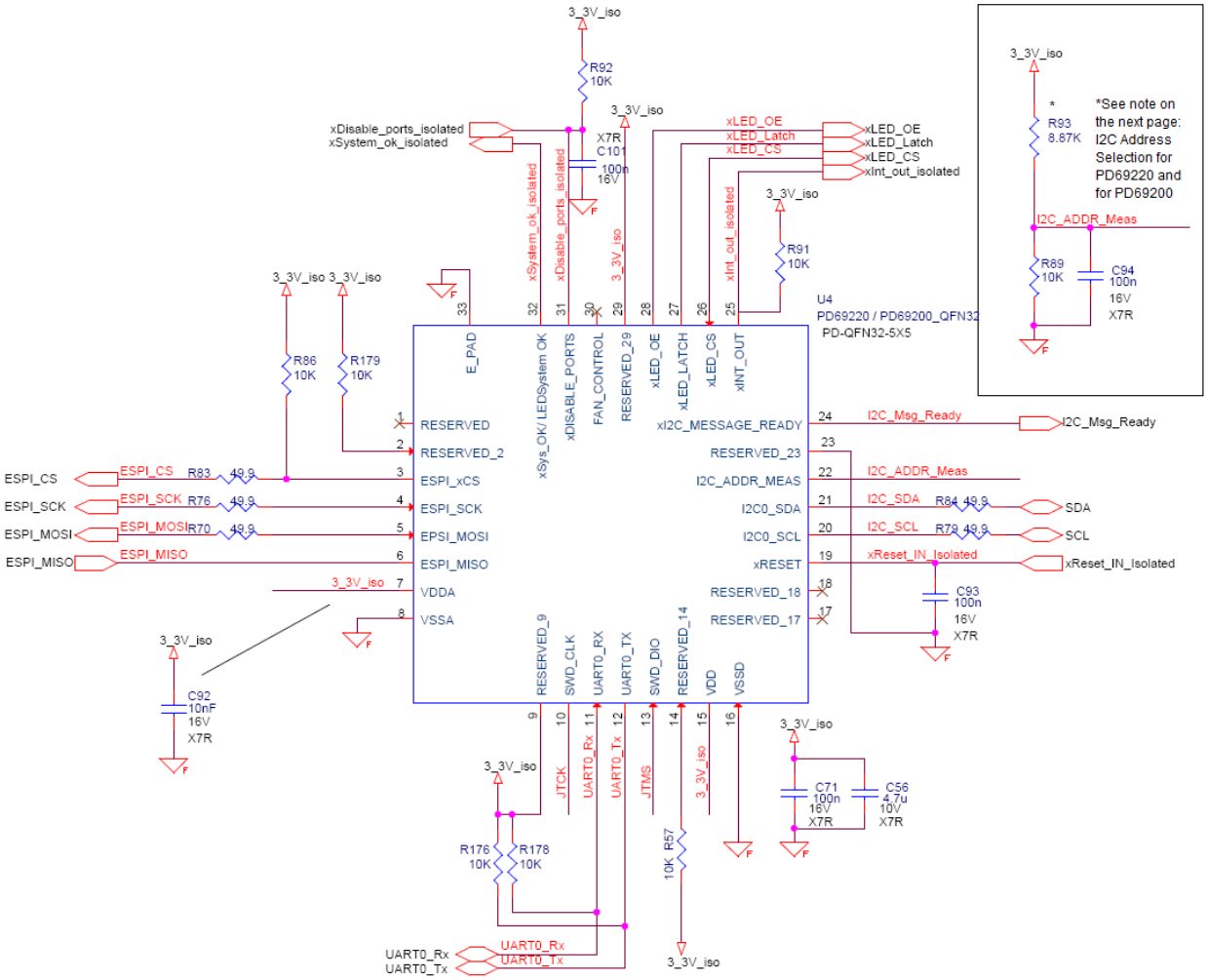


Figure 4-6. I²C Address Selection for PD69200 and PD69220

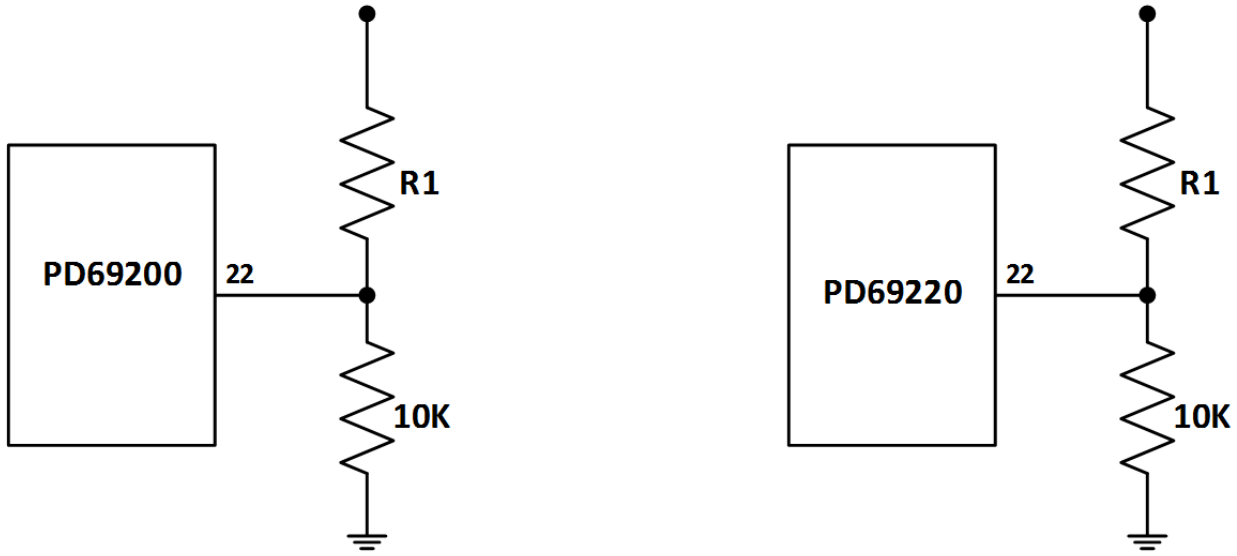
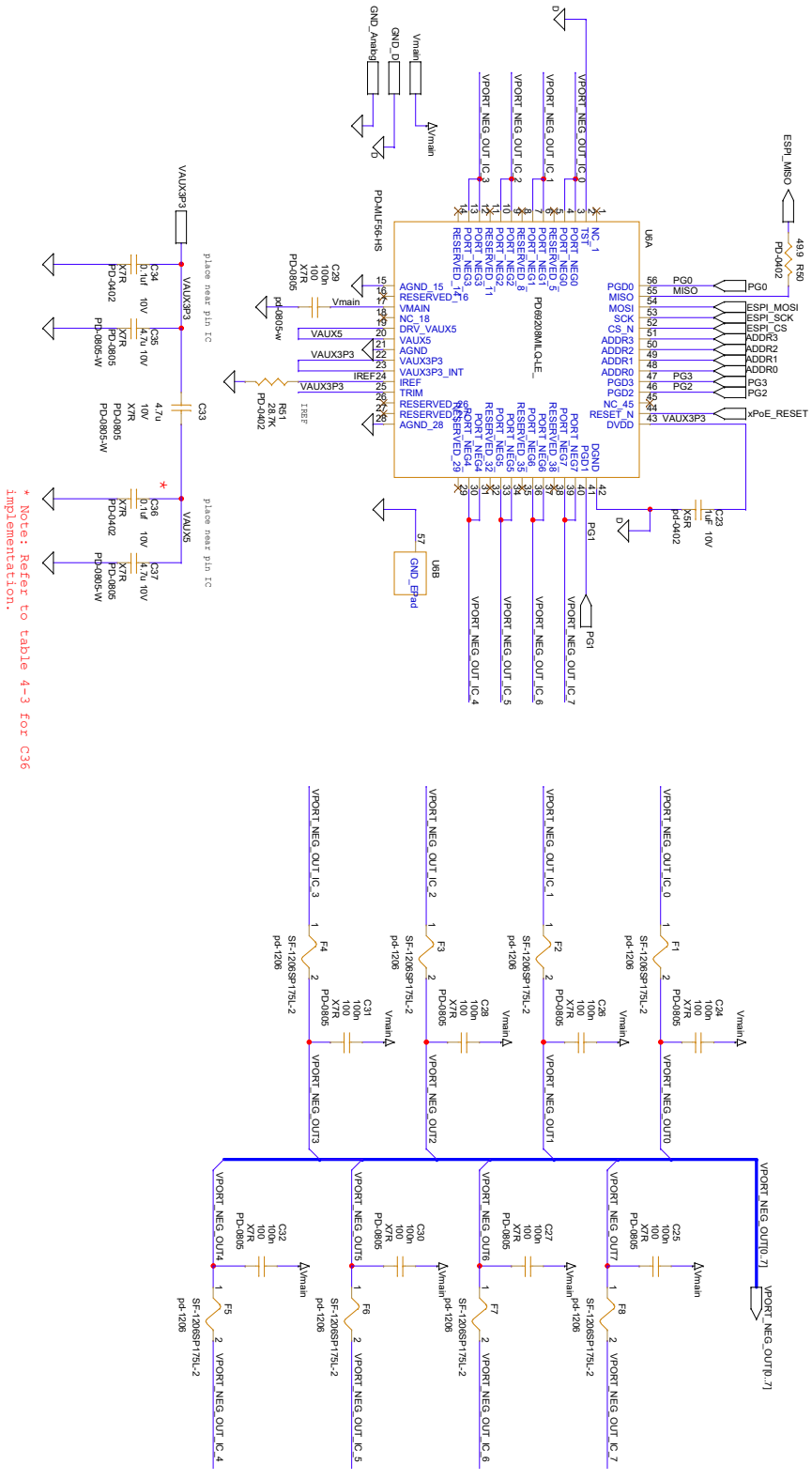


Table 4-2. I²C Address Selection for PD69200 and PD69220

I²C Address Hexadecimal	R1–KΩ (1%)	
	PD69200	PD69220
UART	N.C.	N.C.
0×4	97.6	147
0×8	53.6	86.6
0×C	35.7	57.6
0×10	25.5	43.2
0×14	19.1	34
0×18	14.7	26.7
0×1C	11.3	22.1
0×20	8.87	18.2
0×24	6.81	15.4
0×28	5.23	13
0×2C	3.92	11
0×30	2.80	9.31
0×34	1.87	7.87
0×38	1.02	6.49
0×3C	0.324	5.49

The following figure shows the PD69208 circuitry for PoE manager number 0. For descriptions and more information, see 1.5. PoE Manager Circuitry.

Figure 4-7. PD69208 PoE Manager Circuitry



The following table lists the V_{AUX5} connection details.

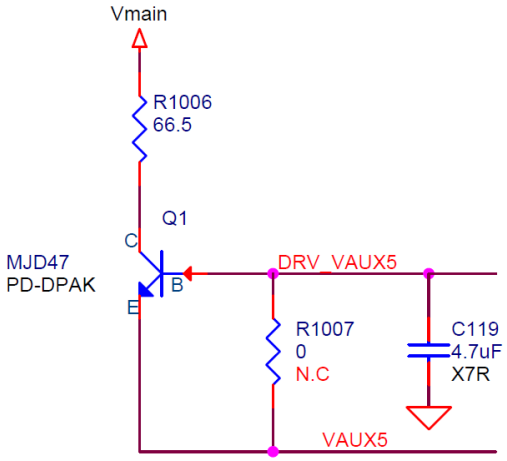
Table 4-3. V_{AUX5} Connection

Revision	Allowed Component	C36	R52
V2R4	C36 or R52	0.1 µF	17.4 kΩ
V2R5	R52	Not allowed	17.4 kΩ
V2R6	C36 or R52	0.1 µF	17.4 kΩ

Note: For more information concerning Device Revisions V2R4, V2R5, and V2R6, see Implications of Adding TowerJazz 5 as Alternative Manufacture Site.

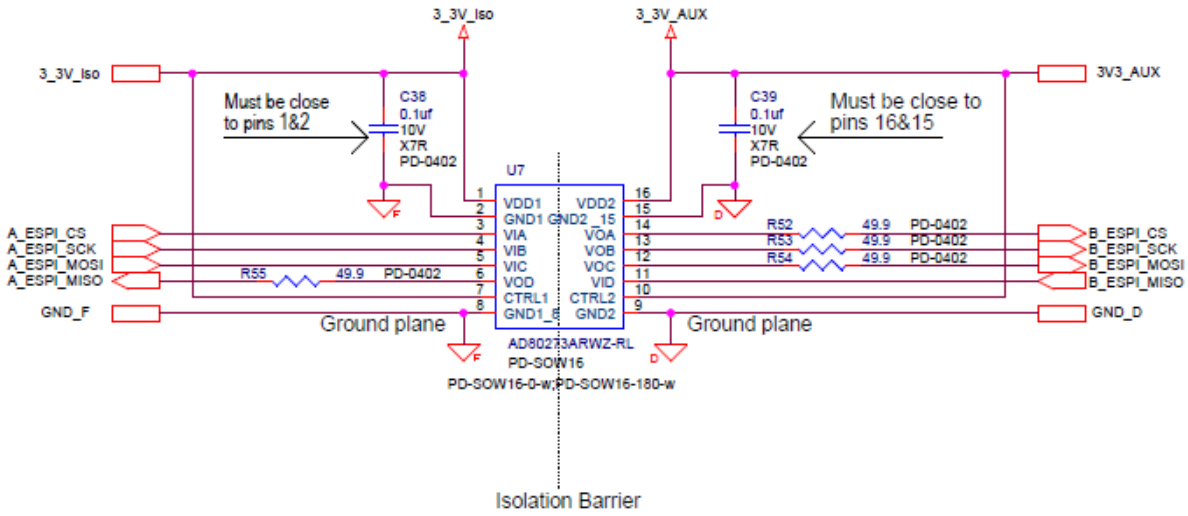
The following figure shows the optional boost transistor to the 5 VDC regulator. For descriptions and more information, see 5 V_{DC} and 3.3 V_{DC} Regulators.

Figure 4-8. (Optional) Boost Transistor to the 5 V_{DC} Regulator



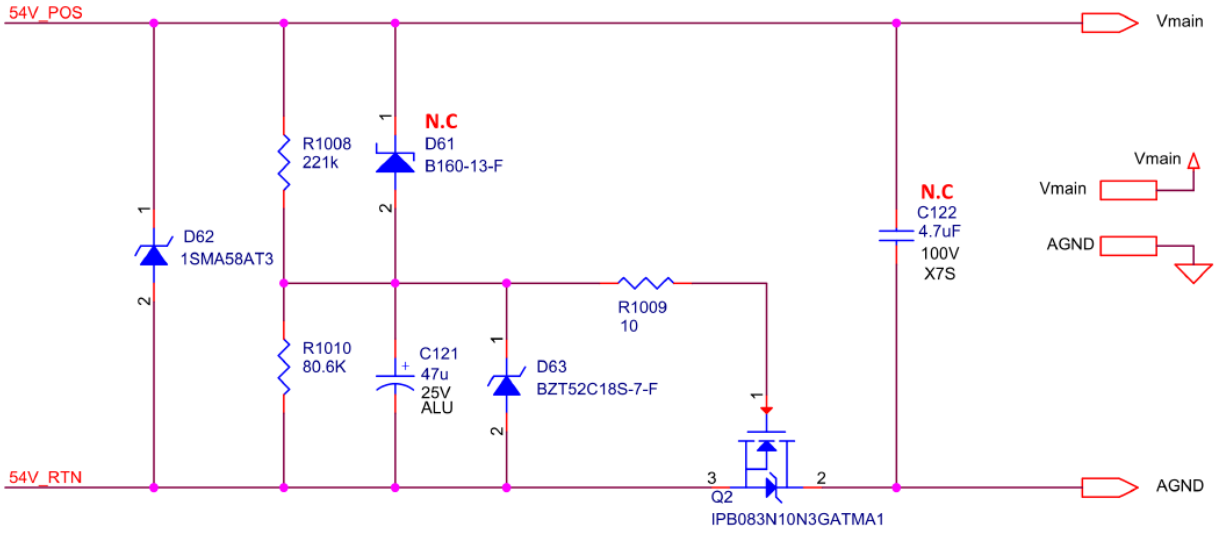
The following figure shows the digital isolator. For descriptions and more information, see 1.1. Communication Interfaces.

Figure 4-9. Digital Isolator



The following figure shows the hot-swap circuit. For descriptions and more information, see 1.2.3. Hot-Swap Circuit.

Figure 4-10. Hot-Swap Circuit



5. Bill of Materials for 48-Port PoE System

The following tables list the bill of materials for a 48-port PoE system.

Table 5-1. 48-Port System Main Blocks Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	R80 R85	3.65 KΩ	3.65K 62.5 mW 1% 0402	Yageo	RC0402FR-073K65L
6	R7 R135 R136 R137 R138 R172	10 KΩ	10K 1% 62.5 mW 0402	Vishay	CRCW040210K0FKED

Table 5-2. 48-Port PoE Manager Blocks Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C52 C53 C54 C55	47 µF	Capacitor ALU 47 µF 100V 20% 8x 11.5 105 °C	Rubycon	100PX47MT7 8X11.5
4	C95 C97 C99 C100	1 nF	Capacitor X7R, 1 nF 50V 10% 0402	Murata	GRM155R71H102KA01D
4	D55 D57 D59 D60	B140	Schottky diode 40V 1A SMAT	Diodes Inc.	B140
4	R1111 R1112 R1113 R1114	10 KΩ	10K 1% 62.5 mW 0402	Vishay	CRCW040210K0FKED

Table 5-3. PD69210 PoE Controller Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	U25	PD69210	PoE PSE controller	Microchip	PD69210-gggg[1]
10	R34 R37 R38 R39 R43 R45 R46 R47 R48 R49	10 KΩ	10K 1% 62.5 mW 0402	Bourns	CR0402-FX-1002GLF
2	R36[2] R50	1 KΩ	1K 1% 62.5 mW 0402	Bourns	CR0402-FX-1001GLF
3	R40 R41 R42	49.9Ω	49.9R 1% 62.5 mW 0402	Bourns	CR0402-FX-49R9GLF
1	R33	11 KΩ	11K 125 mW 1% 0805	Samsung	RC2012F1102CS
3	C12 C13 C15	0.1 µF	CAP CER 0.1 µF 10V X7R 10% 0402 SMT	Nic	NMC0402X7R104K10TRP
1	C14	1 µF/16V	CAPCRM 1 µF 16V 10% 0805X7R SMT	Murata	GRM21BR71C105KA01
1	C17	4.7 µF/10V	CAP CRM 4.7 µF 10V 10% X5R 0805 SMT	Taiyo Yuden	LMK212BJ475KD-T
5	C16 C18 C19 C20 C22	0.1 µF	CAP CRM 100 nF 16V 10% X7R 0603 SMT	Taiyo Yuden	EMK107B7104KA-T
1	D5[2]	Sys-OK	LED SuperYelGrn 100-130o 20-40mcd h=1 0603 SMD	Everlight	19-21-SYGCS530E3TR8

Notes:

1. gggg refers to the firmware version.
2. Optional component.

Table 5-4. PD69220/PD69200 PoE Controller Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C71 C93 C94 C101	100 nF	Capacitor 100 nF 16V 10% X7R 0603	Samsung	CL10B104KO8NNNC
1	C56	4.7 µF	Capacitor 4.7 µF 10V 10% X5R 0805	Taiyo Yuden	LMK212BJ475KD-T
1	C92	10 nF	Capacitor X7R 10 nF 16V 10% 0402	Samsung	CL05B103KO5NCNC
6	R57 R86 R89 R91 R92 R179	10 KΩ	10K 100 mW 1% 0603	Samsung	RC1608F1002CS
2	R176 R178	49.9 KΩ	49.9K 125 mW 1% 0805	Samsung	RC2012F4992CS
5	R70 R76 R83 R79 R84	49.9Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L
1	R93	8.87 KΩ	8.87K 125 mW 1% 0805	Yageo	RC0805FR-078K87-L
1	U4	PD69220 PD69200	PoE PSE controller	Microchip	PD69220X-gggg[1] PD69200X-gggg[1]

Note:

1. gggg refers to the firmware version.

Table 5-5. PD69208 PoE Manager Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
8	C24–C32	100 nF	Capacitor 100 nF 100V 10% X7R 0805	Samsung	CL21B104KCFSFNE
3	C33 C35 C37	4.7 µF	Capacitor 4.7 µF 10V 10% X5R 0805	Murata	GRM219R61A475KE19D
2	C34 C36	0.1 µF	Capacitor 0.1 µF 10V X7R 10% 0402	Murata	GRM155R71A104KA01J
1	C23	1.0 µF	Capacitor 1.0 µF 10V X5R 10% 0402	Panasonic	ECJ-0EB1A105M
1	R51	28.7 KΩ	28.7K 125 mW 1% 0805 (For PoH and IEEE® 802.3bt, 99W must be 0.1%)	Vishay	CRCW080528K7FKEA
1	R52[1]	17.4 KΩ	17.4K, 1%, 62.5 mW 0402	Bourns	CR0402-FX-1742-ELF
1	R50	49.9Ω	49.9R 1% 62.5 mW 0402	Bourns	CR0402-FX-49R9-ELF
1	U6A	PD69208	8-Port PSE PoE Manager SMT	Microchip	PD69208T4/M/PD69204T4
8	F1–F8	1.75A	Time Lag Ceramic Cavity Laminate 1.75 A 63 V_{DC} 1206 SMD Fuse	Bourns	SF-1206SP175L-2-A9[2]

Notes:

1. See Implications of Adding TowerJazz 5 as Alternative Manufacture Site.
2. Required for systems with > 250 VA certified to IEC/UL/EN 62368-1 Ed.2. May not be required for systems < 250 VA per IEC/UL/EN 62368-1 Ed.2 or system with any power level certified per IEC/UL/EN 62368-1 Ed.3. See the *AN3527 Compliance to Limited Power Source Requirements Application Note*.

Table 5-6. (Optional) Boost Transistor to the 5 V_{DC} Regulator

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	Q1	1A 250V V_{CEO}	DPAK—High Voltage Power Transistor	ON Semi	MJD47
1	C119	4.7 µF	Capacitor 4.7 µF 10V 10% X5R 0805	Taiyo Yuden	LMK212B7475KG-T
1	R1006	66.5Ω	5% 125 mW 0805	Yageo	GRM155R71A104KA01J
1	R1007	0Ω	0402	Yageo	RC0402JR-070RL

Table 5-7. Digital Isolator Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	C38 C39	0.1 µF	Capacitor 0.1 µF 10V X7R 10% 0402	Murata	GRM155R71A104KA01J
4	R52 R53 R54 R55	49.9Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L
1	U7	AD80273A RWZ	IC digital isolator SO16	Analog Devices	AD80273ARWZ-RL[1]

Note:

1. Special part number for Microchip PoE applications; preferential pricing for Microchip customers.

Table 5-8. Hot-Swap Circuit Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	Q2	IPB083N10N3	MOSFET N-CH 100V 80A 8.3 mΩ TO263-3	Infineon	IPB083N10N3GATMA1
1	C121	47 µF	Capacitor ALU 47 µF 25V 20% SMT	SUNCON	25CE47FS
1	R1008	221 KΩ	221K 1% 1/10W 0603	Yageo	RC0603FR-07221KL
1	R1010	80.6 KΩ	80.6K 125 mW 1% 0603	ASJ	CR16-8062FL
1	R1009	10Ω	10.0R 1% 62.5 mW 0402	Yageo	RC0402FR-0710R0L
1	D63	BZT52C18S-7-F	Diode Zener, 18V 200 mW SOD323	Diodes Inc.	BZT52C18S-7-F
1	D62	1SMA58AT3	DIO TVS 58V 40A SRG400WPK SMA SMT	ON Semiconductor	1SMA58AT3

6. Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a 48-port PoE system, based on Microchip's PD69208 8-channel PoE manager.

6.1 Isolation and Termination

According to PoE standards, certain isolation requirements must be met in all PoE equipments. In addition, EMI limitations must be considered, as specified in the FCC and European EN regulations. These requirements are considered by the PoE switch vendors while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met because of the unique combination of data and power circuitries.

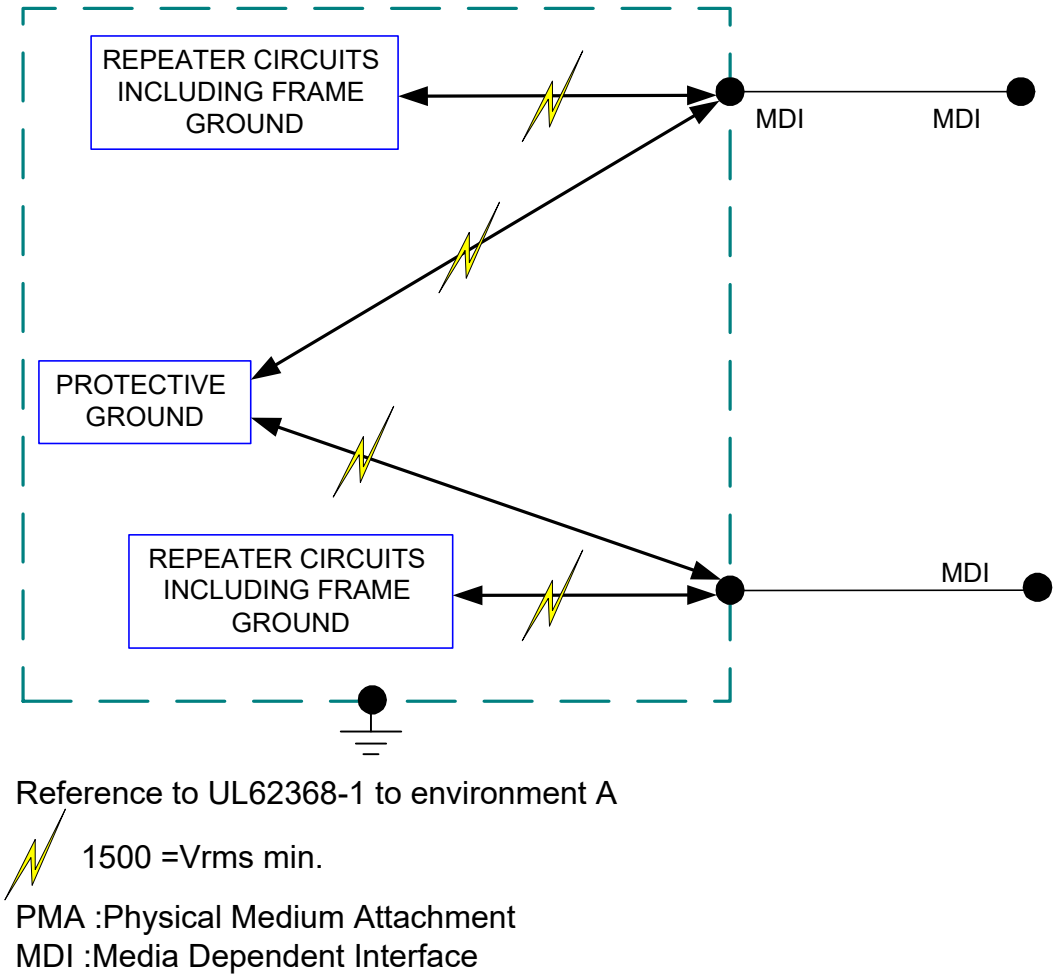
The following sections define the requirements and provide recommendations for their implementation to assist designers in meeting those requirements, while also integrating Microchip's PoE chipset over mother boards or Daughter Boards (DBs).

6.1.1 Isolation

As specified in the IEEE PoE standards, 1500 V_{RMS} isolation is required between the switch's main board circuitry (including protective and frame ground) and the Media Dependent Interface (MDI).

The following figure shows the overall isolation requirements.

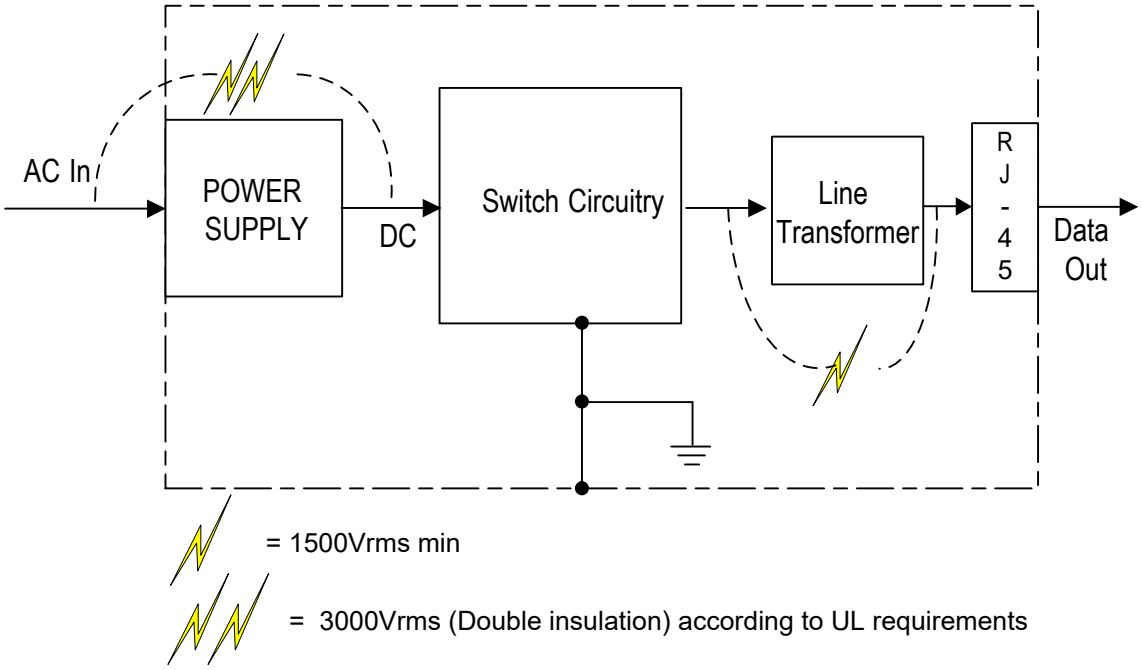
Figure 6-1. Isolation Requirements



6.1.2 High-Voltage Isolation

For a switch with no PoE circuitry, isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers, as shown in the following figure.

Figure 6-2. Standard Switch Circuitry

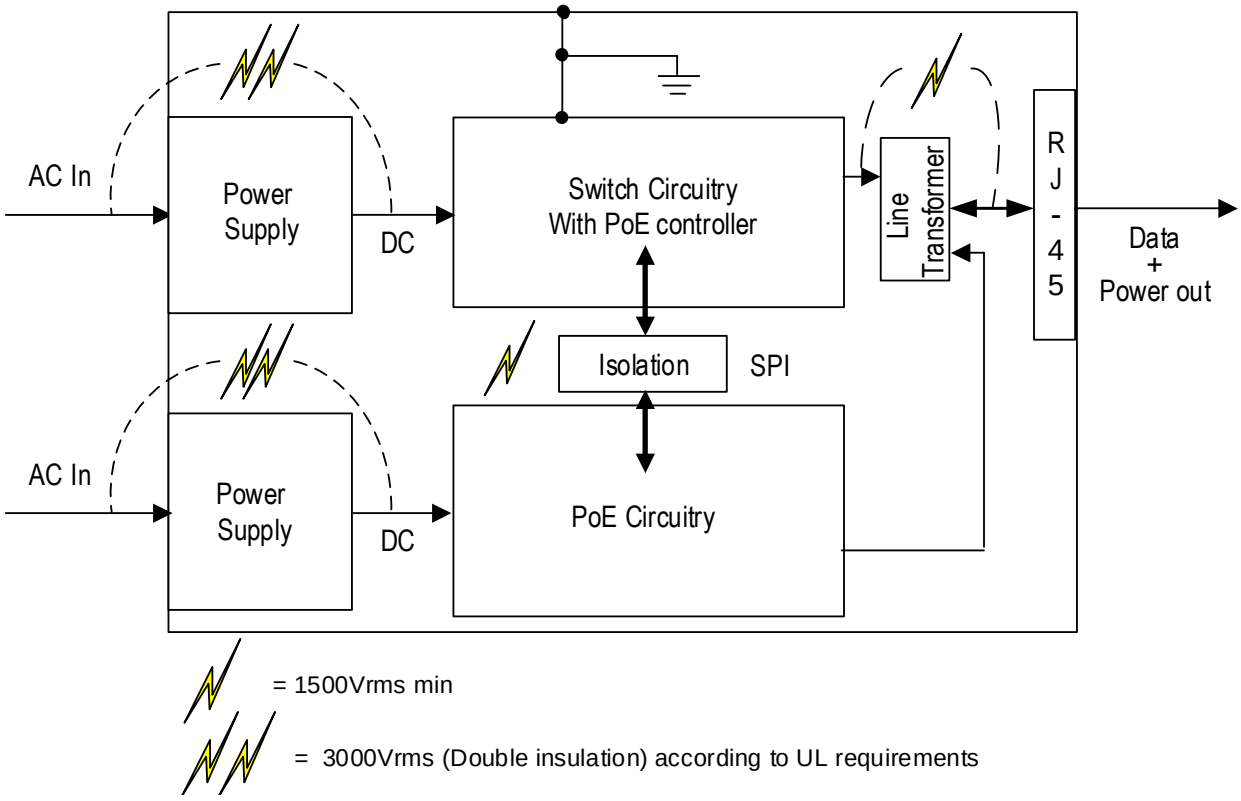


When integrating PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless the power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation if the PoE ground or DC input is connected to the switch's circuitry/ground.

To comply with these isolation requirements, the PoE managers must be isolated in regard to all other switch circuitries. Use one of the following two methods.

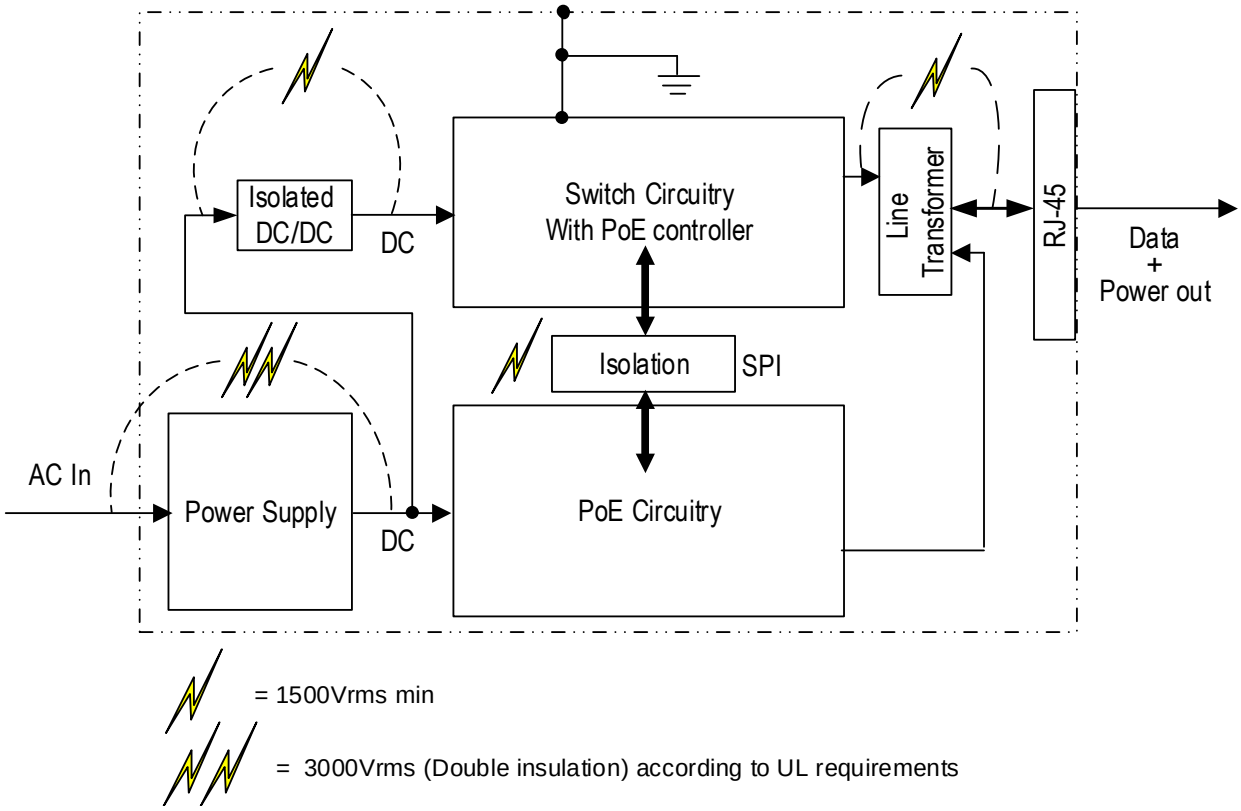
Method 1: Use a separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry, as shown in the following figure.

Figure 6-3. Switch Circuitry with Two DC Source



Method 2: Use a single DC input (separate power supplies) for both the switch and PoE circuit, as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry, as shown in the following figure.

Figure 6-4. Switch Circuitry with a Single DC Source

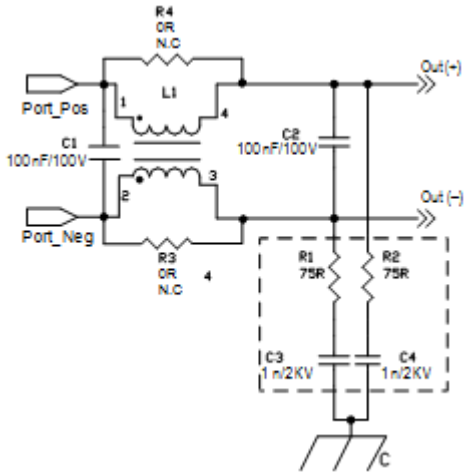


To maintain 1500 V_{RMS} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

6.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry, as shown in the following figure.

Figure 6-5. Recommended EMI Filter



Note: In most PoE systems, it is recommended to use 0Ω resistors for R1 and R2. However, certain systems may benefit from 75Ω resistors. Filtering provisions must be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

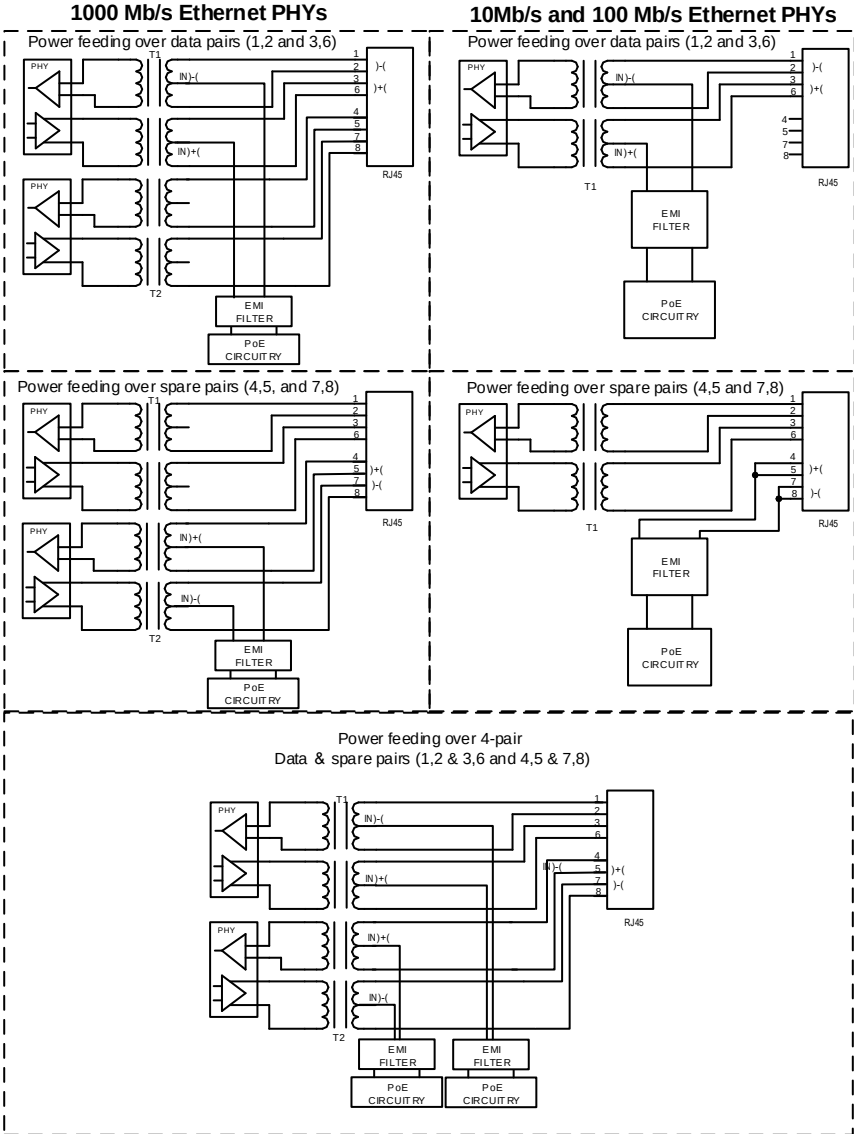
A circuitry for the recommended filter includes the following.

- A common mode choke for conducted EMI performances (such as, ICE CS01 series).
- Output differential cap filter for radiated EMI performances.
- Y-capacitive/resistive network to chassis as each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note: For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs, the spare pairs, or both the data and spare pairs. The following figure shows all the methods where an MDI-X (or Auto MDI-X) connection is associated with the switch.

Figure 6-6. Output Ports Design Details



6.1.4 Isolating Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 V_{RMS} isolation between PoE voltages and frame ground (EGND). The RJ45 jack assemblies have a metal cover of 80 mils that almost reaches to the PCB surface. Maintain an 80 mils traces clearance between EGND traces for the RJ45 modular jack assembly metal covering and adjacent circuit paths and

components. To prevent 1500 V_{RMS} isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ45 connector assemblies.

PoE technology involves voltages as high as 57 V_{DC}. Therefore, plan adjacent traces for 100 V_{DC} operational creepage. Operational creepage must be maintained to prevent breakdown between traces carrying these potentials.

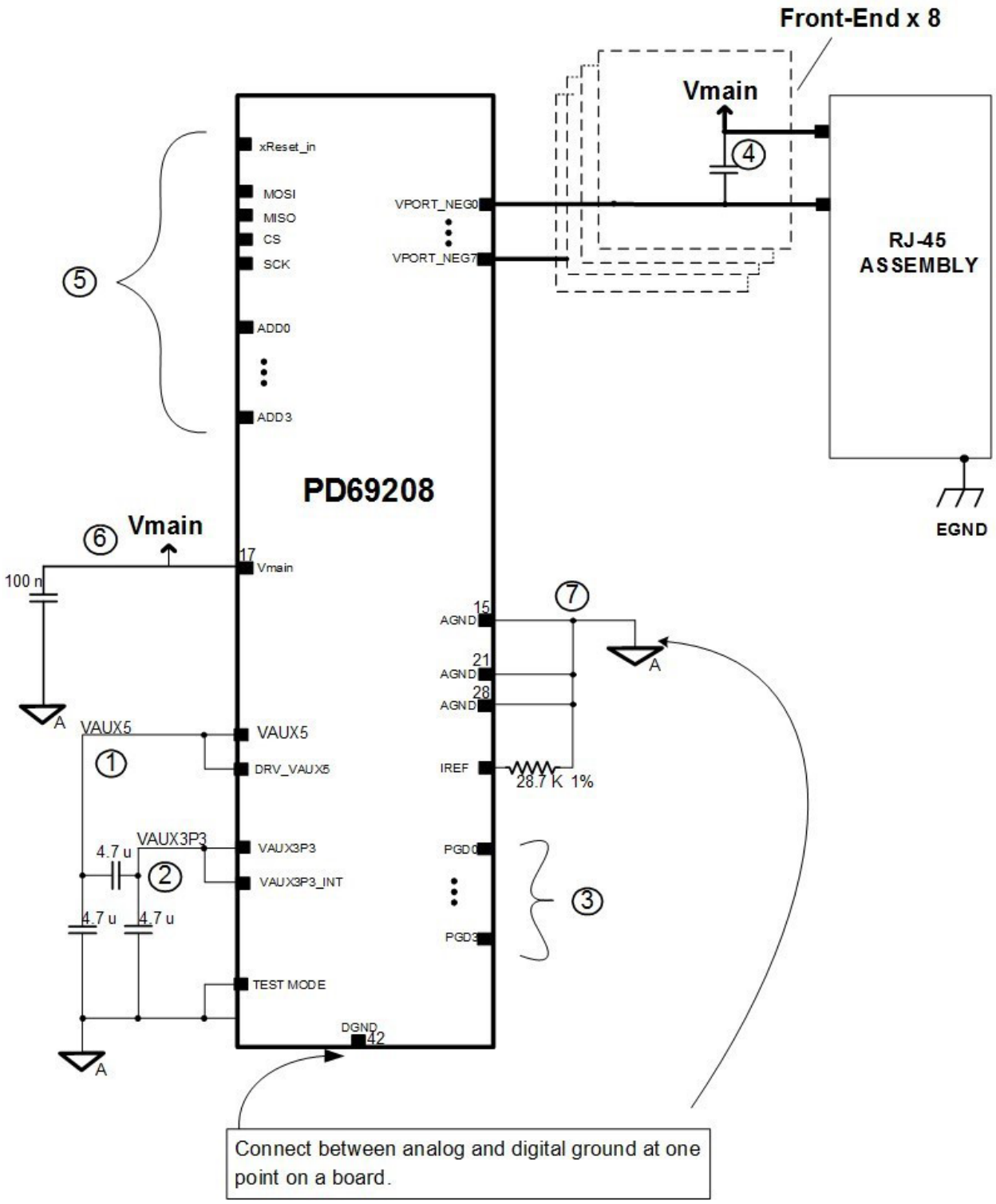
6.2 Guidelines

Microchip's PD69208 PoE manager is designed to simplify the integration of PoE circuitry into switches based on the IEEE PoE standards. The pinout arrangement has been configured for optimal PCB routing.

The following figure shows the various circuits and elements surrounding the PD69208 PoE manager. This block diagram includes the following peripheral elements, identified by numbers.

1. 5V voltage source (V_{AUX5})
2. 3.3V voltage source (V_{AUX3P3})
3. Power good inputs
4. Output capacitor used for filtering
5. ESPI bus, ESPI address lines
6. V_{MAIN} input
7. Analog ground/AGND

Figure 6-7. Component Identification for PD69208 Circuitry

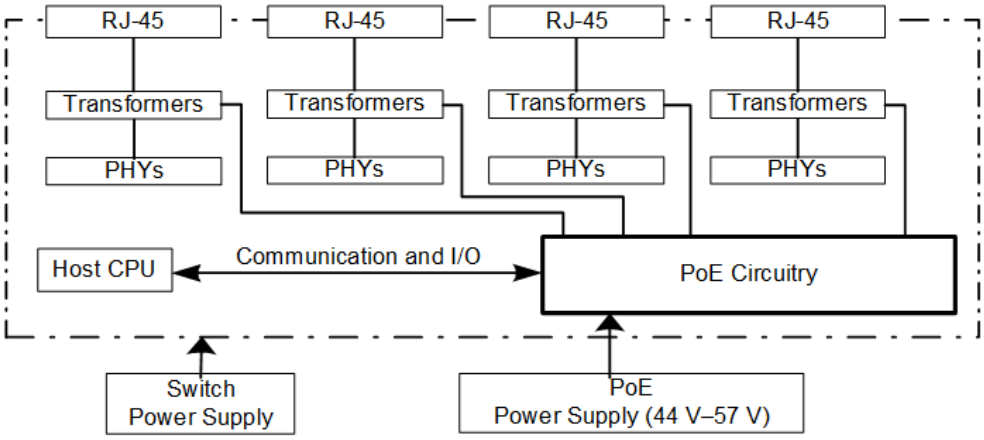


Note: The V_{AUX5} supply may include an external transistor connected to pin 20, to increase current drive for external circuitry. To prevent heat from being transferred to the PD69208 device, place this transistor away from the PoE managers.

6.2.1 Locating PoE Circuitry in a Switch

To minimize the length of the high current traces and the RFI pick-up, place the PoE circuitry as close as possible to the switch's line transformers. The circuit can be fully integrated into the switch's PCB or can be easily placed on top of the switch's using a daughter board. The following figure shows typical integration of the PoE modules inside a switch.

Figure 6-8. PoE Circuitry Inside the Switch



6.2.2 Ground and Power Planes

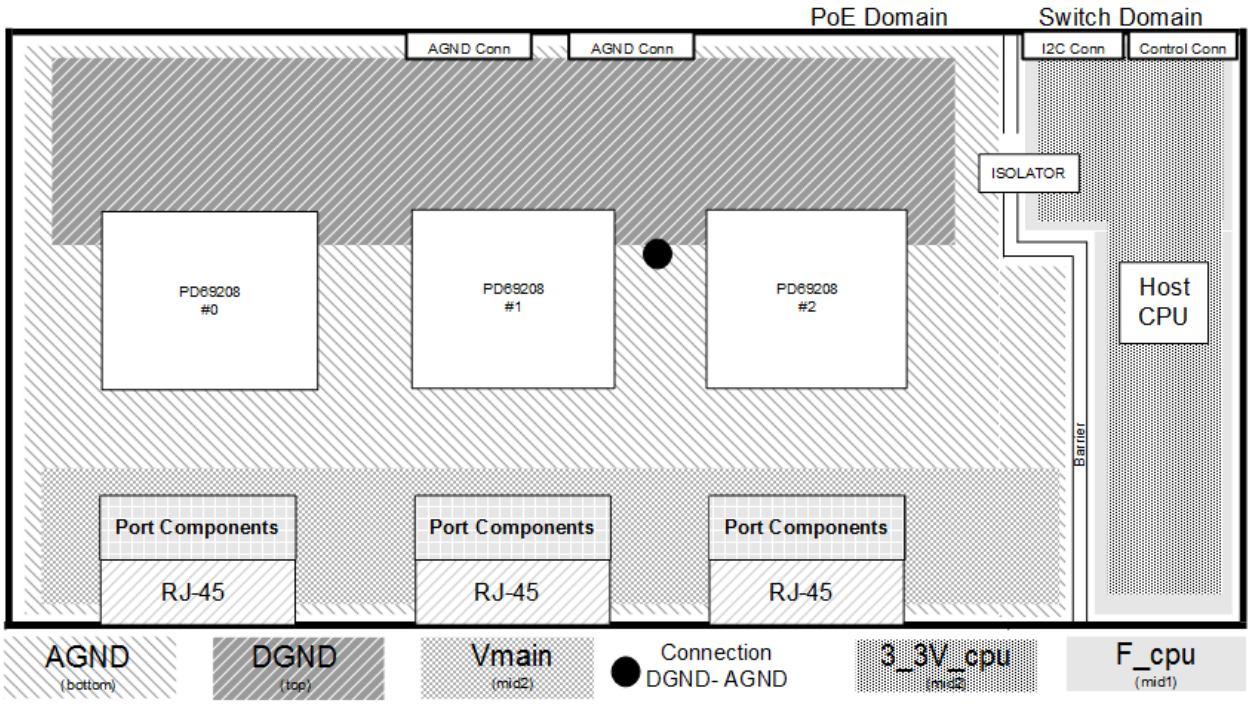
As the PoE solution is a mixed-signal (analog and digital) circuitry, care must be taken when routing the ground and power signals lines.

The reference design assumes a four-layer board such as, top, mid1, mid2, and bottom. The main planes are VMAIN/AGND and DGND.

Ground planes are crucial for proper operation and must be designed in accordance with the following guidelines.

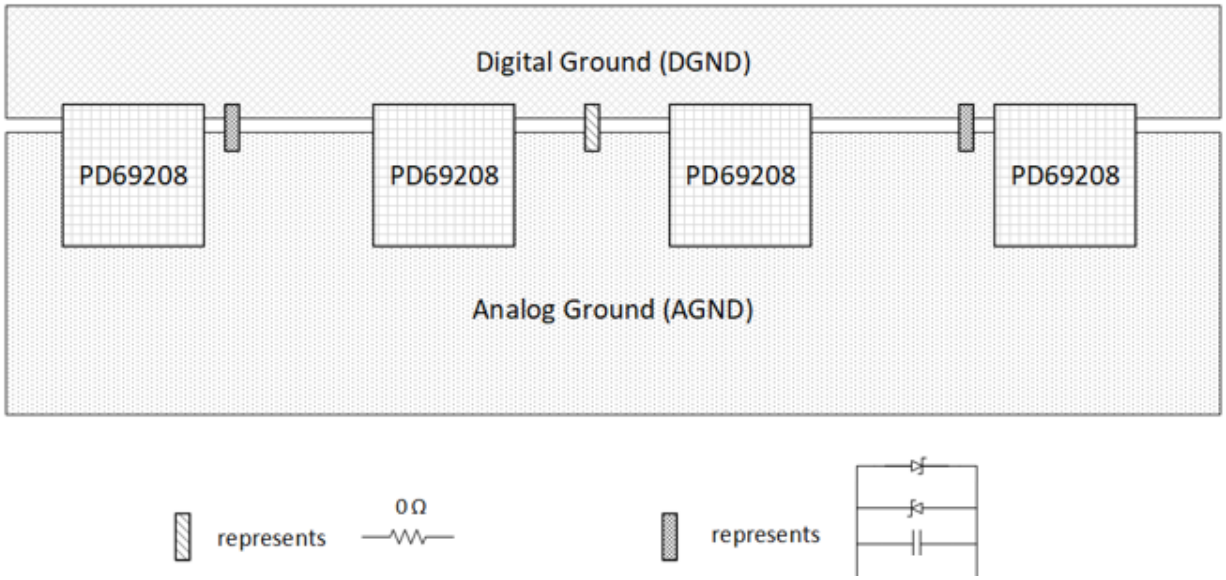
- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69208. The AGND must be located on external layer.
- Earth ground is used to tie in the metal frame of the RJ45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds, as shown in the following figure.

Figure 6-9. Ground and Power Planes



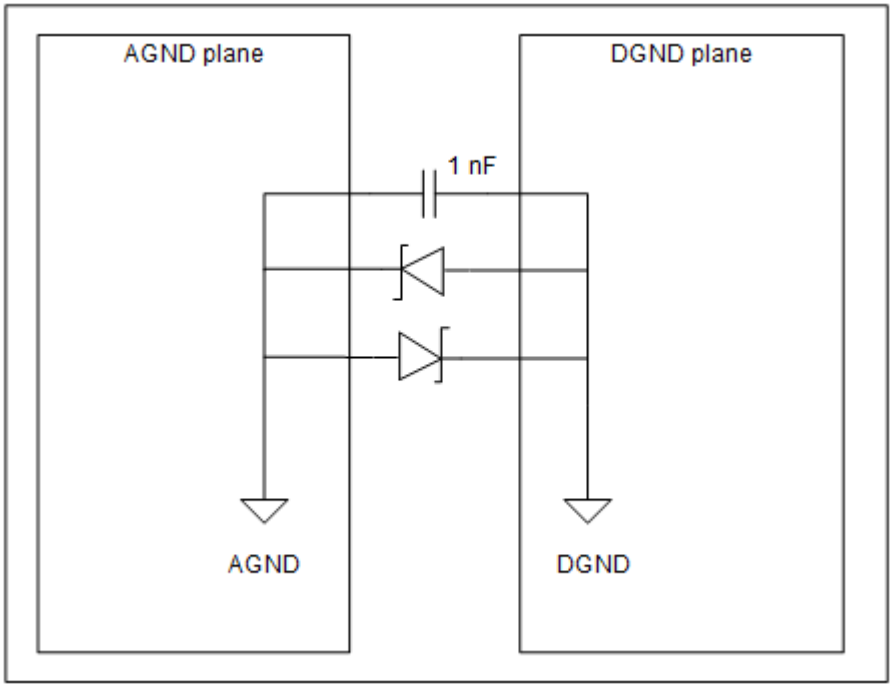
- To connect various digital ground (DGND) points and to enable stable impedance to the ESPI bus traces, extend the DGND surface under pins 41–56 of the PD69208 managers.
- A focal interconnection point for the digital and analog grounds must be located at about the middle of the overlapping section, as shown in the following figure.

Figure 6-10. Single-Point Connection Between DGND and AGND



- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inversed Schottky diodes near each PoE manager between the analog and digital layers, as shown in the following figure. The capacitors form low impedance paths for digital driving signals.

Figure 6-11. Grounding Scheme

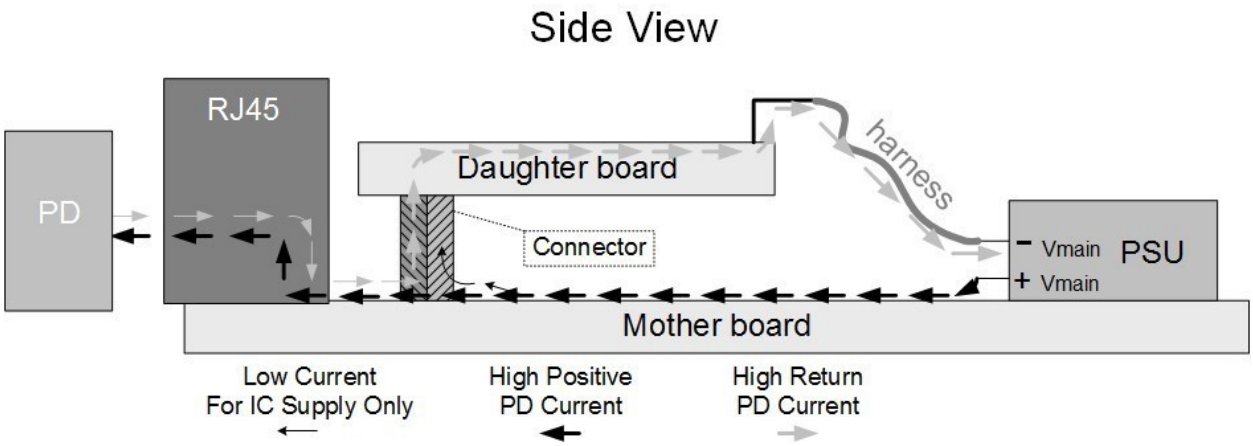


- The power and return (ground) planes for the V_{MAIN} supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using wide copper lands. When implementing the PoE circuitry on a daughter board, the high current does not have to be routed through the daughter board but only the return path, as seen in the following figure.

6.2.3 Current Flow Through the PoE Application Utilizing a Daughter Board

The current flow through the PoE application daughter board is shown in the following figure.

Figure 6-12. Blocks Identification for PD69208 Circuitry (Side View)



The port's DC current flows in an application utilizing a PoE DB as follows.

1. Coming from the switch's power supply positive to the center taps of the line transformer through a mother board wide trace (not through the DB).
2. From the center tap of the line transformer through the switch's RJ45 to the PD side.
3. The return current from the PD flows through the RJ45 and the line transformer to the DB PoE circuitry.
4. From the DB analog ground (AGND), the current flows back to the switch's power supply negative through harness.

Note: The positive port's heavy current flows directly to the PD side without going through the PoE managers on the DB.

6.2.4 Conductor Routing

The following sections describe the conductor routing guidelines.

6.2.4.1 General Guidelines

The conductor (or printed lands) routing is performed as practiced in the general layout guidelines, specifically listed as follows.

- Conductors that deliver a digital signal are routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

6.2.4.2 Specific Requirements for Clock and Sensitive Signals

The following issues require special design considerations.

- The I_{REF} resistor (connects to pin 24), used for current reference, must be directly connected to AGND and pin 24 using the shortest path.

6.2.4.3 Port Outputs

For robust design, the port output traces are 45-mil wide to handle maximum current and port power. However, to obtain a 10 °C (maximum) copper rise under 1A per port, set the minimum width for traces in accordance with the layer location and copper thickness, listed as follows.

- For two ounce copper, external layer: 15 mils
- For two ounce copper, internal layer: 20 mils
- For one ounce copper, external layer: 25 mils
- For one ounce copper, internal layer: 40 mils
- For ½ ounce copper, external layer: 30 mils
- For ½ ounce copper, internal layer: 55 mils (20 °C copper rise)

Additionally, the following port output guidelines must be considered.

- The port output traces must be short and parallel to each other to reduce RFI pickup and keep the series resistance low.
- The PoE port outputs must be connected to the switch's pulse transformers, as shown in Figure 6-6. The common mode choke and Bob Smith termination (resistor-capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is located as close as possible to the pulse transformer.
- Route the ESPI communication clock (SCK) line coming from the PoE controller carefully so that it does not disturb the other lines. Two ground lines (connected to DGND) can be routed alongside the clock line to isolate it from the rest of the lines.

6.3 Specific Component Placement

The following section provides placement details for specific components.

6.3.1 Peripheral Components

To minimize heat transfer among various components, a gap between them must be maintained. The following are suggested gaps, but any gap can be used if the designer monitors the thermal performance during the design and follows the maximum temperatures allowed at the various components.

- Minimum gap between the PD69208 ICs must be 50 mm.
- Minimum gap between the PD69208 and the PoE controller must be 30 mm.
- Minimum gap between the PD69208 and the NPN transistor regulator (if used) must be 50 mm.

6.3.2 PoE Controllers and Peripherals

For PD69210 and PD69220, see the Microchip SAM D21/DA1 Family Datasheet for recommendations related to the PoE controller layout guidelines

For PD69200, see the Freescale Semiconductor MKL15Z128VFM4 Datasheet for recommendations related to the PoE controller layout guidelines.

The following guidelines are for the integration of the PoE controller into a PoE circuit.

- Locate the filtering capacitors for V_{DD} and for V_{DDA} close to power and ground pins.
- Termination resistors for the outgoing ESPI digital lines must be located close to the respective driving pins.

6.3.3 PD69208T4, PD69208M, or PD69204T4 PoE Manager and Peripherals

The side of the PoE manager that includes pins 41–56 must face the DGND plane. These pins function as communication and control pins for the manager; connect between the PoE manager and the PoE controller through isolation circuitry.

Locate the bypass capacitors for the PoE manager supply input close to the relevant pin. If two bypass capacitors are placed on the same line, then locate the lower valued capacitor closer to the pin on the same layer and place the higher valued capacitor at a more distant location.

Locate the V_{AUX5} and V_{AUX3P3} 0.1 µF and 4.7 µF filtering capacitors as close as possible to the PoE manager's pins 20 and 22, respectively.

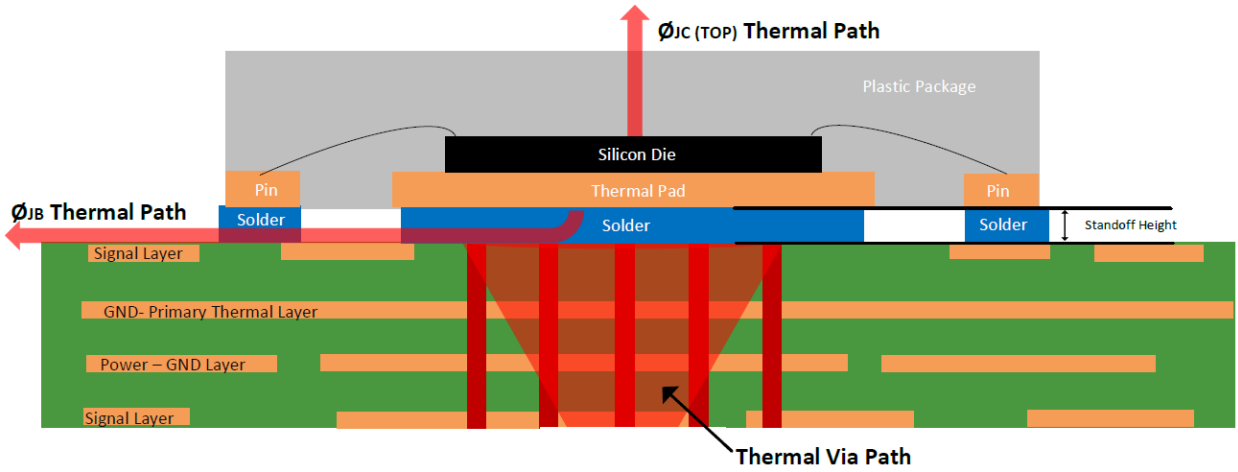
6.3.4 V_{MAIN} Capacitors

It is a good design practice to have 47 µF capacitors near each RJ45 gang, over V_{MAIN}, to prevent noise and spikes events to penetrate the V_{MAIN} rail.

7. Thermal Pad Design

For proper heat dissipation, the recommended footprint/layout guidelines must be followed.

Figure 7-1. Heat Dissipation in PCB



There are three thermal paths for heat to flow from the IC.

- Heat flow from the junction to the package side and pins. This parameter is a package parameter and is defined by ØJB in the device datasheet.
- Heat flow from the junction to the package top surface. This parameter is a package parameter and is defined by ØJC (TOP) in the device datasheet.
- Heat flow from the junction to the package bottom surface (the thermal pad) through the thermal vias to the various thermal ground planes. This is the most significant thermal path. The thermal resistance of this path is determined by the package e-pad design and the PCB construction: number PCB layers, number of thermal vias, construction of thermal vias, size and location of the copper thermal plane. This is the primary heat flow path. Therefore, it is important to follow footprint recommendations.

The footprint that details the solder mask, copper layers, and paste mask that is recommended is detailed in the PD6920x datasheet.

- Per IPC7093 standard standoff must be minimum of 2 mil (0.050 mm), with a Microchip recommended target of 2.5 mil (0.0635 mm). For this reason, a paste mask stencil thickness of 5 mils must be considered.
- Thermal vias must be unplugged with a diameter approximately 0.33 mm. Microchip recommends a 7 × 7 via array and no solder paste covering on the bottom PCB layer.
- Solder paste is a 9 × 9 array with **streets** in-between the array. It is important to have streets to allow for outgassing during the reflow process to help achieve a uniform standoff height.

The PCB copper thermal planes must be of maximum practical area on as many PCB layers as possible.

See the device datasheet for package footprint guidelines.

8. References

The following documents can be obtained from Microchip Power over Ethernet.

- *PD69208T4, PD69204T4, and PD69208M PoE PSE Manager Datasheet*
- *PD69210/PD69220 PoE PSE Controller Datasheet*
- *PD69200 PoE PSE Controller Datasheet*

Consult Microchip for *AN3378 Surge Protection 8-Port PSE PoE Manager PD69208T4/M/4T4*.

The following are available on Microchip's Software Library.

- *Firmware (without the boot section), GUI, and API*
- *PD692x0 Communication Protocol User Guide*

In addition, the following non-Microchip documents can be consulted.

- *IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet*
- *IEEE 802.3af-2003 Standard, DTE Power via MDI*
- *IEEE 802.3at-2009 Standard, DTE Power via MDI*

Technical support for Microchip PoE products is available at the Microchip Technical Support Portal.

9. Revision History

Revision	Date	Description
C	02/2023	The following is the summary of changes made in this revision: • Edited – Features – 1.5.3. Front-End Components – 3.3. Controller Setup • Replaced Figure 4-7 • Added Table 4-3 • Edited Table 5-5
B	06/2022	• Added IEC 62368-1 Ed.3 requirements to list of Features and section Front-End Components. • Added section 3.3.4 Save System Settings. • Updated C36 to R52 in Figure 4-7. PD69208 PoE Manager Circuitry and Table 5-5. PD69208 PoE Manager Circuitry Components.
A	07/2020	Updated the application note as per Microchip standards. Changed AN250 to AN3361. Changed PD-000392301 to DS-00003361.

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