PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications

PIC18F25/45/55Q43

The PIC18F25/45/55Q43 devices you have received conform functionally to the current device data sheet (DS40002170**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F25/45/55Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID				
		B0	B2	B3	D2	E0
PIC18F25Q43	0x73C0	0xA040	0xA042	0xA043	0xA0C2	0xA100
PIC18F45Q43	0x73E0	0xA040	0xA042	0xA043	0xA0C2	0xA100
PIC18F55Q43	0x7400	0xA040	0xA042	0xA043	0xA0C2	0xA100

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ43 Family Programming Specification"** (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				B0	B2	B3	D2	E0
ADCC	Capacitive Voltage Divider	Capacitive Voltage Divider (CVD)	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X				
	Double Sample Conversions	Double Sample Conversions	An unexpected acquisition time is added between the first and second conversions.	X	X	X	X	X
Oscillator	XT mode	Maximum Clock Frequency Limited to 2 MHz for XT Mode	Maximum clock frequency limited to 2 MHz for XT mode	X	X			
I²C	I²C	The I2CxADR0/1/2/3 Registers Have Incorrect Reset Value	I2CxADR0/1/2/3 registers have incorrect Reset value	X	X	X		
	I²C	The I2C Start and/or Stop Flags May Be Set When I2C Is Enabled	I2C Start and/or Stop flags may be set when I2C is enabled	X	X	X	X	
	Multi-Host mode	Operating in Multi-Host Mode Will Cause Bus Failures	Multi-Host mode will cause bus failures	X	X	X	X	X
	Host Data Request (MDR) bit	MDR Bit Is Not Cleared after Bus Time-Out	MDR bit is not cleared after Bus Time-Out	X	X	X	X	X
	Bus Time-Out	Bus Time-Out Not Detected Properly When External Host Clock Stretches	Bus Time-Out not detected properly when External Host Clock stretches	X	X	X	X	X
	Clock Stretch Disable	Clock Stretch Disable Not Working Properly	Clock Stretch Disable not working properly	X	X	X	X	X

.....continued

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				B0	B2	B3	D2	E0
I^2C	Bus Time-Out	Bus Time-Out Causes False Start/Stop	Bus Time-Out causes false Start/Stop	X	X	X	X	X
	CSTR Bit	CSTR Bit Is Not Cleared after Bus Time-Out	CSTR bit is not cleared after Bus Time-Out	X	X	X	X	X
	Bus Free Time	The Bus Free Divider Ratio BFREDR = 1 Value Is Not Functional	The Bus Free Divider Ratio BFREDR = 1 value is not functional.	X	X	X	X	X
	Bus Collision	Bus Collision Followed by a Stop Condition during a Transaction by an External Host Device May Hang the Bus	Bus Collision Followed By a Stop Condition During a Transaction by an External Host Device May Hang the Bus	X	X	X	X	X
	Multi-Host Arbitration	I2C Module May Hang the Bus during Multi-Host Arbitration	I2C Module May Hang the Bus During Multi-Host Arbitration	X	X	X	X	X
SRAM	SRAM read-back	SRAM Read-Back	SRAM read-back can be incorrect	X				
In-Circuit Debug	Software breakpoints	Software Breakpoints Are Not Available	Software breakpoints are not available	X	X	X	X	X
SMT	Reset bit	Reset Bit	Module stops working if RST bit is set while prescaler setting is not zero	X	X	X	X	X
Universal Asynchronous Receiver Transmitter	UART	UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted	UART TXDE signal may go low before the STOP bit has been entirely transmitted	X	X	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X				

1.1.2 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no Pre-charge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Pre-charge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.2 Module: Oscillator (OSC)

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

B0	B2	B3	D2	E0

X	X			

1.3 Module: Inter-Integrated Circuit (I^2C)

1.3.1 The I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/2 registers reset to `0xFF` when the I2CxMD is enabled instead of `0x00`. The I2CxADR1/3 registers reset to `0xFE` when the I2CxMD is enabled instead of `0x00`.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X		

1.3.2 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	

1.3.3 Operating in Multi-Host Mode Will Cause Bus Failures

If operating in Multi-Host mode and a second host drives SDA low at the same time the Start bit is generated, the module will fail to go into Host mode, but will continue to send an address and data as if it won arbitration. I2CCNT fails to decrement, and the module will remain in this state until a bus time-out occurs or the device is reset.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.4 MDR Bit Is Not Cleared after Bus Time-Out

In the Host mode of the I²C module, when a bus time-out occurs during clock stretching and TOREC = 1, the MDR bit will not be cleared and a Stop will not be transmitted on the bus.

Work around

Force a Stop on the bus by setting the P bit upon bus time-out in Host mode. Forcing a Stop on the bus clears the MDR bit.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.5 Bus Time-Out Not Detected Properly When External Host Clock Stretches

When the module is operating in Client mode and an external Host device is clock stretching after the 8th SCL clock and a bus time-out occurs, the bus time-out is not detected properly. When the external Host times out before the Client and releases SCL to generate a Stop condition, the module continues to stretch SDA as if to generate an ACK and hangs the bus, and a Stop is never seen on the bus.

Work around

Reset the module by toggling the EN bit.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.6 Clock Stretch Disable Not Working Properly

When the CSD bit is set between a Start condition and the 8th falling SCL edge, the I²C module enters a state where the module clock stretches indefinitely after the next Start until a bus time-out occurs.

Work around

Force a reset of the module by toggling the EN bit.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.7 Bus Time-Out Causes False Start/Stop

When the module is operating in Client mode and an external Host device is clock stretching and a bus time-out occurs in the Client, the Client releases SDA and goes into the idle state. After the external Host generates a Stop condition on the bus by releasing SCL, the module can erroneously drive a low pulse on the SDA line, which acts as a false Start and Stop on the bus.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.8 CSTR Bit Is Not Cleared after Bus Time-Out

When the module is operating in Client mode and TOREC = 1, and a bus time-out occurs during clock stretching, the CSTR bit will not be cleared, and the module continues to clock stretch and hang the bus.

Work around

Reset the I²C module by toggling the EN bit.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.9 The Bus Free Divider Ratio BFREDR = 1 Value Is Not Functional

Setting the Bus Free Divider Ratio bit (BFREDR = 1) has no effect on the Bus Free Time Divider ratio.

Work around

Maintain BFREDR = 0 at all times.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.10 Bus Collision Followed by a Stop Condition during a Transaction by an External Host Device May Hang the Bus

In a Multi-Host environment, when another Host device on the bus causes a collision (BCLIF bit) and forces a Stop during a transaction, the I²C module may not respond appropriately and hang the bus.

Work around

When a Bus Collision (BCLIF) is detected along with a Stop condition (PCIF), reset the I²C module by toggling the EN bit.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.3.11 I²C Module May Hang the Bus during Multi-Host Arbitration

The I²C module may hang the bus in a Multi-Host environment when another Host device initiates a transaction on the bus by issuing the Start condition before the I²C module pulls down the SDA line, and the most significant bit of the address header starts with a '0' in FME=0 or FME=1 mode.

Work around

When using FME=0 or FME=1 modes, the user can choose to assign addresses such that the most significant bit of the address header starts with a '1'. Alternatively, the user can select the FME=2 mode of operation.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.4 Module: SRAM

1.4.1 SRAM Read-Back

Following a device power-up sequence, there is a possibility that some SRAM locations will not return the expected written value but will read back '00' instead.

Work around

None. The device can only recover by power cycling.

This erroneous condition can be detected by running the following code that writes nonzero values to SRAM and then verifies that the returned read values are not '00'. If a returned value is '00', the application code has to be put into a safe state until a POR event occurs. This code has to be executed immediately after power-up. If the test passes, the device operation will be normal.

```
// SRAM test

FSR0 = 0xcff;         // Write data into RAM address for devices up to 2K RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 2K of SRAM, add the following code
FSR0 = 0x14ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 4K of SRAM, add the following code
FSR0 = 0x24ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to Safe state
}
```

Affected Silicon Revisions

B0	B2	B3	D2	E0
X				

1.5 Module: In-Circuit Debug

1.5.1 Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.6 Module: Signal Measurement Timer (SMT)

1.6.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment,

and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work around

Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

B0	B2	B3	D2	E0
X	X	X	X	X

1.7 Module: Universal Asynchronous Receiver Transmitter (UART)

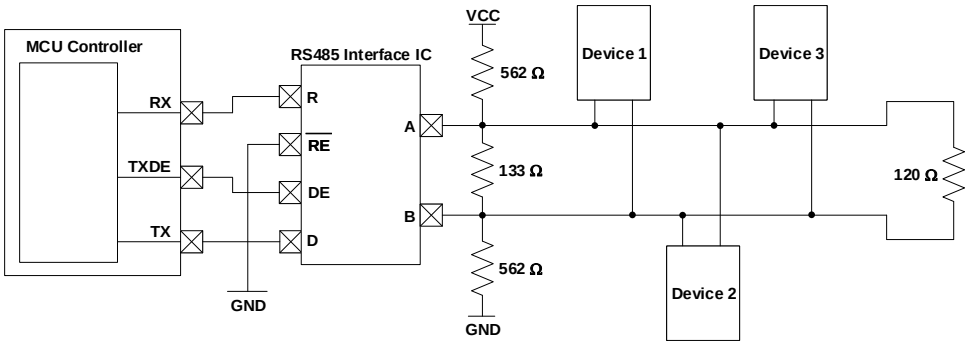
1.7.1 UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

B0	B2	B3	D2	E0

X	X	X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002170**F**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 NVM-Nonvolatile Memory Module (Writing to DFM)

In Section **10.4.2 Writing to DFM**, the stepwise process is clarified to provide specific instructions on when to enable interrupts during the NVM Write sequence. The code example in Example 10-10 is also amended with an additional line. The changes are shown below in **bold**.

1. Set NVMADR registers with the target byte address.
2. Load NVMDATL register with desired byte.
3. Set the NVMCMD control bits to `'b011` (Byte Write).
4. Disable all interrupts.
5. Perform the unlock sequence as described in the Unlock Sequence section.
6. Set the GO bit to start the DFM byte write.
7. **Interrupts can be enabled after the GO bit is set. If it is not desired to have interrupts during DFM write, then enable interrupts after the next step when the GO bit is cleared.**
8. Monitor the GO bit or NVMIF interrupt flag to determine when the write has been completed.
9. Set the NVMCMD control bits to `'b000`.

Example 10-10. Writing a Byte to Data Flash Memory in C

```
// Code sequence to write one byte to a DFM
// DFM target address is specified by DFM_ADDR
// Target data are specified by ByteValue

// Save interrupt enable bit value
uint8_t GIEBitValue = INTCON0bits.GIE;

// Load NVMADR with the target address of the byte
NVMADR = DFM_ADDR;
NVMDATL = ByteValue;               // Load NVMDAT with the desired value
NVMCON1bits.CMD = 0x03;            // Set the byte write command
INTCON0bits.GIE = 0;               // Disable interrupts
//--------- Required Unlock Sequence ---------
NVMLOCK = 0x55;
NVMLOCK = 0xAA;
NVMCON0bits.GO = 1;                // Start byte write
//------------------------------------------------
INTCON0bits.GIE = GIEBitValue;   // Restore interrupt enable bit value (if interrupts are desired during DFM write)
while (NVMCON0bits.GO);            // Wait for the write operation to complete

// Verify byte write operation success and call the recovery function if needed
if (NVMCON1bits.WRERR){
   WRITE_FAULT_RECOVERY();
}

NVMCON1bits.CMD = 0;               // Disable writes to memory
```

2.2 PIC18 CPU (System Arbitration)

The following note has been added after the existing text of Section **7.1 System Arbitration**, to clarify the interaction of the System Arbiter, the PRLOCKED bit and system interrupts.

Important: When the PRLOCKED bit is set, the Non Volatile Memory (NVM) module has a fixed priority of 0 that cannot be changed. If an interrupt is desired when an NVM read/write operation is in progress, then the ISR priority level must be set to 0. The NVM module priority is ignored when PRLOCKED bit is cleared.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
N	8/2024	Added silicon errata items 1.3.9 through 1.3.11; added new data sheet clarifications 2.1 and 2.2.
M	08/2023	Added silicon revision E0; added silicon errata items 1.3.3 through 1.3.8; deleted data sheet clarifications 2.1 and 2.2.
L	03/2022	Added silicon errata items 1.1.2, 1.6.1, 17.1 and data sheet clarifications 2.1 and 2.2.
K	07/2021	Added silicon errata item 1.3.2.
J	03/2021	Added silicon errata item 1.5.1.
H	12/2020	Added silicon revision D2; deleted clarification 2.1.
G	10/2020	Added silicon revision B3 and UART Transmit Collision Interrupt data sheet clarification; updated silicon errata item 1.3.1.
F	08/2020	Added silicon revision B2.
E	06/2020	Added silicon errata item 1.4.1.
D	06/2020	Added silicon errata item 1.3.1.
C	04/2020	Added XT mode erratum and Temperature Indicator data sheet clarification.
B	02/2020	Added working pins for CVD.
A	12/2019	Initial document release

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