AN1791

Bit-Banging the SDI and SQI Modes of Microchip 23XX512/23XX1024 Serial SRAMs

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INTRODUCTION

This application note explains in detail the recommended usage of the SDI and SQI modes of operation of the Microchip 23XX512/23XX1024 Serial SRAM devices, as well as the possibilities to configure the device for the above alternative modes of operation.

Many embedded systems require some amount of volatile storage for temporary data. Because of their small footprint, low I/O pin requirement, low-power consumption and low cost, serial SRAMs are a popular choice for volatile storage.

Serial SRAM devices are available in a number of density offerings, operational voltage ranges and packaging options. The serial SRAM products offer an alternative to the traditional parallel architecture in order to save board area, I/O count, power, and cost. However, the speed advantages often offered by parallel SRAM can limit the adoption of serial SRAM products into embedded designs.

Microchip Technology has addressed this need by offering a line of serial SRAMs that use not only the industry standard SPI communication, but also two other modes of communication for increased data throughput: SDI and SQI modes, which will be detailed further in this text.

OVERVIEW AND BENEFITS OF SDI AND SQI MODES

The 23XX512/23XX1024 serial SRAM supports SDI (Serial Dual) and SQI (Serial Quad) modes of operation, when used with compatible master devices. As a definition, for SDI mode of operation, two bits are transferred per clock using the SIO0 and SIO1 pins. Bits are clocked MSB first.

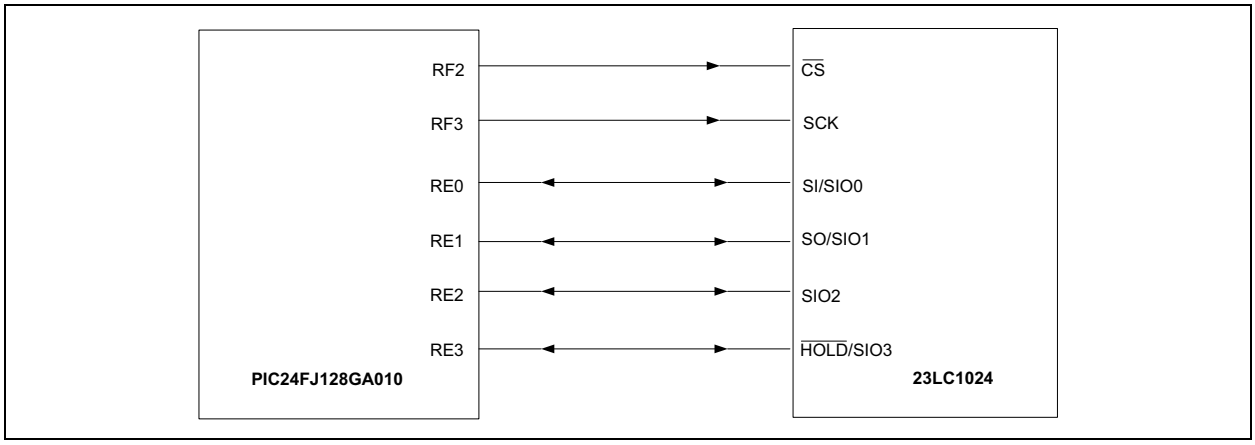
For the SQI mode of operation, one nibble per clock or four bits of data are transferred per clock using the SIO0, SIO1, SIO2 and SIO3 pins. The nibbles are clocked MSB first.

The main reason to use these modes of operation is the increased data rates.

As an example, in the Quad mode, one nibble is entered per clock. This means that, at a rate of 20 MHz, the maximum speed will be 80 Mbits/second.

Note that hardware ports supporting SDI/SQI modes are not common on many MCUs today, so the alternative to communicate on a SDI/SQI bus is to bit-bang using GPIOs (two in the case of the dual protocol, four in the case of the quad protocol).

FIGURE 1: SCHEMATIC DIAGRAM



As presented in Figure 1, the example application uses PORTE of the PIC24FJ128GA010 to drive the four serial lines: SIO0, 1, 2, 3. On an Explorer 16 evaluation board, PORTE also drives the LCD. When operating the 23LC1024 at 3.3V, an Explorer 16 board with a 3V LCD should be used. Using a 5V LCD will result in the input voltage of the SIOx pins to exceed their maximum rated values.

PORTF was used to drive the general command lines: $\overline{CS}$, SCK.

APPLICATION DESCRIPTION

A string (source) is written in the SRAM, then read back (destination string).

The two strings are compared. In case of a mismatch, an error message is displayed on the on-board LEDs. In case of a successful comparison, a success message is displayed on LEDs D3-D10. The display value for errors is 0xFF, and for success is 0x55, where a '1' corresponds to an LED being turned on.

All these actions are performed in four modes of operation:

- Random Byte mode SDI (serial dual interface)
- Random Byte mode SQI (serial quad interface)
- Sequential mode SDI (serial dual interface)
- Sequential mode SQI (serial quad interface)

Since both modes (dual and quad) can be entered from the basic SPI mode (through the EDIO/EQIO commands), every sequence will be ended through the RSTIO command, in order to come back to the basic SPI mode.

Finally, keep in mind that the mode of operation must be set by the user, in firmware, at the beginning of the main function using the "mode" variable (SDI byte, SDI sequential, SQI byte, SQI sequential).

FIRMWARE OVERVIEW

The code was developed on an Explorer 16 evaluation board, using a PIC24 platform (PIC24FJ128GA010). The following software tools were used:

MPLAB® X IDE V2.10. and the XC16 compiler V1.21. Communication was performed through the "bit-bang" method.

The presented drivers are:

- HEADERS (declaring all necessary low-level functions)
  - `delay.h` – for easy and general use, delays were performed in `.asm`, avoiding timers.
  - `spibb.h` – basic SPI access header (the suffix "bb" means bit-bang)
  - `sdibb.h` – header for the serial dual communication
  - `sqibb.h` – header for the serial quad communication
- FUNCTIONS (defining all necessary low-level functions)
  - `delay_func.c`
  - `spibb_func.c`
  - `sdibb_func.c`
  - `sqibb_func.c`

DUAL INTERFACE MODE (SDI)

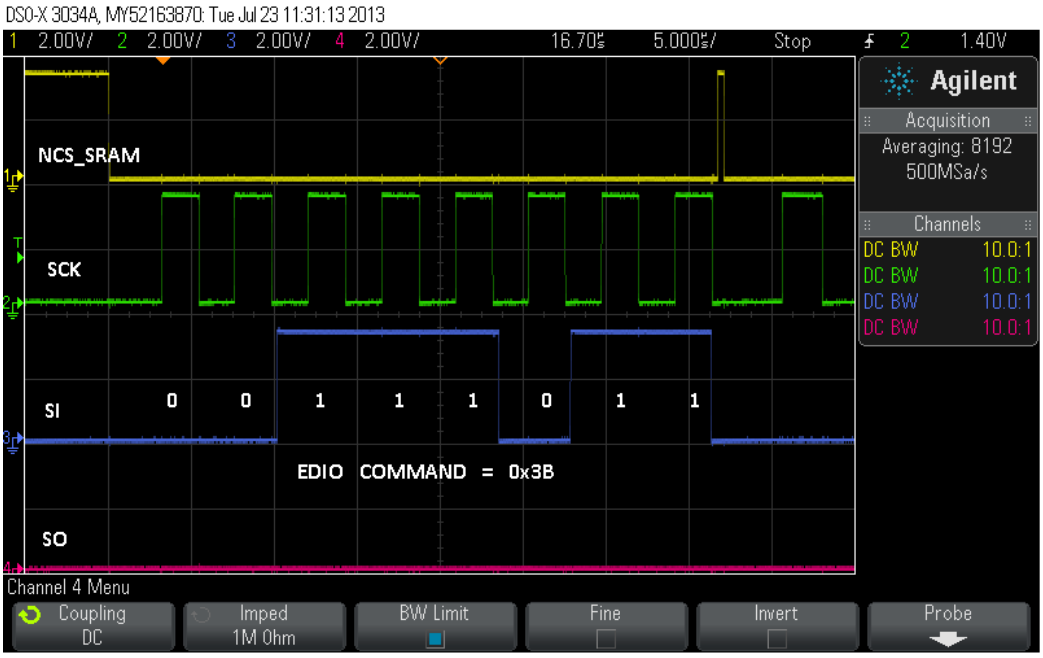
The 23XX512/23XX1024 support the Serial Dual Input (SDI) mode of operation. To enter SDI mode, the EDIO command must be clocked, as shown in Figure 2. It should be noted that if the MCU resets before the SRAM, the user will need to determine the serial mode of operation of the SRAM and reset it accordingly.

Read and write sequences in SDI mode are shown in the figures below.

Entering the SDI Mode from SPI Mode

The SDI mode must be entered through the EDIO command, starting from the SPI mode. The related sequence is shown in Figure 2.

FIGURE 2: ENTERING THE SDI MODE



Writing the Mode Register in SDI Mode

Once in the SDI mode (through the EDIO command), the user may set one of three modes of operation: Byte, Page and Sequential, by writing the mode register. Upon power-up, the 23LC1024 defaults to Page mode.

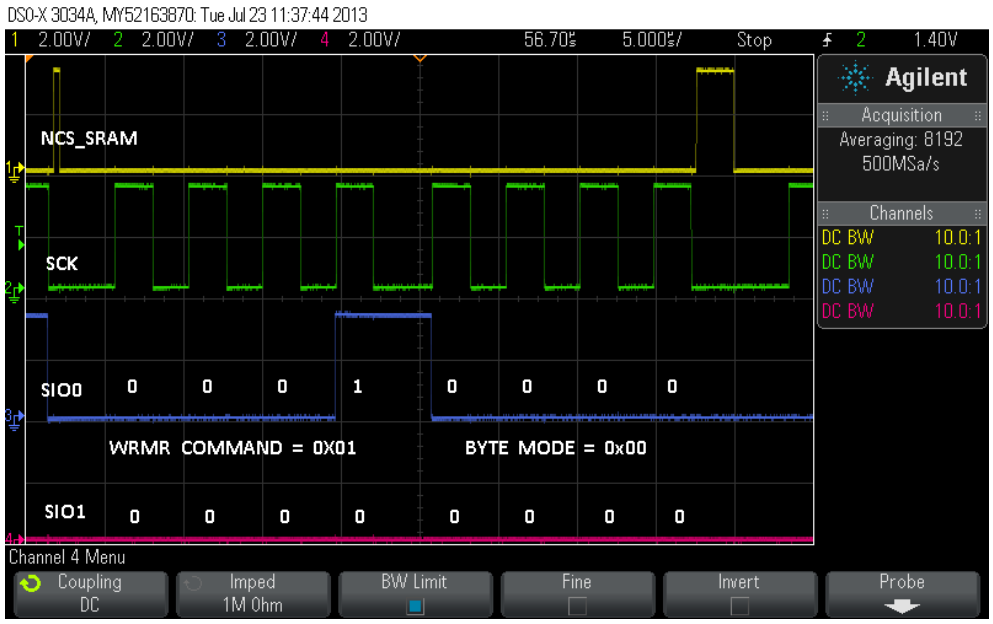
SETTING THE BYTE MODE IN SDI MODE

For the Byte mode, the flow is:

- transmit first the WRMR command
- transmit the Byte mode value

The sequence is shown in Figure 3.

FIGURE 3: ENTERING THE BYTE MODE IN SDI MODE



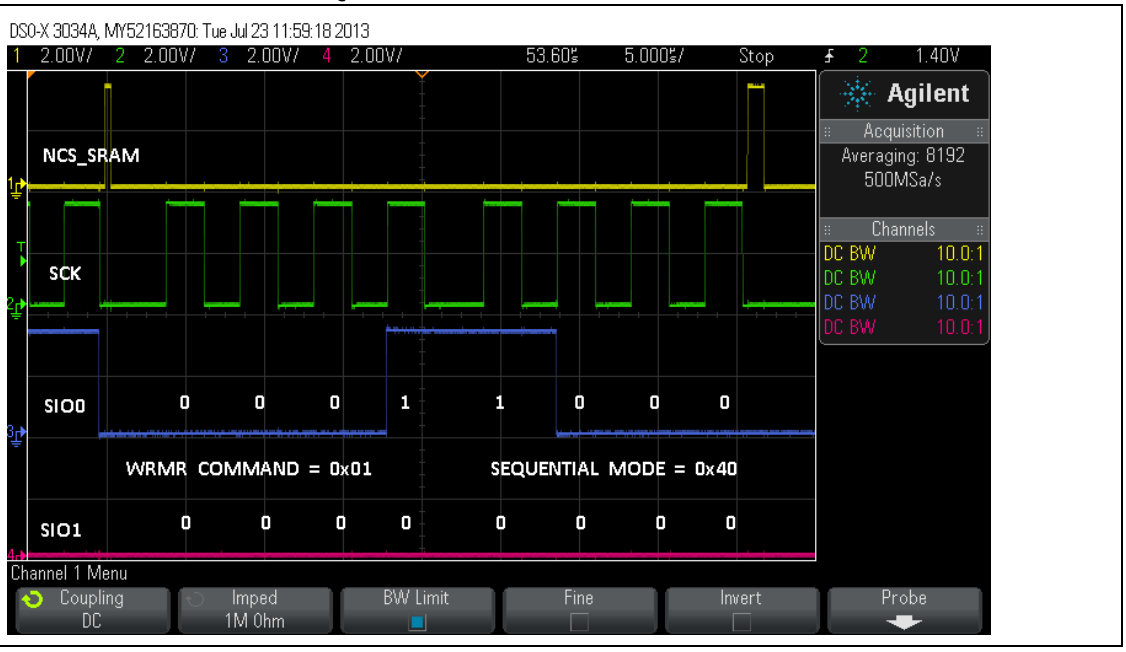
SETTING THE SEQUENTIAL MODE IN SDI MODE

For the Sequential mode, the flow is:

- transmit first the WRMR command
- transmit the Sequential mode value

The sequence is depicted in Figure 4.

FIGURE 4: ENTERING THE SEQUENTIAL MODE IN SDI MODE



Writing a Byte in SDI Mode

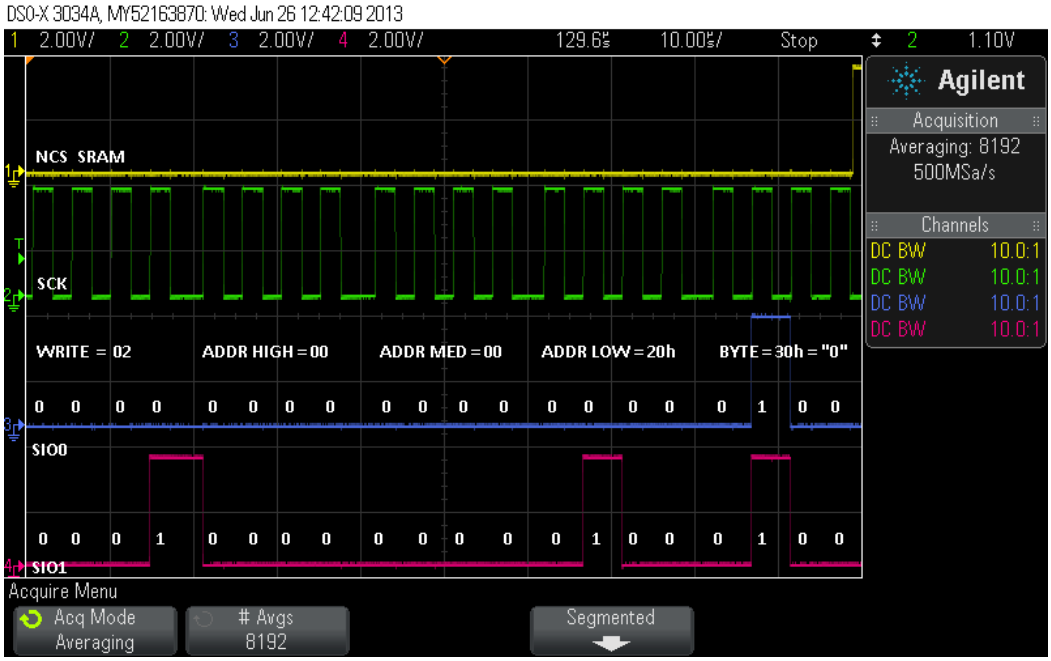
The general flow is:

- assert $\overline{CS}$ low
- transmit the Write command
- send the three address bytes: high, medium, low
- send the data byte
- deassert $\overline{CS}$ high

The sequence is shown in Figure 5.

Since two wires are used to send the information (SIO0, SIO1), four clocks are needed per byte.

FIGURE 5: WRITING A BYTE IN SDI MODE



Reading a Byte in SDI Mode

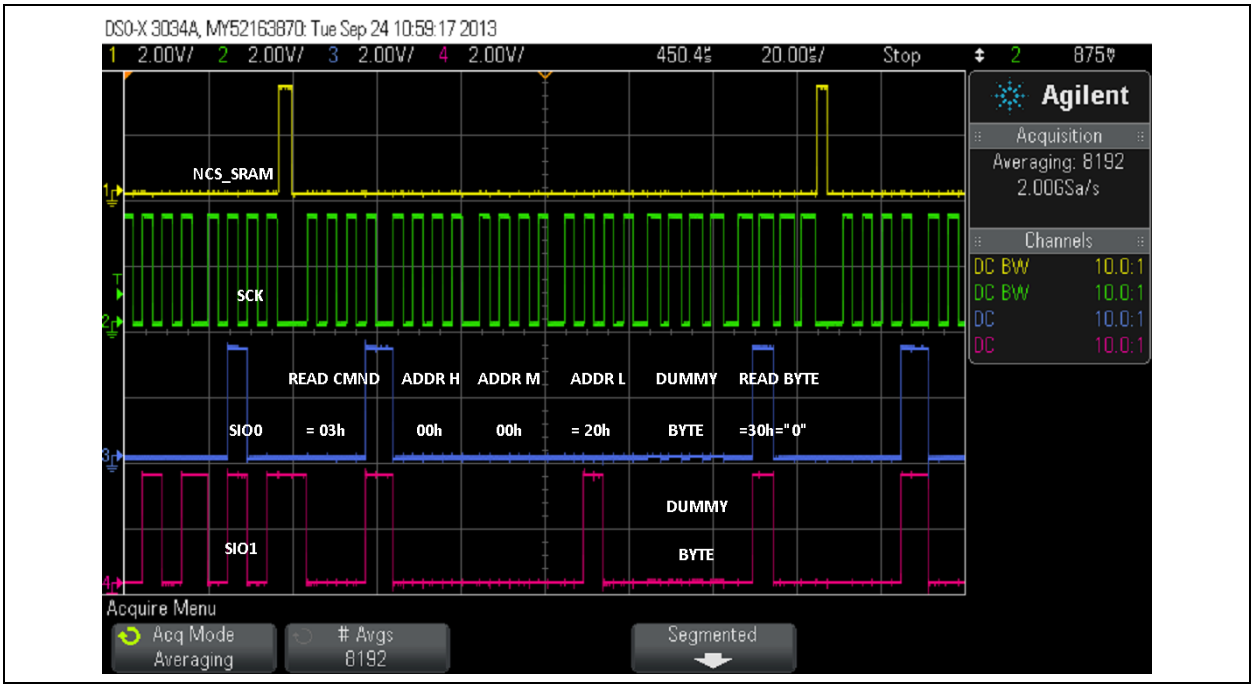
The general flow is:

- assert $\overline{CS}$ low
- transmit the Read command
- send the three address bytes: high, medium, low
- read the first byte, which is a dummy byte.
- read the useful byte
- deassert $\overline{CS}$ high

The sequence is shown in Figure 6.

Note: Keep in mind that during the dummy byte, the SRAM does not offer a valid byte, but instead, the SIOx lines are high-impedance. At the same time, the MCU is waiting to read and, accordingly, the related GPIOs are set as inputs. Therefore, the state of the bus is high-impedance.

FIGURE 6: READING A BYTE IN DUAL MODE

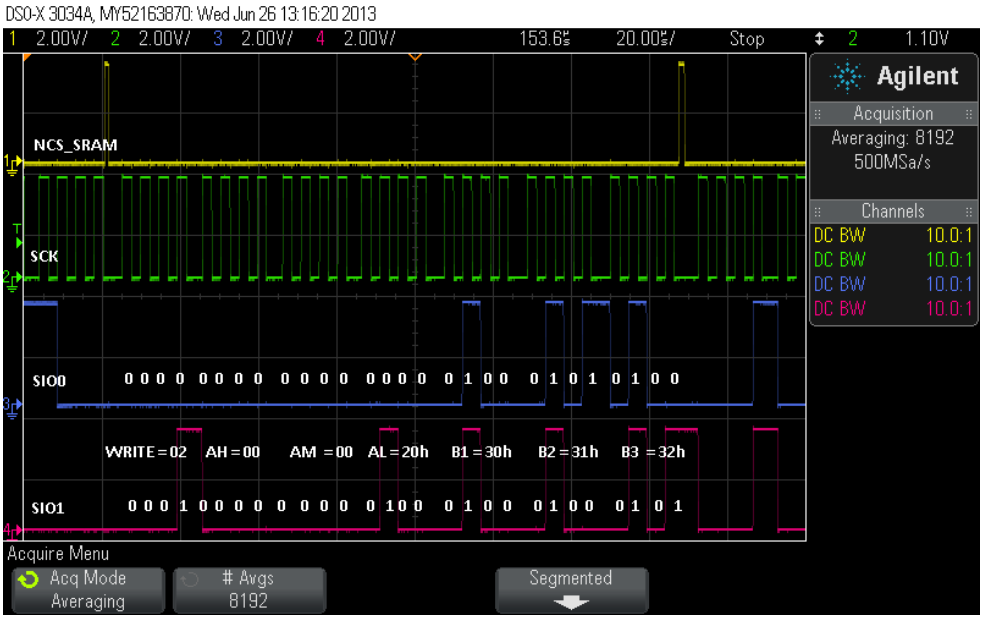


Writing a String (Sequential) in SDI Mode

The flow of the sequential write is similar to the random byte write, except that the user may write as many bytes as necessary, until the $\overline{CS}$ is again deasserted high.

While operating in Page mode, the write is limited to the current page, whereas operating in Sequential mode allows the entire array to be written in a single command. The sequence is presented in Figure 7.

FIGURE 7: WRITING A STRING IN SDI SEQUENTIAL MODE



Note 1: AH = High address

2: AM = Medium address

3: AL = Low address

4: B1 = First written byte

5: B2 = Second written byte

6: B3 = Third written byte

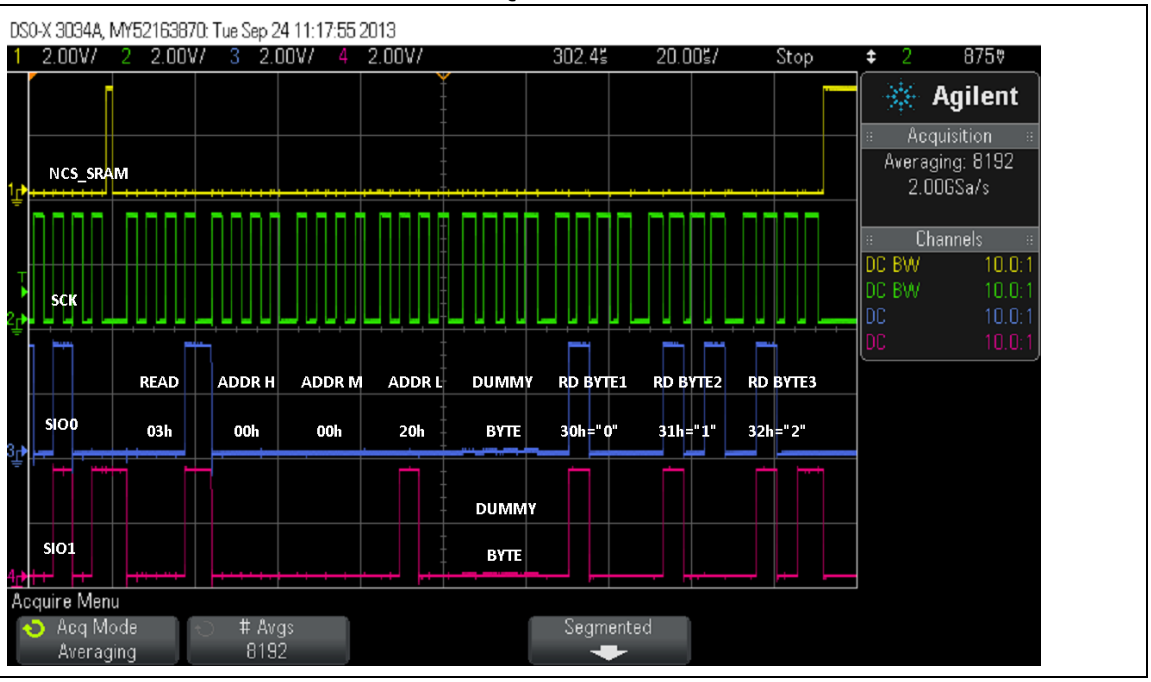
Reading a String (Sequential) in SDI Mode

The flow of reading a string in Sequential mode is similar to the read of random byte, except that the user may read as many bytes as necessary, until $\overline{CS}$ is again deasserted high.

The first read byte is a dummy byte.

The sequence is shown in Figure 8.

FIGURE 8: READING A STRING IN SDI SEQUENTIAL MODE

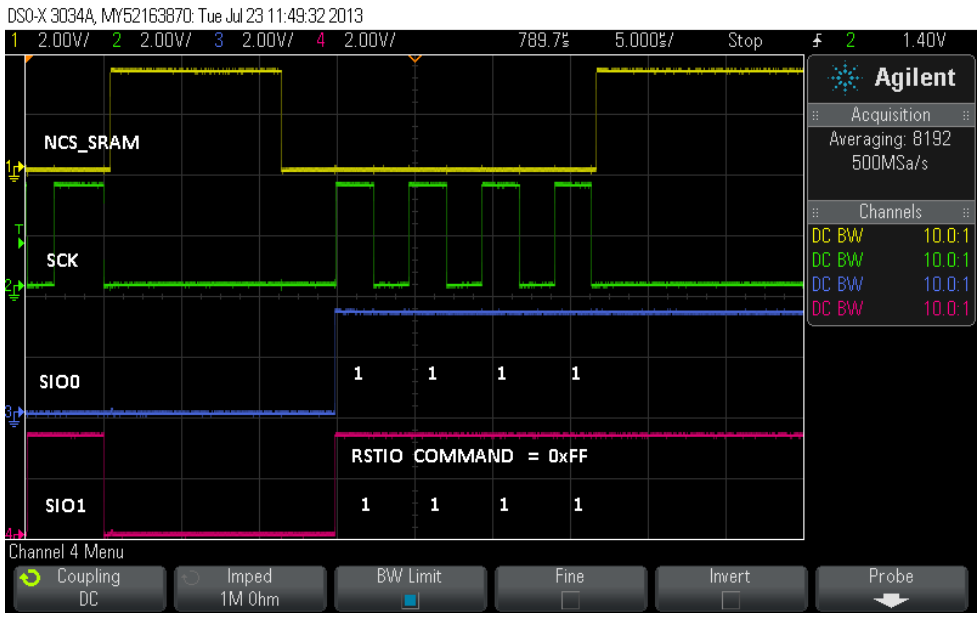


The SIOx signals are high-impedance during the dummy byte.

Exiting the SDI Mode

To exit the Dual mode and return to the basic (default) SPI mode, the RSTIO command (FFh) must be transmitted on the two lines of the SDI interface. The streaming is shown in Figure 9.

FIGURE 9: EXITING THE SDI MODE



QUAD INTERFACE MODE (SQI)

In addition to the Serial Dual interface (SDI) mode of operation, Serial Quad Interface (SQI) is also supported. In this mode the hold functionality is not available since the HOLD pin is used for communication.

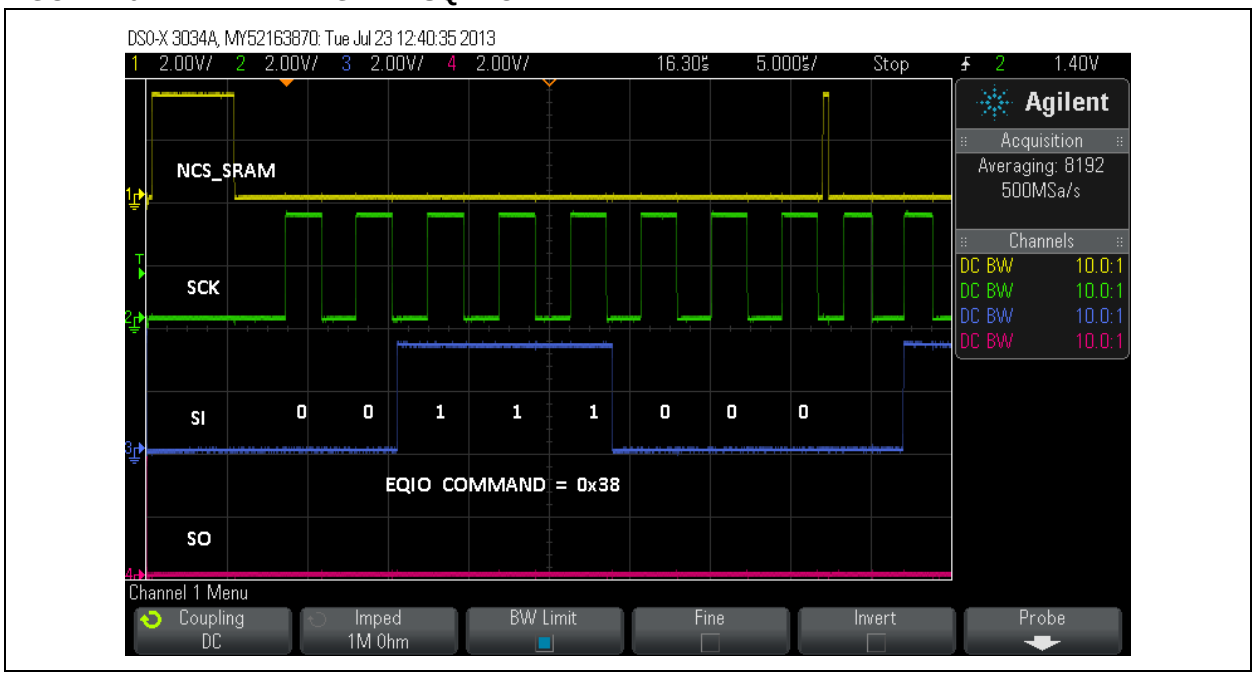
This mode has the same operating principles as the SDI mode. The only difference is the number of wires, four instead of two.

To enter SQI mode, the EQIO command must be clocked, as shown in Figure 10.

Entering the SQI Mode from SPI Mode

The SQI mode must be entered from the SPI mode by issuing the EQIO command. The related sequence is shown in Figure 10. Only the EQIO waveform is shown; waveforms for SQI commands are not shown due to a limitation in the number of available scope channels (only four).

FIGURE 10: ENTERING THE SQI MODE



The SQI mode can be exited (returning to the default SPI mode) in the same manner as the Dual mode, except that the RSTIO command (FFh) is issued on four wires instead of two.

CONCLUSION

This document presents basic support for customers who need to use the two fast modes of communication (SDI and SQI) with Microchip's serial SRAMs 23XX512/23XX1024. Many of the necessary headers and drivers are presented, as well as an example of the main function, detailing how to access (read/write) the serial SRAM.

The code was developed on a Explorer 16 evaluation board, using a PIC24 platform (PIC24FJ128GA010). The software tools used are: MPLAB X IDE V2.10 and the XC16 compiler V1.21.

APPENDIX A: REVISION HISTORY

Revision A (07/2014)

Initial release of this document.

NOTES:

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ISBN: 978-1-63276-383-9

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