PIC18(L)F65/66K40 Family Silicon Errata and Data Sheet Clarifications

PIC18(L)F65/66K40

Product Page Links

Introduction

The PIC18(L)F65/66K40 devices that you have received conform functionally to the current device data sheet (DS40001842**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18(L)F65/66K40 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A3	A4
PIC18F65K40	0x6B00	0xA003	0xA004
PIC18LF65K40	0x6B60	0xA003	0xA004
PIC18F66K40	0x6AE0	0xA003	0xA004
PIC18LF66K40	0x6B40	0xA003	0xA004

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A3	A4
Analog-to-Digital Converter (ADC)	ADC Conversion	1.1.1	Delay of one instruction cycle required prior to setting the ADGO bit when using ADCRC as the ADCC clock source.	X	
	ADCRC Oscillator Operation in Sleep	1.1.2	The ADCRC oscillator does not stop after conversion is complete in Sleep mode.	X	X
	ADC Conversion with FVR	1.1.3	Using FVR as the ADC positive voltage reference can cause missing codes.	X	X
	ADC Conversion with F_{OSC} as Clock	1.1.4	The ADGO bit remains set when using F_{OSC} as clock source with clock divider.	X	X
	ADC Operation in Burst Average Mode	1.1.5	The ADCNT register does not increment past `'0b1'` in Burst Average mode with double sampling enabled.	X	X
	Double Sample Conversions	1.1.6	An unexpected acquisition time is added between the first and second conversions.	X	X
	ADC Acquisition Time	1.1.7	Conversion during Sleep mode when ADACQ = `0` affects results on values in the upper half of the 10-bit range. The analog input is disconnected for 3-4 uS and the first bit of the result becomes zero.	X	X
	ADC Short in Pre-Charge State	1.1.8	ADC shorts briefly in pre-charge state when the corresponding analog pin is selected as an output.	X	X
PIC18 Debug Executive	Data Write Match Breakpoints	1.2.1	Data write match breakpoints do not work when used on a location GSR space.	X	
	Single Step Function (SSTEP)	1.2.2	Single Step function does not execute at SW Breakpoint.	X	X
PIC18 Core	TBLRD	1.3.1	TBLRD requires NVMREG value to point to appropriate memory.	X	
Program Flash Memory (PFM)	Endurance of PFM Cell	1.4.1	Endurance of the PFM cell is lower than specified.	X	X
	Back to Back Writes	1.4.2	Repetitive writes may cause write/erase failures.	X	X
MSSP	SMBus 2.0 Voltage Level	1.5.1	Input low-voltage threshold level is dependent on V_{DD}.	X	X
	SPI	1.5.2	SSPBUF may become corrupted.	X	X
	I^2C	1.5.3	Acknowledge failure on LF devices only.	X	
Electrical Specifications	Min V_{DD} Specification	1.6.1	V_{DDMIN} specifications are changed for LF devices only for -40°C and 0°C.		X
	FVR Specification	1.6.2	FVR specifications require use above -20°C.	X	X
	Analog-to-Digital Converter	1.6.3	ADC offset error specification is +/-3.0 LSb.	X	X
Timer0	Synchronous Mode	1.7.1	TMR0 does not function properly in Sync mode.	X	X
	Clock Source	1.7.2	TMR0H register does not increment when the clock source is Fosc/4 and the T0ASYNC bit is cleared.	X	X
Windowed Watchdog Timer (WWDT)	WWDT Operation in Doze Mode	1.8.1	Erroneous window violation error occurs in Doze mode.	X	X
Nonvolatile Memory (NVM)	NVMERR Bit Operation	1.9.1	NVMERR bit is set incorrectly due to specific Reset events.	X	X
Signal Measurement Timer (SMT)	Reset Bit	1.10.1	Module stops working if RST is set while prescaler setting is not zero.	X	X

Table 2. Silicon Issue Summary (continued)

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A3	A4
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Transmit Mode	1.11.1	Possible duplicate byte transmitted.	X	X
Capture/ Compare/PWM Module (CCP)	PWM Mode	1.12.1	Duty cycle values are incorrect.	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.13.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled.	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: ADCC - Analog-to-Digital Converter with Computation

1.1.1. ADC Conversion

When using the ADCRC as the clock source for ADCC, there is a delay of one instruction cycle between setting the ADGO bit and being able to read it as set. This delay may result in a false conversion complete scenario (i.e., ADGO being cleared), particularly if the user code has a bit clear test `BTFSC` instruction on the ADGO bit immediately after setting it. See code example below.

```
BSF ADCON0, ADGO                    ;    Start conversion
BTSFC ADCON0, ADGO                  ;    Is conversion done?
GOTO $-1                            ;    No, test again
```

Work around

Add a `NOP` instruction after setting the ADGO bit and before testing the bit for completion of conversion. See code example below.

```
BSF ADCON0, ADGO                    ;    Start conversion
NOP
BTSFC ADCON0, ADGO                  ;    Is conversion done?
GOTO $-1                            ;    No, test again
```

Affected Silicon Revisions

A3	**A4**						
X							

1.1.2. ADCRC Oscillator Operation in Sleep

If the part is in Sleep and the ADCRC oscillator is used as the clock source for the ADC, the oscillator will continue to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.3. Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Method 1:

Increase the bit conversion time, known as T_{AD}, to 8 µs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.4. ADC GO Bit May Remain Set When the Clock Source is F_{OSC}

When using F_{OSC} as the clock source (ADCON0.CS = 0) and any clock divider setting other than $F_{OSC}/2$ is selected, the ADGO bit remains set and the conversion does not complete.

Work around

Method 1:

When using F_{OSC} as the clock source (ADCON0.CS = 0), clear the ADCLK register value to zero (ADCLK.CS = 0) and ensure that the F_{OSC} frequency does not violate any timing requirements for the ADC.

Method 2:

Use ADCRC as the clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.5. ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (ADMD = 0b011 in the ADCON2 register) while enabling noncontinuous operation and double-sampling (ADCONT = 0 in the ADCON0 register and ADDSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond '0b1' toward the value in the ADRPT register.

Work around

When operating the ADCC in Burst Average mode with double-sampling, enable continuous module operation (ADCONT = 1 in the ADCON0 register) and set the Stop-on-Interrupt bit (the ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in noncontinuous Burst Average mode can be operated with a single ADC conversion (ADDSEN = 0 in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.6. Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no precharge time along with the desired Acquisition time.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.7. ADC Conversion Acquisition Time in Sleep (ADCC)

Conversion during Sleep mode when ADACQ = 0 affects results on values in the upper half of the 10-bit range. The analog input is disconnected for 3-4 uS and the first bit of the result becomes zero.

Work around

Add five counts of ADACQ time.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.1.8. ADC Short in Pre-Charge State

During the pre-charge state, if the analog pin on which the ADC conversion is performed is selected to be an output (such as LATx or ADGRDx), there is a 20 ns short between pull-up/down and the external Low/High states, resulting in an inaccurate ADC conversion reading.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.2. Module: PIC18 Debug Executive

1.2.1. Data Write Match Breakpoints

If the data in a GPR location is modified using any arithmetic instruction like INCF, ADDWF, SETF, CLRF, etc., the data write match breakpoint does not work. It works with MOVF, which moves the data into the same memory location. See code examples below.

1.

```
MOVLB       0x00
CLRF        0x08
LOOP
INCF        0x08    ;Doesn't break when data
                    breakpoint set @ 0x08
                    with data match for 0xAA
GOTO LOOP
```

2.

```
MOVLB        0x00
MOVLW        0xAA
MOVF         0x08   ;Breaks when data
                    breakpoint set @ 0x08
```

```
                    with data match for 0xAA
GOTO LOOP
```

Work around

Use data write breakpoints without matching wherever possible.

Affected Silicon Revisions

A3	**A4**						
X							

1.2.2. Single Step Function Does Not Execute at SW Breakpoint

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.3. Module: PIC18 Core

1.3.1. TBLRD Requires NVMREG Value to Point to Appropriate Memory

The affected silicon revisions of the PIC18(L)F65/66K40 devices improperly require the NVMREG[1:0] bits in the NVMCON register to be set for TBLRD access of the various memory regions. The issue is most apparent in compiled C programs when the user defines a const type and the compiler uses `TBLRD` instructions to retrieve the data from Program Flash Memory (PFM). The issue is also apparent when the user defines an array in RAM for which the compiler creates start-up code, executed before main(), that uses `TBLRD` instructions to initialize RAM from PFM.

Work around

Assembly code:

Set the NVMREG[1:0] bits to select the appropriate memory region before executing `TBLRD` instructions.

C code:

Create an assembly file named powerup.as and include this file with the other files in the project. This file will change the NVMREG[1:0] bits to point to program Flash before any code is executed. Contents of the powerup.as file:

```
#include <xc.inc>
        GLOBAL    powerup, start
        PSECT     powerup, class=CODE, delta=1, reloc=2
powerup:
        BSF       NVMCON1, 7
        GOTO      start
        end
```

If there is a need to change the NVMREG[1:0] value to anything other than '`10`' and the Interrupt Service Routine uses constants or literal strings, then interrupts must be disabled before the change and restored to '`10`' before interrupts are enabled.

Affected Silicon Revisions

A3	**A4**						
X							

1.4. Module: Program Flash Memory (PFM)

1.4.1. Endurance of PFM is Lower than Specified

The Flash memory cell endurance specification (Parameter MEM30) is 1k cycles.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.4.2. PFM Back-to-Back Writes

When repetitive writes to nonvolatile memory (Program Flash Memory) are performed, they could result in write/erase failures at some locations. The issue is due to latent timing in the nonvolatile memory controller, which can cause the write instruction to fail under certain conditions.

Work around

To avoid the issue, it is recommended to wait an additional 100 µs after the NVMCON1.WR bit has been set, allowing for the last word to be loaded into the write buffer.

```
NVMCON2 = 0x55;
NVMCON2 = 0xAA;
NVMCON1bits.WR = 1;
__delay_us(100);

NVMCON1bits.WREN = 0;
```

Note: The `__delay_us()` function uses a `#define macro` definition. For the intrinsic `__delay_us()` function to work correctly, the value of the _XTAL_FREQ must be clearly defined. This macro is defined in the `device_config.h` file if the code is generated using MCC. The value of XTAL_FREQ is equal to the system clock frequency.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.5. Module: MSSP

1.5.1. SMBus 2.0 Voltage Level

The input low-voltage threshold level (V_{IL}) depends on V_{DD}, as follows:

V_{IL} = 0.7 for V_{DD} < 4V

V_{IL} = 0.8 for V_{DD} > 4V

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.5.2. MSSP SPI Client Mode

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF Transmit Shift Register (TSR) may become corrupted. The byte transmitted to the client cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM before an SFR read

Work around

Method 1 (Interrupt based using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise, check that $\overline{SS}$ == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When invoking the Interrupt Service Routine (ISR), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Method 2 (Bit polling based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.$\overline{SS}$ == 0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Once one of these two methods is complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.5.3. SMBus 2.0 Voltage Level

When using the MSSP to perform I^2C communication and the voltage for V_{DD} is above 3.0 Volts, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP is configured either for 7-bit or 10-bit addressing and in either Host or Client mode.

The issue occurs more frequently when using 10-bit addressing in Client mode and the lower address bits (A7-A0) are transmitted by the Host on the SDA line.

Work around

Do not exceed 3.0 Volts on V_{DD} when using an LF device.

Affected Silicon Revisions

A3	**A4**						
X							

1.6. Module: Electrical Specifications

1.6.1. Min V_{DD} Specification (LF Devices Only)

V_{DDMIN} specifications are changed for LF devices only at -40°C and 0°C as below.

V_{DDMIN} for -40°C to 0°C = 2.3V

V_{DDMIN} for 0°C to 25°C = 2.1V

Work around

None.

Affected Silicon Revisions

A3	**A4**						
	X						

1.6.2. FVR - Fixed Voltage Reference

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting) and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.6.3. ADC - Analog-to-Digital Converter

The table containing the Offset Error specification (AD04: EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSb.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.7. Module: Timer0

1.7.1. Synchronous Mode

Operation of TMR0 is incorrect when $F_{OSC}/4$ is used as the clock source.

Work around

Clearing the T0ASYNC bit in the T0CON1 register when TMR0 is configured to use $F_{OSC}/4$ may cause incorrect behavior. This issue is only valid when $F_{OSC}/4$ is used as the clock source.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.7.2. TMR0H Register Does Not Increment

Configuring Timer0 in 16-bit mode with $F_{OSC}/4$ and clearing the T0ASYNC bit in the T0CON1 register may result in the High-Byte register, TMR0H, failing to increment. This issue is valid only when $F_{OSC}/4$ is used as the clock source.

Work around

When using $F_{osc}/4$ as the Timer0 clock, set the T0ASYNC bit in the T0CON1 register to '1'.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.8. Module: Windowed Watchdog Timer (WWDT)

1.8.1. Window Operation in Doze Mode

When enabling the Windowed operation mode in Doze mode, a window violation error is issued even though the window is open and armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed operation mode in any mode other than Doze. If disabling Doze mode is not an option, use the WWDT module without enabling the window.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.9. Module: Nonvolatile Memory (NVM)

1.9.1. NVMERR

When a Reset is issued while an NVM high-voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.10. Module: Signal Measurement Timer (SMT)

1.10.1. Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work around
Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.11. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

1.11.1. Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around
Method 1:

Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2:

Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.12. Module: Capture/Compare/PWM Module (CCP)

1.12.1. Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around

None.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

1.13. Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.13.1. Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A3	**A4**						
X	**X**						

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001842**G**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. PPS Input Selection Register Details

Table 18-1 PPS Input Selection Register Details has been updated as follows:

Table 2-1. PPS Input Selection Register Details

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	PORT From Which Input Is Available							
Interrupt 0	INT0PPS	RB0	0x08	A	B	—	—	—	—	—	—
Interrupt 1	INT1PPS	RB1	0x09	—	B	C	—	—	—	—	—
Interrupt 2	INT2PPS	RB2	0x0A	—	B	—	D	—	—	—	—
Interrupt 3	INT3PPS	RB3	0x0B	—	B	—	—	E	—	—	—
Timer0 Clock	T0CKIPPS	RA4	0x04	A	B	—	—	—	—	—	—
Timer1 Clock	T1CKIPPS	RC0	0x10	**—**	—	C	D	—	—	—	—
Timer1 Gate	T1GPPS	RB5	0x0D	—	B	C	—	—	—	—	—
Timer3 Clock	T3CKIPPS	RB5	0x0D	—	B	C	—	—	—	—	—
Timer3 Gate	T3GPPS	RA5	0x05	A	—	C	—	—	—	—	—
Timer5 Clock	T5CKIPPS	RD1	0x19	**—**	—	—	D	E	—	—	—
Timer5 Gate	T5GPPS	RG4	0x34	—	**—**	—	—	E	—	G	—
Timer7 Clock	T7CKIPPS	RG4	0x34	**—**	—	—	—	E	—	G	—
Timer7 Gate	T7GPPS	RD1	0x19	—	**—**	—	D	E	—	—	—
Timer2 Clock	T2INPPS	RA1	0x01	A	—	C	—	—	—	—	—
Timer4 Clock	T4INPPS	RE4	0x24	—	B	—	—	E	—	—	—
Timer6 Clock	T6INPPS	RC1	0x11	—	B	C	—	—	—	—	—
Timer8 Clock	T8INPPS	RA0	0x00	A	—	—	—	E	—	—	—
ADC Conversion Trigger	ADACTPPS	RH1	0x39	—	**—**	C	—	—	—	—	H
CCP1	CCP1PPS	RE5	0x25	—	**—**	C	—	E	—	—	—
CCP2	CCP2PPS	RE4	0x24	—	**—**	C	—	E	—	—	—
CCP3	CCP3PPS	RE6	0x26	—	**—**	C	—	E	—	—	—
CCP4	CCP4PPS	RG3	0x33	—	**—**	—	—	E	—	G	—
CCP5	CCP5PPS	RG4	0x34	—	**—**	—	—	E	—	G	—
SMT1 Window	SMT1WINPPS	RE6	0x26	**—**	—	C	—	E	—	—	—
SMT1 Signal	SMT1SIGPPS	RE7	0x27	—	**—**	C	—	E	—	—	—
SMT2 Window	SMT2WINPPS	RG6	0x36	**—**	—	C	—	—	—	G	—
SMT2 Signal	SMT2SIGPPS	RG7	0x37	—	**—**	C	—	—	—	G	—
CWG	CWG1PPS	RC2	0x12	**—**	—	C	—	—	—	—	—
DSM Carrier Low	MDCARLPPS	RD3	0x1B	**—**	—	—	D	—	—	—	H
DSM Carrier High	MDCARHPPS	RD4	0x1C	**—**	—	—	D	—	—	—	H
DSM Source	MDSRCPPS	RD5	0x1D	**—**	—	—	D	—	—	—	H
MSSP1 Clock	SSP1CLKPPS	RC3	0x13	—	B	C	—	—	—	—	—
MSSP1 Data	SSP1DATPPS	RC4	0x14	—	B	C	—	—	—	—	—

Table 2-1. PPS Input Selection Register Details (continued)

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	PORT From Which Input Is Available							
MSSP1 Client Select	SSP1SSPPS	RF7	0x2F	—	B	—	—	—	—	F	—
MSSP2 Clock	SSP2CLKPPS	RD6	0x1E	—	B	—	D	—	—	—	—
MSSP2 Data	SSP2DATPPS	RD5	0x1D	—	B	—	D	—	—	—	—
MSSP2 Client Select	SSP2SSPPS	RD7	0x1F	—	B	—	D	—	—	—	—
EUSART1 Receive	RX1PPS	RC7	0x17	—	—	C	D	—	—	—	—
EUSART1 Clock	CK1PPS	RC6	0x16	—	—	C	D	—	—	—	—
EUSART2 Receive	RX2PPS	RG2	0x32	—	—	—	D	—	—	G	—
EUSART2 Clock	CK2PPS	RG1	0x31	—	—	—	D	—	—	G	—
EUSART3 Receive	RX3PPS	RE1	0x21	—	B	—	—	E	—	—	—
EUSART3 Clock	CK3PPS	RE0	0x20	—	B	—	—	E	—	—	—
EUSART4 Receive	RX4PPS	RC1	0x11	—	B	C	—	—	—	—	—
EUSART4 Clock	CK4PPS	RC0	0x10	—	B	C	—	—	—	—	—
EUSART5 Receive	RX5PPS	RE3	0x23	—	—	—	—	E	—	G	—
EUSART5 Clock	CK5PPS	RE2	0x22	—	—	—	—	E	—	G	—

2.2. Peripheral PPS Output Selection Codes

Table 18-3 Peripheral PPS Output Selection Codes has been updated as follows:

Table 2-2. Peripheral PPS Output Selection Codes

RxyPPS	Pin Rxy Output Source	PORT To Which Output Can Be Directed							
0x21	**ADGRDB**	—	—	C	—	—	—	—	H
0x20	**ADGRDA**	—	—	C	—	—	—	—	H
0x1F	**DSM1**	—	—	C	—	—	—	—	H
0x1E	**CLKR**	—	—	C	—	—	—	—	H
0x1D	TMR0	—	B	C	—	—	—	—	—
0x1C	MSSP2 (SDO/SDA)	—	B	—	D	—	—	—	—
0x1B	MSSP2 (SCK/SCL)	—	B	—	D	—	—	—	—
0x1A	MSSP1 (SDO/SDA)	—	B	C	—	—	—	—	—
0x19	MSSP1 (SCK/SCL)	—	B	C	—	—	—	—	—
0x18	**CMP3**	—	—	—	—	—	F	G	—
0x17	**CMP2**	—	—	—	—	—	F	G	—
0x16	**CMP1**	—	—	—	—	—	F	G	—
0x15	**EUSART5 (DT)**	—	—	—	—	E	—	G	—
0x14	**EUSART5 (TX/CK)**	—	—	—	—	E	—	G	—
0X13	EUSART4 (DT)	—	B	C	—	—	—	—	—
0x12	EUSART4 (TX/CK)	—	B	C	—	—	—	—	—
0x11	EUSART3 (DT)	—	B	—	—	E	—	—	—
0x10	EUSART3 (TX/CK)	—	B	—	—	E	—	—	—
0x0F	**EUSART2 (DT)**	—	—	—	D	—	—	G	—
0x0E	**EUSART2 (TX/CK)**	—	—	—	D	—	—	G	—
0x0D	**EUSART1 (DT)**	—	—	C	D	—	—	—	—
0x0C	**EUSART1(TX/CK)**	—	—	C	D	—	—	—	—
0x0B	**PWM7**	—	—	C	—	E	—	—	—
0x0A	**PWM6**	—	—	C	—	E	—	—	—

Table 2-2. Peripheral PPS Output Selection Codes (continued)

RxyPPS	Pin Rxy Output Source	PORT To Which Output Can Be Directed							
0x09	**CCP5**	—	—	—	—	E	—	G	—
0x08	**CCP4**	—	—	—	—	E	—	G	—
0x07	**CCP3**	—	—	C	—	E	—	—	—
0x06	**CCP2**	—	—	C	—	E	—	—	—
0x05	**CCP1**	—	—	C	—	E	—	—	—
0x04	**CWG1D**	—	—	—	—	E	—	G	—
0x03	**CWG1C**	—	—	C	—	E	—	—	—
0x02	**CWG1B**	—	—	—	—	E	—	G	—
0x01	**CWG1A**	—	—	C	—	E	—	—	—
0x00	LATxy	A	B	C	D	E	F	G	H

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
J	06/2025	Added Data Sheet Clarifications 2.1 (PPS Input Selection Register Details) and 2.2 (Peripheral PPS Output Selection Codes).
H	10/2024	Updated document format to most current version; silicon issues renumbered accordingly. Added silicon issue 1.7.2 (TMR0H Register Does Not Increment). Removed existing data sheet clarifications. Other minor editorial updates.
G	09/2022	Removed 2.1.2. Added 2.1.6, 2.1.7, 2.1.8, 2.4.2, 2.5.3, 2.10.1, 2.11.1, 2.12.1, 2.13.1. Removed all Data Sheet Clarifications except ADC offset Error should be -+3.0 LSb. Other minor editorial corrections.
F	03/2021	Added silicon revisions 2.1.5, 2.1.6, 2.5.2, 2.6.3 2.8.1 and 2.9.1. Data Sheet Clarifications: Added Module 3.2 (Pin Diagrams), Module 3.3 (Electrical Specifications), Module 3.4 (Analog-to-Digital Converter) and Module 3.5 (Capture/Compare/PWM (CCP) Module).
E	06/2018	Data Sheet Clarifications: Added Module 2: Pin Allocation Tables (ADC Channel Selection).
D	05/2018	Added Module 7: Electrical Specifications (FVR) and Module 8: Timer0. Data Sheet Clarifications: Added Module 1 (Core Features).
C	03/2017	Added Module 6: Electrical Specifications for LF Devices Only. Other minor corrections.
B	12/2016	Added modules 1.3. ADCRC Oscillator Operation in Sleep, 1.4. ADC Conversion with FVR, and 5. MSSP to the Silicon Errata Issues section. Other minor corrections.
A	09/2016	Initial release of this document.

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