VSC8664 VSC8574
Application Note
VSC8664 to VSC8574 Migration Design Guide

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.03

Revision 1.03 was published in December, 2010. Updated VSC8574 Block Diagram, Figure 2. Revised Maximum Power Requirements, Section 10. Revised REFCLK jitter requirements, Section 11.11. 2 Recovered Clocks, Section 11.6. SPI at 62.5MHz, Section 14.

1.2 Revision 1.02

Revision 1.02 was published in November, 2010. Updated REFCLK and 1588_diff_input_clk jitter requirements, Section 11.

1.3 Revision 1.01

Revision 1.01 was published in September, 2010. Corrected Section 13 pull-up to 1.0 V analog. Pin L4 and P4 changed to Reserved (NC in schematics), Section 2 and section 3.

1.4 Revision 1.0

Revision 1.0 was published in September, 2010. Enhanced details of power supply pin descriptions in section 2. Identified VSC8664 3.3 V supply pins that are analog and digital. 100 nF AC coupling cap on differential clock inputs.

1.5 Revision 0.51

Revision 0.51 was published in September, 2010. Basic and Enhanced Serial LED additions (Section 7.14) G15 (CLKOUT on VSC8664) changed back to NC on VSC8574 Changed Pin E13 to VDD25A power supply Renamed K16 to 1588_PPS_0 and N3 to 1588_PPS_1.

1.6 Revision 0.50

Revision 0.50 was published in August, 2010. Pins marked NC (No Connect) were changed to VSS (Ground).

1.7 Revision 0.49

Revision 0.49 was published in August, 2010. I/O on VSC8574 is 2.5 V with 3.3 V input tolerant PHYADD2, 3, 4 pin changes.

1.8 Revision 0.48

Revision 0.48 was published in August, 2010. Clarified FastLinkFail pin as K14 same on VSC8664 as VSC8574. Added Clock_Squelch_In to pin E15 to VSC8574 only.

Note: Updated 1588 Differential Clock interface in revision 0.47

1.9 Revision 0.47

Revision 1.0 was published in August, 2010. Added MDCIO & SPI FIFO Timestamp read estimates QSGMII drive strength design.

1.10 Revision 0.45

Revision 0.45 was published in August, 2010. Typo page 13 item 12 d should be bullet. Added LVDS resistors to 1588 Differential Clock.

1.11 Revision 0.44

Revision 0.44 was published in August, 2010. 2.5 V supply maximum current raised 550 ma. LVDDS changed to LVDS for 1588 Differential Input Clock

1.12 Revision 0.43

Revision 0.43 was published in July, 2010. Only 2 Recovered Clocks on VSC8574. Added VSC8574 unique Pin Descriptions. Fixed TDN_0, TDP_0 description.

1.13 Revision 0.41

Revision 0.41 was published in July, 2010. Fix Coma Mode comment in Section 4.1 and Section 5.5. Added multiple PPS outputs.

1.14 Revision 0.4

Revision 0.4 was published in July, 2010. Removed SPI 1, Added power estimates.

1.15 Revision 0.3

Revision 0.3 was published in June, 2010. Added SPI 1 and 2, 4 LEDS per PHY supported.

1.16 Revision 0.2

Revision 0.2 was published in June, 2010. It was the first publication of this document.

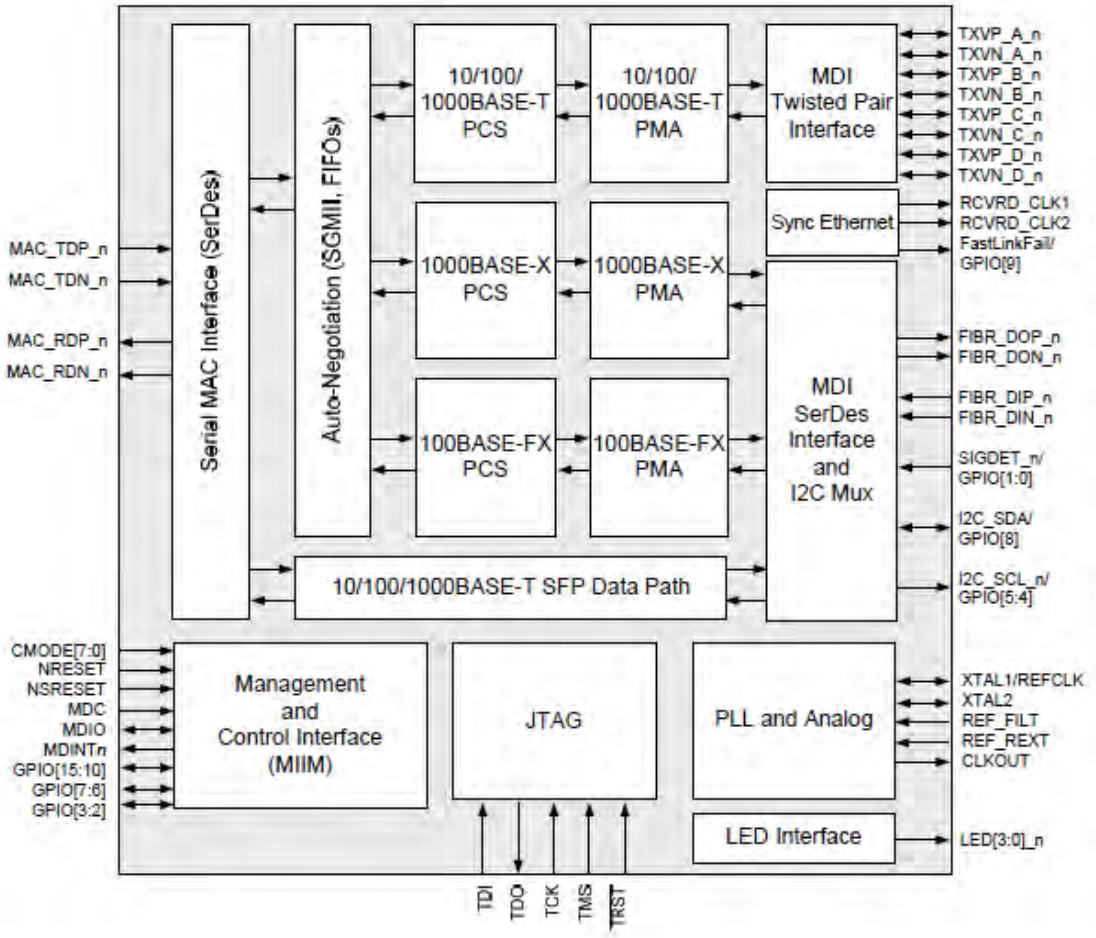
2 Introduction

This document highlights differences that should be considered when designing a system based on the VSC8664 that will migrate to the VSC8574. Changes in voltage supplies, pinout, registers, and other features are listed along with design recommendations.

Fundamental motivations behind migration to the VSC8574 include IEEE-1588v2 and IEEE 802.3az Energy Efficient Ethernet (EEE) support, and lower power.

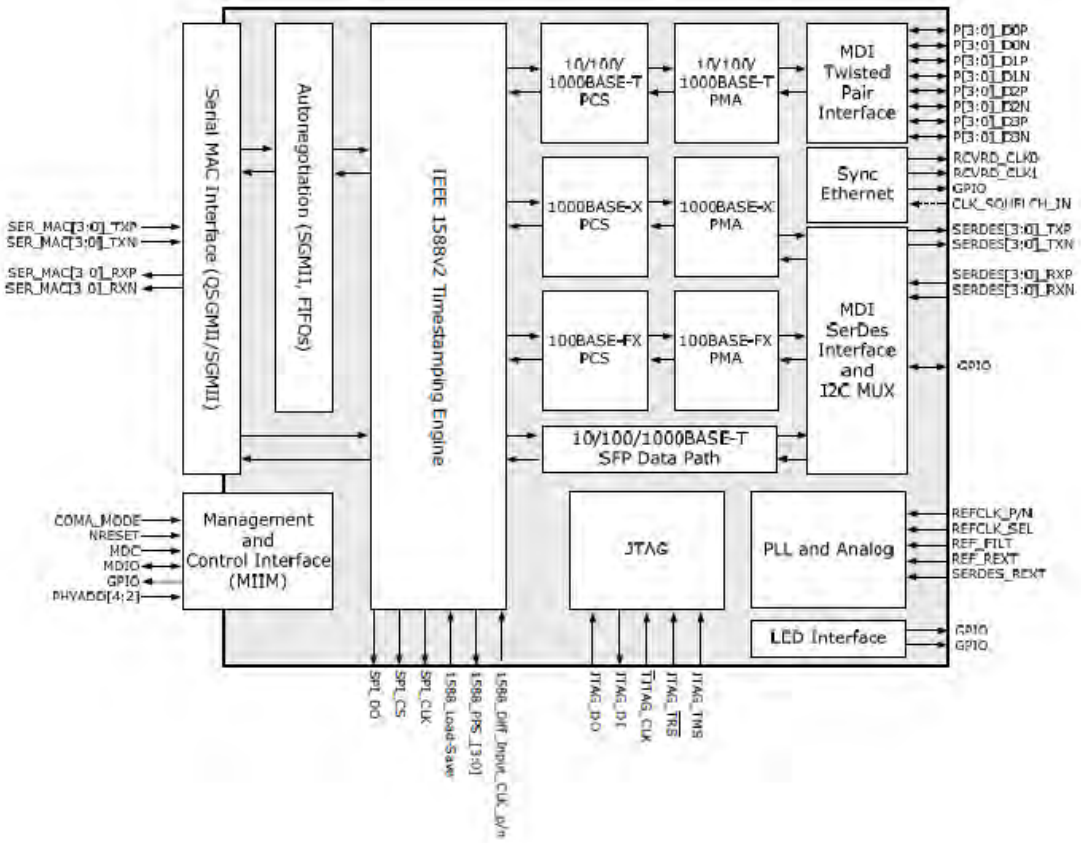
The following figure illustrates the VSC8664 block diagram.

Figure 1 • VSC8664 Block Diagram



The following figure illustrates the VS8574 block diagram.

Figure 2 • VSC8574 Block Diagram



3 Voltage Supply Changes

The following table lists the VSC8664 and VSC8574 voltage supply changes.

Table 1 • VSC8664 and VSC8574 Voltage Supply Changes

VSC8664 Supply	VSC8574 Supply
VDD12A (1.2 V Analog)	VDD1A (1.0 V Analog) Pins: C7, C8, C9, C13, P6, P7, P8, P9, P10, P11
VDD33A (3.3V Analog) **Note:** VSC8664 VDD33A pins require strong filtering with a C-L-C (Pi) filter or equivalent.	VDD25A (2.5 V Analog) Pins:C2, C4, C6, C11, C14, E4,E13*, P5, P12*,P13*
VDD12 (1.2 V digital)	VDD1 (1.0V Digital) Pins:E5,E12, F5, F12, G5, G12, H5, H12, J5, J12, K5,K12, L5,L12, M5, M12, N5, N12
VDDIO (Choose one: 1.8 V, 2.5 V, 3.3 V) and VDD33D (3.3 V digital)	VDD25 (2.5 V Digital) Pins: H13* M4,M13* P3
VSS (Ground)	VSS (Ground)
Same as VSC8574 plus L4 and P4	Pins: B1 and B16
	C3, C5, and C12
	D5, D6, D7, D8, D9, D10, D11, and D12
	E6, E7, E8, E9, E10 and E11
	F4, F6, F7,F8, F9, F10, and F11
	G6, G7, G8, G9, G10, and G11
	H6, H7, H8, H9, H10 and H11
	J6, J7, J8, J9, J10, J11, and J13
	K6, K7, K8, K9, K10, and K11
	L6, L7, L8, L9, L10, and L11
	M6, M7, M8 ,M9, M10, and M11
	N6, N7, N8, N9, N10, N11, and N13*
	P14*
	R1 and R16

*** Notes on voltage supply pin changes**

- E13 VSC8664 Reserved changes to VSC8574 2.5V analog
- P12 and P13 should be analog supplies on both the VSC8664 and VSC8574
- H13 and M13 should be digital supplies on both the VSC8664 and VSC8574
- N13 on VSC8664 is VSS on VSC8574 changes to SerDes_REXT_0
- P14 on VSC8664 is VSS on VSC8574 changes to SerDes_REXT_1

4 Pinout Changes

The following table lists the pinout changes.

Table 2 • Pinout Changes

VSC8664 Pin Name	VSC8574 Pin Name	Pin Location
CMODE0	PHYADD2 (Address Bit 2)	G13
CMODE1	PHYADD3 (Address Bit 3)	G14
CMODE2	PHYADD4 (Address Bit 4)	F14
GPIO10	1588_Load-Save	K15*
GPIO11	1588_PPS_0	K16*
GPIO14	1588_Diff_Input_CLK_p	J15
GPIO15	1588_Diff_Input_CLK_n	J16
NSRESET	Coma_Mode	L3
PLLMODE	Ref_CLK2 (0 = 25 MHz, 1 = 125 MHz)	E1
VSS	SerDes_REXT_0	N13
VSS	SerDes_REXT_1	P14
XTAL1/REFCLK	RefCLK_p	D1
XTAL2	RefCLK_n	C1
CLKOUT	NC	G15
CMODE3	VSS	F15
CMODE4	VSS	E14
CMODE5	VSS	D14
CMODE6	Clock_ Squelch_In	E15
CMODE7	SPI_CLK	E16
GPIO12	SPI_CS	J14*
GPIO13	SPI_Do	H14*
OSCEN	VSS	D2
THERMDA	VSS	H16
THERMDA	VSS	H15
RDN_0 (SGMII 0 Receive Negative)	RDN_0 (SGMII or QSGMII Receive Negative)	P 16
RDP_0 (SGMII 0 Receive Positive)	RDP_0 (SGMII or QSGMII Receive Positive)	P15
TDN_0 (SGMII 0 Transmit Negative)	TDN_0 (SGMII or QSGMII Transmit Negative)	N16
TDP_0 (SGMII 0 Transmit Positive)	TDP_0 (SGMII or QSGMII Transmit Positive)	N15
MDINT1	1588_PPS_1	N3
MDINT2	1588_PPS_1	N4
MDINT3	1 588_PPS_1	L2
Reserved	VDD25A	E13
VSS	NC	L4 and P4

* Can be configured as GPIO if not used as 1588 related function.

Notes:

- I/O on VSC8574 is 2.5 V and 3.3 V input tolerant
- Reserved are No Connection (NC)

5 VSC8664 Features Not In VSC8574

This section describes the VSC8664 features not present in VSC8574.

5.1 CMODE Initialization

Initialization will be done by SMI bus configuring registers.

5.2 Temperature Diode

VSC8574 has built-in temperature measurement and alarm system accessible through the SMI register interface.

5.3 CLKOUT

5.4 Crystal Clocking Support

6 VSC8574 Features Not In VSC8664

This section describes the VSC8574 features not present in VSC8664.

6.1 IEEE-1588V2

6.1.1 High bandwidth SPI for reading 1588 Timestamp FIFO

- 3 pin serial interface for reading 1588 Timestamp FIFOs of all 4 PHYs
- SPI will only have access to 1588 Timestamp FIFOs, no PHY registers access
- Typical usage is for high bandwidth 2-step operation
- Use SMI (MDC/MDIO) interface for PHY and other 1588 register access

Note: SMI also has access to 1588 Timestamp FIFOs

6.2 Energy Efficient Ethernet (EEE)

6.3 Temperature Measurement Management

6.4 Serial LED Enhancement

6.5 Coma_Mode for Initialization

Use Coma_Mode pin to hold PHYs in shutdown from power-on reset through configuration.

6.6 Dual End Ref_CLK

6.7 Recovered Clock input Pin For Clock Squelching

See Clock_Squelch_In for details.

7 Registers Difference Summary

1. Same, IEEE 802.3 Standard Registers (Base 0, Register 0-15)
   a. Except Register 3 Device Identification and Revision
   b. Except New Register 13 and 14 for EEE support
2. Same, Main Registers (Base 0, Register 16–30)
   a. Except Reg 3 operation modes
   b. Except No Reg 24 bit 3:1 100BT transmitter amplitude control
   c. Except No Reg 27 MAC control
   d. Except No Reg 30 bit 15-14, Copper Fiber Combine, Activity (TX/TX- RX) select
3. Same Extended Page (Register 31 == 1)
   a. Except No Reg 16 bit 11, 10, 7
   b. Except No Reg 17 bits 10-4 SerDes MAC/Media and Fast link Failure
   c. Except No Reg 19 bits 10- 5
   d. Except No Reg 20 bit 8 CLKOUT frequency select
   e. Except No Reg 28 SerDes MAC/Media status
4. New Extended Page 2 (Register 31 == 2)
   a. Register 16 CAT5 modes Amplitude control
   b. Register 17 EEE controls
5. New Extended Page 3 (Register 31==3)
   - MAC and Media SerDes controls moved to registers 16-29
6. General Purpose Register Page (Register 31==0x10)
   a. Different Reg 13
      Same Fast Link Fail select
      New MAC mode select
   b. Different Reg 14
   c. Different Reg 15
   d. Different Reg 19
   e. Different Reg 23 and 24
      SyncE recovered clock options and control different
   f. Different Reg 25
      New LED controls
   g. New Reg 26–29
      Temperature measurement
      Interrupt source status
7. New IEEE-1588v2 Register Control

   TBD

8 Functional Detail Comparison

1. Same operating modes
2. Same MAC interfaces functionally and electrically
3. Same SerDes media interface
4. Same CAT5 interface
5. Slightly different reference clock
   - VSC8574 single-ended not equivalent to VSC8664
     - VSC8664 uses OSCEN and PLLMODE for speed selection from a typical clock buffer for 25 MHz and 125 MHz
     - VSC8574 uses Ref_Clk2 for speed selection and clock input requires a resistor network from clock source for 25 MHz or 125 MHz
   - VSC8574 differential clock source recommended
   - No Crystal clocking support
6. Same AMS interface mode
7. Same tranformerless Ethernet
8. Same PoE
9. Same ActiPHY
10. Similar media recovered clock outputs (SyncE)
    - VSC8574 and VSC8664 have 2 recovered clock outputs
    - Register configuration of VSC8574 Recovered Clocks different
11. New Clock_Squelch_In added on VSC8574 Pin E15

    Input allows for remote control to squelch recovered clock put
12. Same fast Link failure indication on GPIO9/FastLinkFail pin K14
13. Slightly different serial management Interface

    VSC8664 has 4 MDINTs, VSC8574 will have 1 MDINT
14. Similar LED interface
    - Same Serial LED interface
      - Additional LD signal for start of frame indicator and Pulse for optional dimming applications.

Standard Pin Name	Serial LED Function	Pin
Basic Serial LED pins		
LED0_0	LED_Data	G1
LED0_1	LED_CLK	H1
Enhanced Serial LED pins		
LED0_0	LED_Data	G1
LED0_1	LED_CLK	H1
LED0_2	LED_LD	J1
LED0_3	LED_Pulse	K1

15. Different GPIO pins
16. Same and similar testing features
    - Same MAC and CAT5 Loopbacks
    - Different and new SerDes loopback
17. Similar JTAG interface
    - VSC8574 JTAG is 2.5 V that is 3.3 V tolerant
    - VSC8574 JTAG pins function the same as VSC8664

18. Different thermal diode
    - VSC8574 built in A/D temperature measurement through SMI interface
19. Different configuration
    - Numerous registers change, most and common stay the same
20. New IEEE-1588v2 Support
    - Required software initialization
    - Required additional clock input for time stamp
    - SPI interface support for reading 1588 time stamp FIFO
    - SMI (MDC/MDIO) supports reading 1588 time stamp FIFO and all 1588 and PHY registers
21. Different I/O on VSC8574 that is 2.5 V and 3.3 V input tolerant

9 Packaging

1. Same, 17mm × 17mm body, 1 mm pin pitch, 2mm maximum height, lead free PBGA
2. Same, pin number 256, BGA
3. Same temperature 2 ranges (0 °C to 90 °C, and –40 °C to 100 °C) offered

10 Errata

VSC8664 design considerations as published in the device datasheet do not apply to VSC8574. Separate lists of design considerations and errata will be maintained for the VSC8574.

11 Power Requirements

The VSC8574 estimated worse case current requirements applicable to power supply sizing are as follows.

- 1 volt supply current maximum estimate 1950 ma
- 2.5 volt supply current maximum estimate 500 ma

Note: This estimate is based upon maximum junction temperature, maximum voltage, highest power CAT5 connections, highest current drawing semiconductor process corner, above typical 1588 operation, and 125 MHz 1588 operation.

12 Recommendations

1. Do not use CMODE support for initialization on VSC8664 - only for PHY address. Use SMI registers for initialization.
2. Initialization on VSC8574 will be with SMI registers and Coma_Mode pin
3. Avoid using GPIOs on VSC8664 not supported on VSC8574
4. Design for software code space, initialization and monitoring update for EEE and IEEE-1588v2
5. Use Interrupts rather than polling
6. Design for 2 Recovered Clocks (SyncE) when upgrade
7. Consider VSC8574 Coma_Mode connections to multiple VSC8574s for synchronization
8. Design for JTAG 2.5 V for VSC8574
9. Do not use CLKOUT on VSC8664 since not available on VSC8574
10. Plan for thermal management on VSC8574 not supporting Thermal Diode found on the VSC8664
11. Use differential 125 MHz REF_CLK on VSC8574
    - Ref_CLK2 pulled high (2.5 V) for 125 MHz
    - PLL requirements are as follows.
      - 125 MHz
      - 100 ppm
      - SGMII only jitter 40ps RMS
      - QSGMII jitter 10ps RMS
12. 1588_Diff_Input_CLK_p&n
    - Use LVDS differential 125 MHz
    - Jitter 10ps RMS
    - 100 ppm for
    - See Section 14.
13. SMI (MDC/MDIO) bus maximum speed on both VSC8664 and VSC8574 is capable of 12.5 MHz. At 10 MHz roughly 20 µs to required read the 1588 Time Stamp used in 2-Step 1588. At 2 MHz the SMI bus can support roughly 10K reads per second and at 12.5 MHz approximately 45K. Actual system throughput can be effect by other devices and bus traffic needs.
14. Ref_CLK2 supports selection of 25 MHz and 125 MHz (pulled to VSS 25 MHz, pulled to 2.5 V 125 MHz). Recommend 125 MHz.
15. MDINTs on VSC8664 may be connected together and then pulled high or low. Software can check registers for PHY causing the interrupt. This is similar to VSC8574 single MDINT operation.
16. Note that if the VSC8574 is in EEE mode, there will be no communication from the link partner to recover the clock commonly used in SyncE applications. System design should take this into account.
17. Example VSC8574 Ref_CLK p/n (Pins D1 and C1) using Si5338b configured to: 2.5 V LVDS at 125 MHz (0.7 V swing, 1.2 V CM voltage). This is then AC-coupled using two 1 nF ceramic capacitors to Pins D1 and C1.
18. QSGMII drive strength designed to support 20 cm PCB (8 in.) + 1 connector (follows CEI 6G-SR).
19. I/O on VSC8574 is 2.5 V and 3.3 V input tolerant.
    FPGA and device connections should be considered that support 2.5 V.

13 VSC8574 Related Pin Descriptions

The following table lists the related pin descriptions.

Table 3 • Pin Descriptions

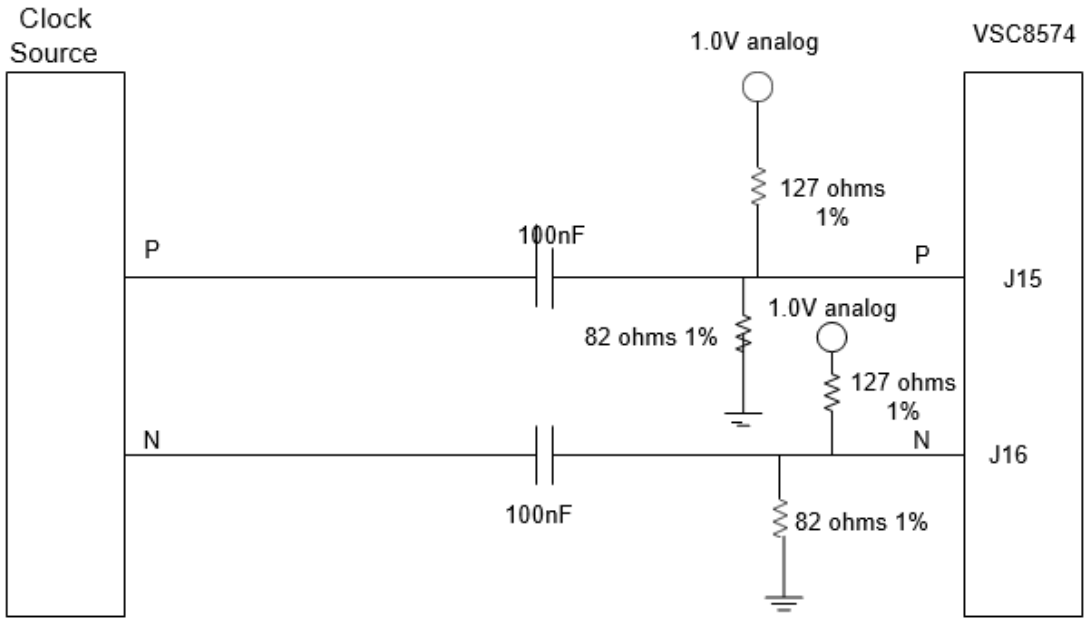
VSC8574 Pin Name	Pin Location	Description	Type
PHYADD4 (Address Bit 4)	G13	Device SMI Address Bit 4	Ipu
PHYADD3 (Address Bit 3)	G14	Device SMI Address Bit 3	Ipu
PHYADD2 (Address Bit 2)	F14	Device SMI Address Bit 2	Ipu
1588_Load-Save	K15	Input strobe all 4 PHYs Time Stamp Counters to use new time in register	Ipd
1588_PPS_[0-3]	K16	Pulse Per Second output selectable for PHY 0,1, 2, 3, and internal enable	Opd
1588_Diff_Input_CLK_p	J15	Differential Clock Input positive	I
1588_Diff_Input_CLK_n	J16	Differential Clock Input negative	I
Coma_Mode	L3	When this pin is asserted high, all PHYs are held in a powered down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven from separate chips.	Ipu
Ref_CLK2 (0=25MHz, 1=125MHz)	E1	Input to select speed of Ref_CLK. Pull high for 125 MHz. Pull low for 25 MHz	Ipd
SerDes_REXT_0	N13	SerDes bias pins (Connect to P14 with 620 Ω 1% resistor)	Abias
SerDes_REXT_1	P14	SerDes bias pins(Connect to N13 with 620 Ω 1% resistor)	Abias
RefCLK_p	D1	125MHz Reference Clock positive	I
RefCLK_n	C1	125MHz Reference Clock negative	I
SPI_CLK	E16	SPI Clock output	O
SPI_CSn	J14	SPI Enable output	O
SPI_Do	H14	SPI Data output	O
RDN_0	P16	PHY0 SGMII or QSGMII Receive Negative	Adiff
RDP_0	P15	PHY0 SGMII or QSGMII Receive Positive	Adff
TDN_0	N16	PHY0 SGMII or QSGMII Transmit Negative	Adiff
TDP_0	N15	PHY0 SGMII or QSGMII Transmit Positive	Adiff
1588_PPS_[0-3]	N3	Pulse Per Second output selectable for PHY 0, 1,2, 3, and internal enable	Opd
1588_PPS_2	N4	Pulse Per Second output for PHY 2	Opd
1588_PPS_3	L2	Pulse Per Second output for PHY 3	Opd
VDD1A, VDD1, VDD25A, VDD25, VSS	<Many>	See Section 3.0 for details	Power & Gnd

Note: See VSC8574 datasheet for Type description as well as RDx_0 and TDx_0 descriptions and connections.

14 VSC8574 1588 Differential Clock

The following figure illustrates the VSC8574 1588 differential clock.

Figure 3 • VSC8574 1588 Differential Clock



15 MDC/MDIO and SPI Timestamp FIFO Bandwidth Estimates

For 1588 2-step mode of operation the VSC8574 supports two methods for accessing the FIFO Timestamps: MDCIO or SPI. Most applications find that MDIO provides sufficient bandwidth to meet their applications needs.

- SPI at 62.5 MHz is approximately 1M timestamps/s
- MDIO at 2.5 MHz is approximately 8K timestamps/s
- MDIO at 12.5 MHz is approximately 40K timestamps/s

Note: For the bandwidth estimates an assumption was made that a read of a timestamp consists of 32 bit 1588 data and 16 bit frame identifier.

Note: Application design needs to take into account other devices or slaves loading on the bus bandwidth.

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