ENT-AN1266

Application Note

VSC8514 Design and Layout Guide

July 2018

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 of this document was published in July 2018. The following is a summary of the changes:

- A reference to advance quad flat no-lead package (aQFN) surface mount assembly guidelines was added. For more information, see References.
- The schematic review checklist was added. For more information, see Schematic Review Checklist.

1.2 Revision 1.0

Revision 1.0 was published in January 2014. It was the first publication of this document.

2 Introduction

This document provides useful guidelines for the design and layout of printed circuit boards utilizing the VSC8514 quad-port PHY or devices within the VSC8514 family. It is geared toward achieving first pass design success.

2.1 References

The following documents are recommended references for use during the board design process.

2.1.1 Microsemi Documents

- VSC8514 Datasheet
- ENT-AN0098 Magnetics Guide
- ENT-AN1198 Advance Quad Flat No-Lead Package (aQFN) Surface Mount Assembly Guidelines
- VSC8514 Orcad Library
- VSC8514EV Evaluation Board Schematic and Layout
- Ocelot Unmanaged Reference Design (VSC5634EV)

2.1.2 IEEE Standards

- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification

2.1.3 External Documents

- High Speed Digital Design, Author: Howard Johnson, Ph.D., ISBN 0-13-395724-1

3 Ground Considerations

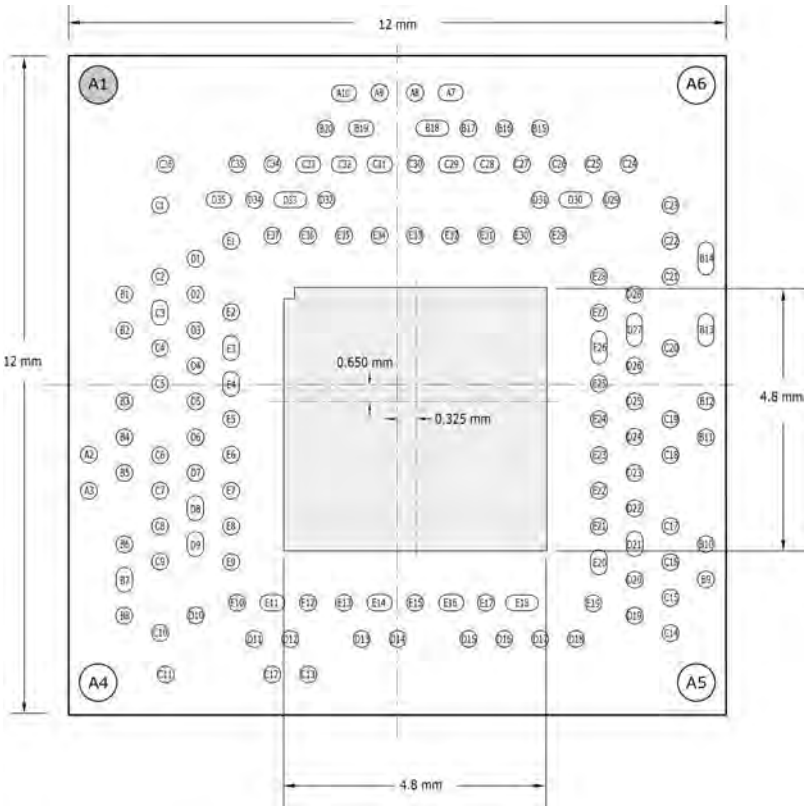
3.1 Exposed Ground Pad

The VSC8514 has an advanced quad-flat no-lead (aQFN) 138-pin package. The package has an exposed pad at the bottom of the device. The exposed pad provides a path for electrical grounding as well as a heat transfer point to the PCB and is sometimes referred to as the “thermal paddle” (for more information, see Power Considerations). The pad provides a very low inductive path to the ground plane, ideal for high-speed applications.

The center exposed pad on the PCB is 4.8 mm × 4.8 mm and is the same size as the exposed pad on the package. The exposed pad on the PCB is NSMD. The solder mask opening is 4.9 mm × 4.9 mm with 50 µm solder mask to metal clearance. To maximize thermal dissipation, there should not be any solder mask on the exposed pad of the PCB. Thermal vias are needed to conduct the heat from the paddle through the inner layers of the PCB. The thermal vias are 0.254 mm in diameter and arranged in a 4 × 4 matrix at 1.2 mm pitch. The recommended via plating is 1 oz copper. More thermal vias can be added if design rules allow. If via tenting is required, it is recommended that this be on the top side of the PCB.

The following illustration shows the PCB land pattern.

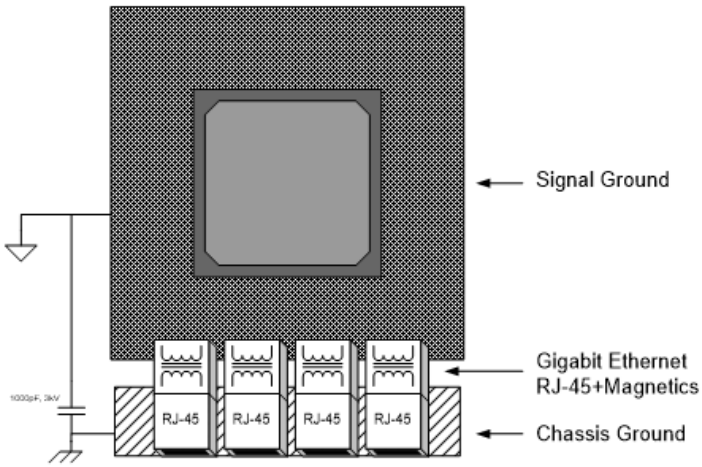
Figure 1 • PCB Land Pattern



3.2 Ground Isolation

To isolate the board from ESD events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, as seen in the following diagram, should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

Figure 2 • Ground Plane Layout

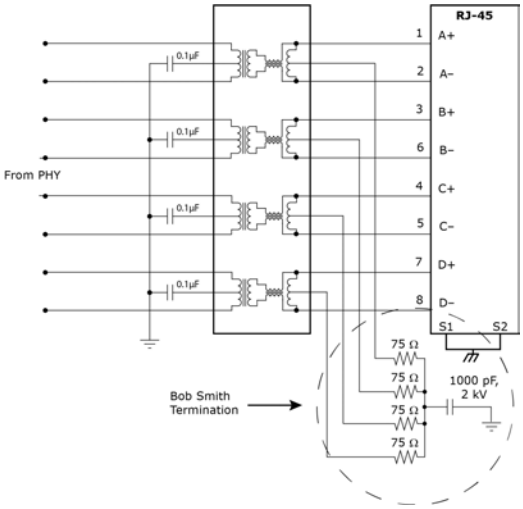


3.3 Bob Smith Termination

In addition, the Bob Smith termination impedance should be connected between the chassis ground and the cable-side center taps of the transformer module.

For additional information, see the Microsemi Magnetics Guide.

Figure 3 • Bob Smith Termination Diagram



4 Power Considerations

4.1 Power Supply Planes

The VSC8514 requires a minimum of two power rails, 2.5 V and 1.0 V. The filtered analog 1.0 V and 2.5 V supplies should not be shorted to any other digital supply at the package or PCB level. Refer to the datasheet for other power supply options. The most important PCB design and layout considerations as follows:

- Ensure the return plane is adjacent to the power plane (that is, without a signal layer in between)
- Ensure a single plane is used for voltage reference with splits for individual voltage rails within that plane. Attempt to maximize the area of each power rail split on the power plane based on corresponding via coordinates for each rail in order to maximize coupling between each voltage rail and the return plane.
- 1-oz copper cladding is recommended to minimize resistive drop while efficiently conducting heat away from the device

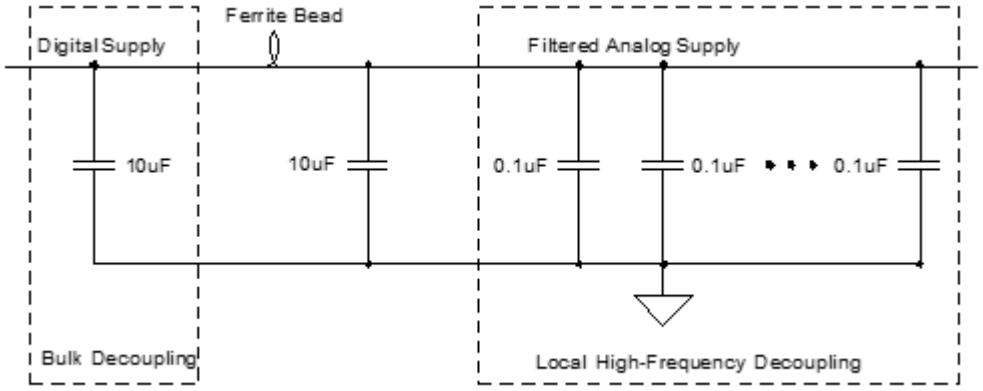
Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events such as CRC errors. Each of these supplies require the lowest resistive drop possible to the power pins of the device with properly placed local decoupling (as described in Bob Smith Termination). Given their low loss, we recommend using ferrite beads when possible over a series inductor filter, particularly for high-density or high-power devices. For the analog supply filtering, a ferrite bead is required (as described in Ground Isolation).

4.2 Analog Power Plane Filtering

A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with zero-Ω resistors once a thorough evaluation of system performance is completed.

Figure 4 • Filtered Supply Schematic



The beads should be chosen to have the following characteristics.

- Current rating of at least 150% of the maximum current of the associated power supply
- Minimum DC resistance (DCR) of less than 100 milliΩ is recommended
- Impedance of 80 Ω to 100 Ω at 100 MHz

The following beads are recommended:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar
- Murata BLM31PG121SN or other BLMxxPG parts

4.3 Local Decoupling

Bulk decoupling capacitors should be tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close to the VSC8514's power pins as possible for each and every power pin. Assuming that the VSC8514 is on the top side of a PCB board, the best location for local decoupling capacitors is on the bottom or underside of the PCB board, directly under the device.

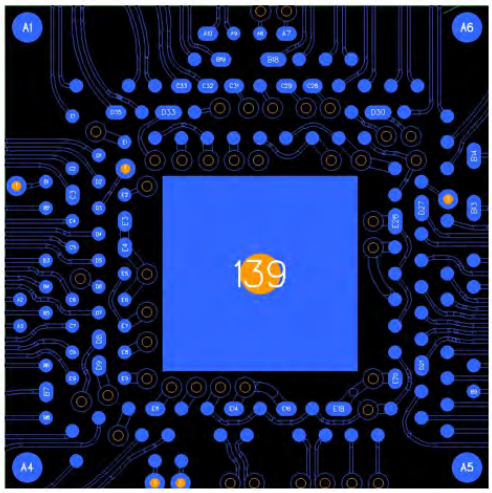
5 Package Considerations

5.1 aQFN Breakout Consideration

As an example of routing signals out from the PCB pads to their corresponding electrical vias connecting to other signal layers, the following figure shows a screenshot of the reference PCB signal breakout around the VSC8514 land area.

Please refer to the Advance Quad Flat No-lead Package (aQFN) Surface Mount Assembly Guidelines for additional information about PCB signal routing.

Figure 5 • 138-pin aQFN Breakout-Reference Layout

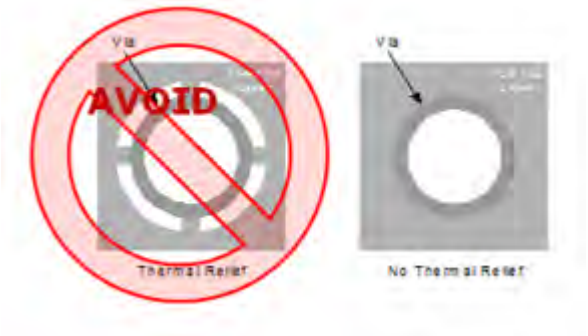


5.2 Thermal Considerations

For proper cooling, maximize the number of via connections to the ground plane for efficient thermal dissipation. Furthermore, for board stackups greater than four layers, additional ground planes will enhance thermal dissipation and signal integrity performance.

When connecting these thermal vias to ground planes, it is advisable to avoid thermal-relief connection traces shown on the left-hand side of the previous figure, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer (as shown on the right-hand-side of the previous figure).

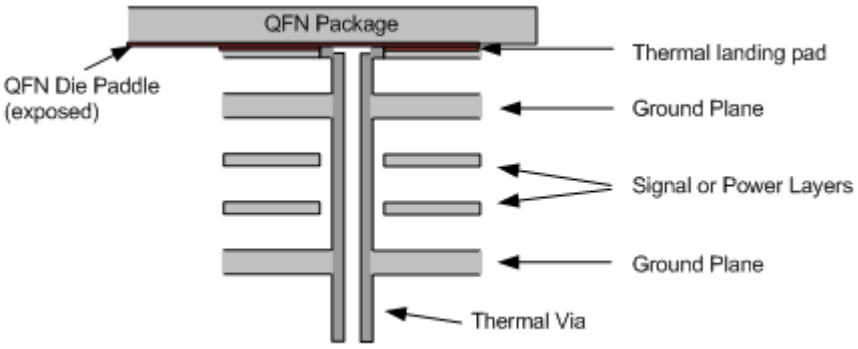
Figure 6 • Thermal Vias



In order to dissipate heat below the package, the PCB thermal vias should connect to the solid ground planes within the board (minimum 1-oz cladding is recommended). Refer to the previous figure for a simplistic profile of a thermal via within the PCB's thermal land area located below the aQFN paddle. Package I/O pins and their corresponding pads are not shown.

Also, steps should be taken to prevent solder wicking by the thermal vias. To avoid solder wicking by the thermal via during the soldering process, it is recommended the vias be fully copper plated. If copper plating does not plug the vias, thermal vias can be tented with solder mask on the top layer. Solder mask should be larger than the diameter of the via.

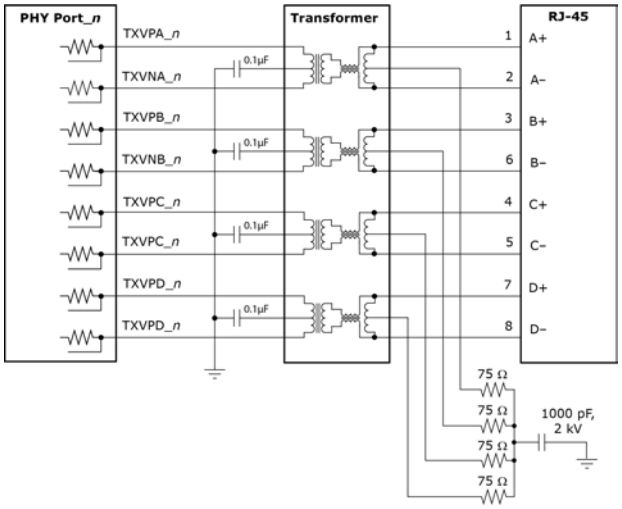
Figure 7 • Thermal Ground Plane Connection



6 Copper Interface

The following illustration shows a copper PHY media interface.

Figure 8 • Copper/CAT-5 Interface Diagram



6.1 Layout Considerations

The Pn_DxP and Pn_DxN pins interface to the external CAT5 cable and are organized in four differential pairs (x= 0, 1, 2, 3) for each PHY port. When routing these pairs on a PCB, the characteristics must match one of the following.

- Route each trace single ended with a characteristic impedance of 50 Ω referenced to ground
- Route each positive and negative trace on each port as differential pairs with 100 Ω characteristic differential impedance

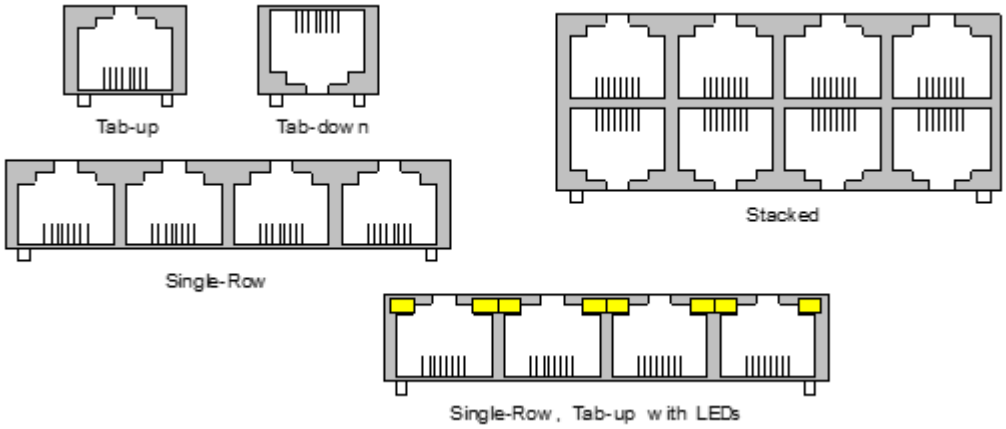
6.2 RJ-45 Connectors

For system designers, several options exist for the choice of RJ-45 connectors.

- Two-tab orientations: tab-up and tab-down
- For multi-port connectors, two orientations: stacked and single-row
- Single and bi-colored LEDs can be integrated into the connectors
- Magnetics can be integrated into the connectors

Most manufacturers can mix or match any combination of features. For example, LEDs may be added to any connector, or single-row multi-port configurations may be tab-up or tab-down. The exception is the stacked connector that contains both tab-up and tab-down orientations.

Figure 9 • RJ-45 Example Configurations

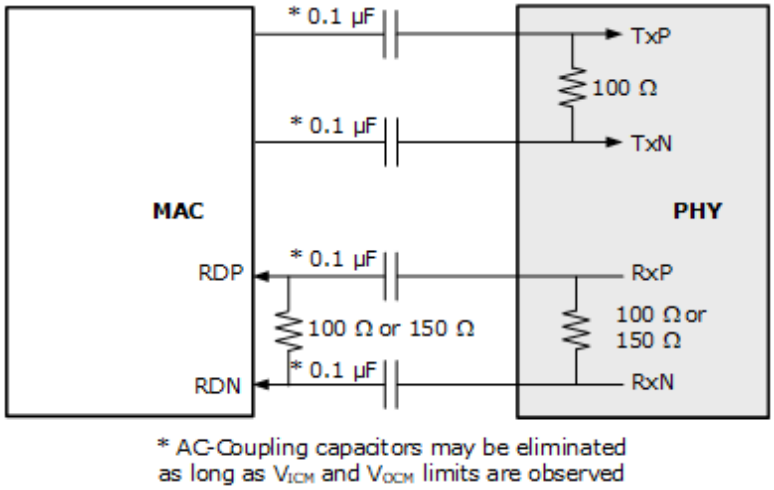


An additional consideration is the pinout of tab-up versus tab-down connectors. Due to the orientation, the pinouts of these two are reversed. While the VSC8514 will work equally well using either orientation, signal routing will be simplified with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation that allows ease of PCB routing.

7 SerDes Interface

The following illustration shows a typical MAC-to-PHY serial interface.

Figure 10 • Typical MAC-to-PHY Serial Interface



7.1 Design Rules

Best performance will result when SerDes traces are placed using the following design rules.

- Traces should be routed as 50 Ω (100 Ω differential) controlled impedance transmission lines (microstrip or stripline)
- Traces should be of equal length on each differential pair and port to minimize skew
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise
- Spacing between adjacent tracks equal to 5 times the ground-plane gap is recommended to reduce crosstalk between SerDes pairs. A minimum spacing of 3 times the ground-plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included nearby to attenuate any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks (2.5 GHz fundamental for QSGMII)

7.2 AC Coupling Capacitors

In general, SerDes interfaces require series AC coupling capacitors to prevent common mode voltages from interfering with transmit and receive operation. If the common mode input and output specifications for the system MAC and VSC8514 are compatible, then the AC coupling capacitors can be removed. For more information, please refer to the VSC8514 datasheet.

8 Miscellaneous Design Considerations

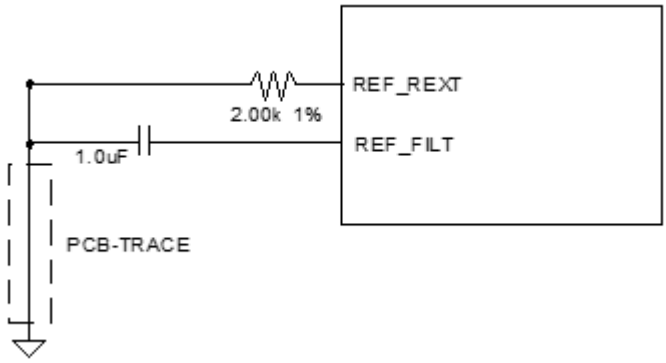
8.1 REF_FILT and REF_REXT Pins

For proper operation, the VSC8514 must generate an on-chip band gap reference voltage at the REF_FILT pin. For this, the following components are required for each VSC8514 in the system.

- 2.0 kΩ resistor, 1% tolerance, minimum 1/16 W
- 1 µF capacitor, 10% tolerance, NPO, X7R, or X5R ceramic materials are all acceptable

For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in the figure below. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8514.

Figure 11 • Voltage Reference Schematic



8.2 Clock Inputs

8.2.1 Device REFCLK

The device reference clock supports 125 MHz and 156.25 MHz frequencies in a differential, AC-coupled LVDS drive clock signal. For specific clock input requirements concerning the QSGMII interface, see QSGMII Operation and Clock Input Requirements.

The REFCLK_SEL[1:0] pins configure the reference clock frequency that is expected as input on the REFCLK input pins. REFCLK_SEL[1:0] have on-chip pull-down resistors setting the device default for 125 MHz. Refer to the datasheet for additional details.

8.2.2 QSGMII Operation and Clock Input Requirements

Because of the high-speed signaling present on the 5 Gbps line-rate QSGMII interface, particular care must be taken regarding the REFCLK_P/N inputs that ultimately determine symbol timing on the QSGMII. Please ensure the following conditions are met to provide as accurate a clock input as possible for QSGMII-based designs.

- Input 125 MHz reference clock signal with differential routing is used
- 1 V differential peak-peak amplitude is recommended
- The provided reference clock source has no greater than 1.2 ps of RMS phase jitter

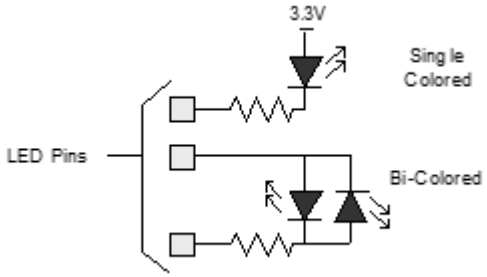
In order to simplify jitter tolerance analysis of reference clock components, it is easiest to verify that the clock oscillator's phase noise integrated over the 10 kHz–20 MHz band (with respect to fundamental—for example, dBc/Hz) is no greater than 1.2 picoseconds single-σ (RMS). Crystal oscillator vendors (including Microsemi) provide application notes showing this conversion in detail or will provide the integrated values directly.

8.3 LEDs

The LED interface supports the following configuration: direct drive, basic serial LED mode, and enhanced serial LED mode. Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. Additional LED modes may be enabled on the LED0 pin whenever register 19E1, bits 15 to 12 are set to 1. See the VSC8514 datasheet for information on specific LED settings, including the default drive state as described by the LED interface's functional description.

For direct-drive, each VSC8514 PHY port can support up to four single-colored LEDs or two bi-colored LEDs. Each LED pin sinks current when an indication is present and de-asserts when inactive. By design, each LED pin can also drive current when not active. This is very useful in the case for bi-colored LEDs. Each LED pin in the VSC8514 can be designated to indicate any of the possible LED status signals, further simplifying the overall design.

Figure 12 • LED Configurations



9 Schematic Review Checklist

The following checklist should be reviewed to ensure proper design connectivity as well as to ensure all considerations are properly followed.

9.1 Generic Considerations

If a board design is based on a Microsemi reference design and use of Microsemi software is planned, perform the following.

- Keep a log of changes made to the Microsemi design, such as port number and PHY addresses.
- Retain the reference board's use of GPIO (parallel and serial) whenever possible.

To reduce emissions, follow these steps.

- Use distributed reference clock signals as low-voltage swing (for example, 400 mVpp) instead of full swing (3.3 V).
- Placing AC-coupling capacitors on QSGMII signals between switch and PHY devices or PHY devices and SFP modules may not be required, as SFPs have built-in capacitors and some Microsemi switch and PHY combinations are DC-compatible and so can be connected directly.
- Small capacitors on 1000Base-T signals sometimes help with emissions. However, beware of impacts to IEEE template compliance.

9.1.1 Reference Clock

The following table describes the reference clock.

Table 1 • Reference Clock

Check	Signal Name	Connectivity Comments
	REFCLK_P/N	Ensure clock driver meets jitter performance requirements. Ensure differential clock driver common mode voltage requirements are met or use AC-coupling capacitors. **Note**: Refclk inputs are self-biased to 1 V (VDDA) with an internal termination, so no external biasing or termination components are needed.
	RCVRD_CLK[1:2]	If used, place an external series termination resistor, ~40 Ω.
	REFCLK_SEL[1:0]	00’b= 125M, 10’b= 156.25M. Internal PD.
	CLK_SQUELCH_IN	Internal pull-down.

9.1.2 Twisted Pair

The following table describes the twisted pair.

Table 2 • Twisted Pair

Check	Signal Name	Connectivity Comments
	P[3:0]_D[3:0]P, P[3:0]_D[3:0]N	The naming convention used is such that [3:0] index on P is the port identification and [3:0] index on D is the differential pair identification. Routed as differential 100 Ω impedance or single-ended 50 Ω impedance reference to GND. Differential pair traces should be kept the same length. **Note**: The correct RJ-45 connectivity to support 1 GbE includes pairs (1, 2, 3, 4, 5, 6, 7, 8). Optional TVS may be acceptable, expect junction capacitance < 3 pF

Refer to ENT-AN0098 Magnetics Guide for more information about the following topics.

- CMC on the line side

- PHY-side center taps individually AC coupled to ground
- Individual Bob Smith termination for the four channels
- Return loss: 18 dB for 1 MHz to 40 MHz and 12–20 log(f/80)dB over 40 MHz to 100 MHz
- The importance of the flatness of frequency response from 1 MHz to 40 MHz
- Turn ratio tolerance of ±3% or better
- Insertion loss ~1 dB
- CMNR: 35 dB or better
- Crosstalk: 35 dB or better

9.1.3 MAC Interface

The following table describes the MAC Interface.

Table 3 • MAC Interface

Check	Signal Name	Connectivity Comments
	TDP/N_0	QSGMII input. Use AC coupling for DC level adjustment and EMI suppression. Differential intra-pair skew must be kept to no more than 5 ps. Ensure RX to TX spacing to minimize crosstalk.
	RDP/N_0	QSGMII output. Use AC coupling for DC level adjustment and EMI suppression. Differential intra-pair skew must be kept to no more than 5 ps. Ensure RX to TX spacing to minimize crosstalk.
	SerDes_Rext [1:0]	Bias resistor of 620 ±1% in between.

9.1.4 JTAG Interface

The following table describes the JTAG Interface.

Table 4 • JTAG Interface

Check	Signal Name	Connectivity Comments
	TCK, TDI, TDO, TMS	May be left floating if unused.
	TRST	Internal PU. Must be pulled/driven low during normal operation.

9.1.5 SMI Interface

The following table describes the SMI Interface.

Table 5 • SMI Interface

Check	Signal Name	Connectivity Comments
	MDC	If not point-to-point, lay out as a daisy chain rather than branching (which results in stubs). Confirm voltage swing compatibility with station master and other slaves on the bus.
	MDIO	If not point-to-point, lay out as a daisy chain rather than branching (which results in stubs). Confirm voltage swing compatibility with station master and other slaves on the bus.
	MDINT	Open-drain output, which requires a pull-up resistor to the proper supply.
	NRESET	Internal pull-down. Only de-assert NRESET after all power supplies and reference clock are stable.
	PHYADD [4:2]	Internal pull-down.

9.1.6 Miscellaneous Signals

The following table describes the miscellaneous signals.

Table 6 • Miscellaneous Signals

Check	Signal Name	Connectivity Comments
	THERMDA	Add a test pad and optional 0 Ω to GND if unused.
	THERMDC_VSS	Add a test pad if unused.
	REF_REXT REF_FILT	REF_REXT must use be 2.0K ± 1% resistor and REF_FILT must use a 1 µF capacitor. The two components must join at a single common point connected to the analog ground plane (see REF_FILT/REF_REXT Pins).
	COMA_MODE	Internal pull-up. If not planned to be configured through software, this signal must be pulled-down to enable PHY operation.
	LED[0:3]_PHY[0:3]	If unused, leave floating. LED pins should have a low series resistance.
	RESERVED	Leave unconnected.

9.1.7 Power Pins

The following table describes the power pins.

Table 7 • Power Pins

Check	Signal Name	Connectivity Comments
	VDD1A	1.0 V analog power supply requiring additional PCB power supply filtering.
	VDD1	1.0 V digital core power supply.
	VDD25A	2.5 V analog power supply requiring additional PCB power supply filtering.
	VDD25	2.5 V general digital power supply.
	VDDMDIO	1.2 V or 2.5 V power supply for MDC, MDIO, and MDINT.
	VSS_CASE	Common device ground. For proper decoupling and filtering details, see Ground Isolation.

10 Bringing Up the Device

10.1 Reset Sequence

Assuming that all power supplies (1.0 V and 2.5 V) are stable, the JTAG reset can be de-asserted 100 ns after REFCLK is stable. Hardware (NRESET) reset should not be de-asserted until at least 100 ns after de-asserting JTAG reset.

Note: Because the value of the REFCLK_SEL pin is latched on the rising edge of the NRESET pin, it is required that the 2.5 V supply be stable before the rising edge of NRESET. NRESET should never be tied directly to logic high on the PCB because the VSC8514 will behave unpredictably if it is done. If the design cannot control the NRESET pin, then a small RC circuit must be added to this signal to provide the necessary delay.

The following events occur in this order when the VSC8514 is brought out of reset, which is triggered by a low-to-high transition of the NRESET pin.

1. Values for the REFCLK_SEL pins are immediately latched asynchronously.
2. Approximately 100 milliseconds after de-assert of NRESET, the analog reference voltages and current stabilize. This is seen on the REF_REXT and REF_FILT pins.
3. Once a stable analog reference is established, the internal PLL will require 110 microseconds to lock. The PLL provides the device with its internal clocks.
4. With a locked PLL, the analog-to-digital converter (ADC) blocks require 4.9 milliseconds to calibrate.
5. Once the ADC is calibrated, the device is in normal operation and its MDC and MDIO pins are operational.

10.2 Application Programming Interface and Initial Configuration

The first API version to recognize the VSC8514 is v4.40 of the Unified PHY API. However, customers should use the latest revision of the Microsemi Unified PHY API to incorporate the most recent initialization scripts (if any) for the VSC8514.

For an initial device bring up, the VSC8514 device can be configured by setting internal memory registers using the management interface. Please refer to the Configuration section of the datasheet for details regarding the configuration procedure for initial operation.

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VPPD-03694