ENT-AN1072

Application Note

Distributed Transparent Clock over Microwave Application

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a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

In revision 2.0 of this document, formatting was updated.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

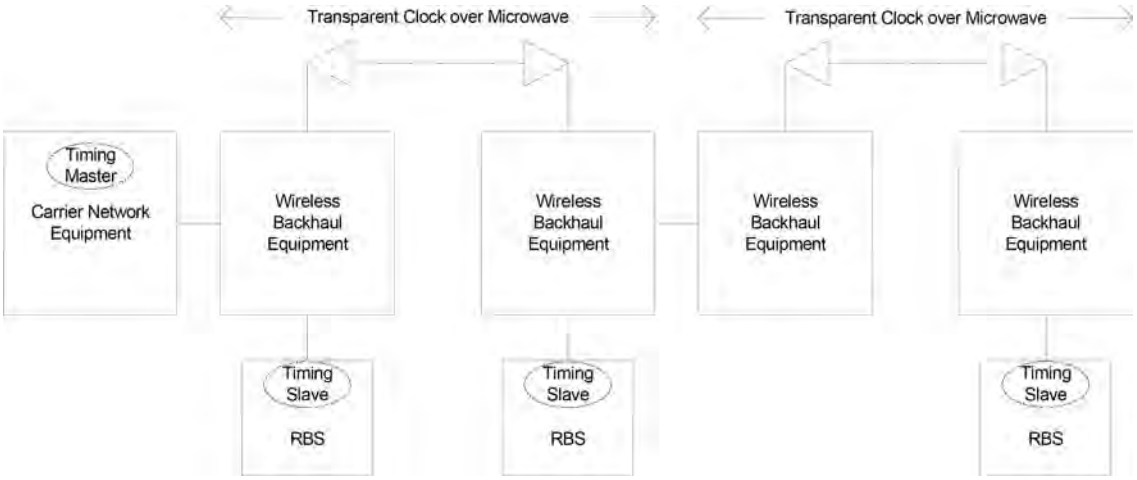
This application note describes how to implement IEEE 1588 Distributed Transparent Clocks using Microsemi's VeriTime™ IEEE 1588 technology, available in several Carrier Ethernet switch engines and PHY devices.

The IEEE 1588v2 (PTP) standard is used to accurately transfer time/phase information over packet networks and is often used in Carrier Ethernet networks to synchronize mobile base stations. Depending on the mobile technology, the time synchronization requirement to the base station is between 1.5 us to below 500 ns.

It is becoming common to use microwave and millimeter wave links to connect to the base stations. The use of PTP as a method for accurate distribution of time/phase is problematic as the PTP protocol relies on a fixed and symmetric latency between Carrier Ethernet PTP nodes. The microwave links are used to interconnect between Carrier Ethernet equipment and produces packet delay variation, PDV (due to buffering), disassembly/reassembly into fixed blocks of data, and dynamic changes in modulation /bandwidth (due to weather changes). The bandwidth/latency is different in the upstream and downstream directions. The solution to this problem is to implement a "Distributed Transparent Clock" in the microwave equipment using Microsemi Carrier Ethernet switches and/or 1588 PHYs (patent pending).

The PTP standard specifies the operation of a transparent clock as a piece of equipment that measures the residence time (the time that a frame is inside the equipment, from ingress to egress) of a PTP frame and adds this value to a field in the PTP frame called the correction field. When implementing Distributed Transparent Clock over a microwave link, it makes the complete microwave link look like one transparent clock, from the Carrier Ethernet microwave link port input to the Carrier Ethernet microwave link port output on the other end. As seen in the following illustration.

Figure 1 • Microwave Distributed Transparent Clock



A 1-step, end-to-end PTP transparent clock measures the residence time of Sync and Delay_req frames, and adds the residence time to the correction field of each frame. This requires the residence time of each PTP frame be measured accurately and dedicated logic can update the correction field of the frame on the port and ensure that the frame is still valid (correct CRC and IP/UDP checksum). Microsemi has developed 1588 PHYs as well as Carrier Ethernet switches that are able to detect the PTP frames and perform the required operations on the frames in hardware.

A transparent clock does not need to know the absolute time, but the timestamping logic on each port needs to agree on the time so the residence time can be correctly calculated. This can easily be solved when a transparent clock is a single piece of equipment. When implementing a Distributed Transparent Clock, where two (or more) Carrier Ethernet ports are located in different physical locations, it becomes more difficult to synchronize the ports.

3 VeriTime Devices

A number of different Microsemi devices can be used to implement a Distributed Transparent Clock.

3.1 IEEE 1588 PHYs

The IEEE 1588 PHYs from Microsemi support all the required frame analysis and operations to implement a Distributed Transparent Clock. The VSC8574 is a quad 1G dual media Ethernet PHY that supports 10/100/1000BASE-T as well as 1G/100 Mbit fiber SFPs. If 10G links are needed, the VSC8488-15 is a dual 10GE PHY that supports the same PTP operations as the VSC8574.

When configured for TC operation the PHY detects the PTP Sync and Delay_req frames and inserts the ingress timestamp inside the PTP frame on ingress. The egress side, the ingress timestamp is extracted from the frame and the correction field is updated with the residence time of the frame. The CRC and IP /UDP (both IPv4/UDP and IPv6/UDP are supported) checksums are updated after each modification, so the frames are valid and can be processed inside the equipment.

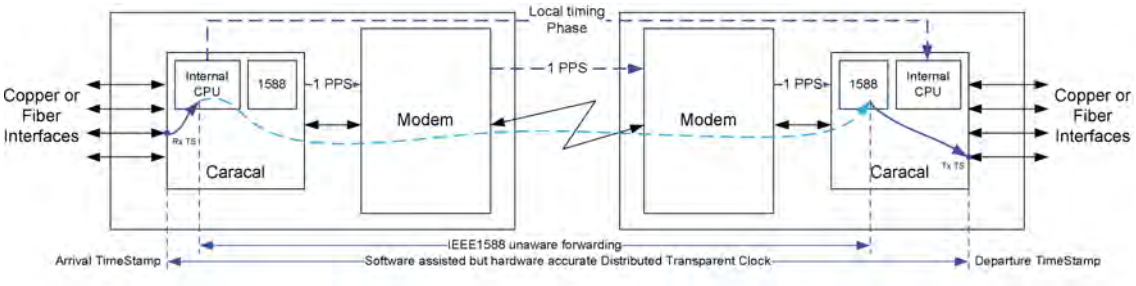
The PTP timer in the PHY is driven by either the normal PHY reference clock or a dedicated 1588 clock input. For TC operation, use the normal PHY reference clock. It is recommended to use SyncE (if supported over the microwave link) to ensure that the PTP timers in the PHYs, at each end of the microwave link, progress at the same rate.

The time in the PHY is loaded by writing a set of registers with a time, this time can then be loaded by a synchronization pulse on a L/S pin. The PHYs also has the ability to provide a 1 PPS synchronization output signal every time the internal time in the PHY reaches a one second boundary.

3.2 VSC7428–Caracal

The VSC7428 is an 11-port Gigabit Carrier Ethernet switch with eight integrated 10/100/1000BASE-T or 1G/100 Mbit SFP ports, two 2.5G/1G/100 Mbit SGMII ports, and an internal MIPS24K CPU system. The switch supports both boundary clock and transparent clock operation, but uses an internal timestamp transfer mechanism between the internal ports. It is required that the PTP frames are reformatted by the internal CPU before being transmitted over the microwave link. This is to reformat the frames to insert the ingress timestamp into the PTP frame towards the microwave link and to extract the ingress timestamp from PTP frames from the microwave link. This ensures interoperability between different Microsemi transparent clock solutions in the two ends of a microwave link.

Figure 2 • Caracal Based Solution



The internal CPU is used to run a Microsemi time sync protocol between the two ends of the microwave link, see Synchronization Requirements.

3.2.1 Life of a PTP Frame

The following describes what happens to a PTP Sync or Delay_req frame when passing through a Distributed Transparent Clock using Caracal.

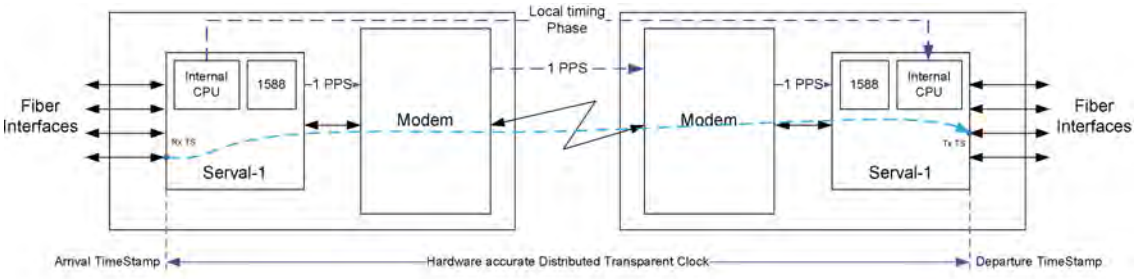
1. A PTP Sync or Delay_req packet arrives on an ingress port of a Caracal device and receives a hardware time stamp.

2. The time stamped 1588 packet is redirected to the local embedded processor.
3. The local processor reformats the 1588 packet, including the arrival timestamp, and sends the packet in-band to the embedded processor at the other Caracal across the microwave link. The format used is the same format as the 1588 PHYs (for instance, reserved bytes) to allow interoperability among all Microsemi based solutions.
4. This in-band packet is not treated as a 1588 sync packet by the egress port nor ingress port along the in-band packet transmission path.
5. At the far-end Caracal, the frame is redirected to the CPU.
6. The receiving processor reformats the in-band packet to a standard 1588 packet with the ingress timestamp in place and sends the 1588 packet to the egress port.
7. The egress port performs a 1588 TC operation on the 1588 packet with hardware time stamping accuracy.

3.3 VSC7418 Serval-1

VSC7418 Serval-1, is an 11-port Gigabit Carrier Ethernet Switch with nine 1G/100 Mbit SFP/SGMII ports and two 2.5G/1G/100 Mbit SFP/SGMII ports. The Distributed Transparent Clock operation is the same as Caracal, but Serval-1 supports the reformatting between the internal switch format and the 1588 PHY format in hardware, so that the forwarding and reformatting of frames does not need any CPU support. If 10/100/1000BASE-T ports are needed, a VSC8574 1588 PHY can be placed in front of the VSC7418 switch.

Figure 3 • Serval-1 Based Solution



4 Synchronization Requirements

The time stamping devices at each end of the link need to be synchronized so they have the same time and progress at the same rate. Any offset between the two devices produces a residence time error equal to this offset, resulting in a time offset among PTP slaves communicating though this Distributed Transparent Clock. Therefore, it is important to ensure the two ends are synchronized as accurately as possible.

4.1 Frequency Synchronization—SyncE

Most microwave systems support the transfer of frequency using SyncE. This feature can be used to keep the time progressing at the same rate, at the two ends of the microwave link. It requires the clocks that drive the IEEE 1588 timers, at both ends of the link, to be driven from the SyncE DPLL outputs, and the SyncE clock is always in lock. The normal SyncE output clock of a SyncE DPLL can cause significant wander on the output clock during holdover, this wander will directly result in time drift in the IEEE 1588 timer driven by this clock.

If the system will experience SyncE holdover (either true holdover caused by changing direction of a ring, or short holdover periods caused by changes to the modulation scheme of the microwave link) it is important that the frequency reference to the SyncE DPLL is able to provide a low wander clock (low MTIE value for the period of holdover). If the IEEE 1588 timer at one end of the microwave link drifts relative to the IEEE 1588 timer at the other end of the link during holdover, it will result in incorrect residence time calculations equal to the size of the phase drift. This error will not be corrected until the next sync pulse of the system. If the system will experience SyncE holdover, it is recommended to use a high quality oscillator that is designed for IEEE 1588 applications, OCXO or TCXO based.

4.1.1 Frequency Syntonization

If SyncE is not supported over the microwave link, frequency syntonization must be used. Frequency syntonization is done by comparing the difference in time between a time master and slave over a long period, then calculating the frequency difference between the two systems. This frequency difference is then taken into account when performing IEEE 1588 operations.

The IEEE 1588 timers in Microsemi devices support frequency syntonization by programming a register that adds or subtracts 1 ns from the IEEE 1588 time, either at programmable intervals or when triggered by a software register write. This allows the IEEE 1588 slave to run off a local reference clock that has a fixed frequency offset to the IEEE 1588 master. When using frequency syntonization in IEEE 1588 applications the local oscillators must be very stable. It is recommended to use a high quality oscillator that is designed for IEEE 1588 applications, often OCXO based.

4.2 Phase Synchronization

The phase synchronization of the time can be done in many different ways depending on the design of the modem part of the microwave link. The following sections will describe the three different methods.

4.2.1 Layer 1 Synchronization Pulse

If the modem can provide a synchronization pulse to the Microsemi switch or PHY in both ends of the microwave link, then this method can be the most accurate synchronization method. The synchronization pulses, in both ends, do not need to be aligned as long as the phase difference is known.

One example solution would be that one end of the microwave link is a master end that generates and transmits a special sync code towards the other end at specific intervals (for instance, every 1.000000000 seconds). At the same time the modem generates a Sync signal on a pin connected to the Microsemi switch/PHY. This sync code is received at the modem at the other end of the microwave link (slave end) where it will generate a Sync pulse to the Microsemi switch/PHY. The slave end switch/PHY will receive this Sync pulse some time later than the master end switch/PHY. The time will be known, as it depends on the distance of the microwave links (must be manually configured) and the encoding /decoding time of the modems. It is also possible to let the slave end do an immediate reply towards the master end, then the master can measure the round-trip delay and report it to the software. This will allow easier installation as the distance between the microwave equipment does not need to be configured.

> ⚠ This method requires the spacing between sync pulses to be very accurate.

If the microwave link already has some kind of phase synchronization, then this can be used as a basis for generating sync pulses towards the Microsemi switches/PHY.

It is also possible to let the master end switch/PHY generate a 1 PPS to the master end modem and let this pulse propagate to the other end as described previously.

Figure 4 • SyncE and Sync Pulse Connections Using Serval or Caracal

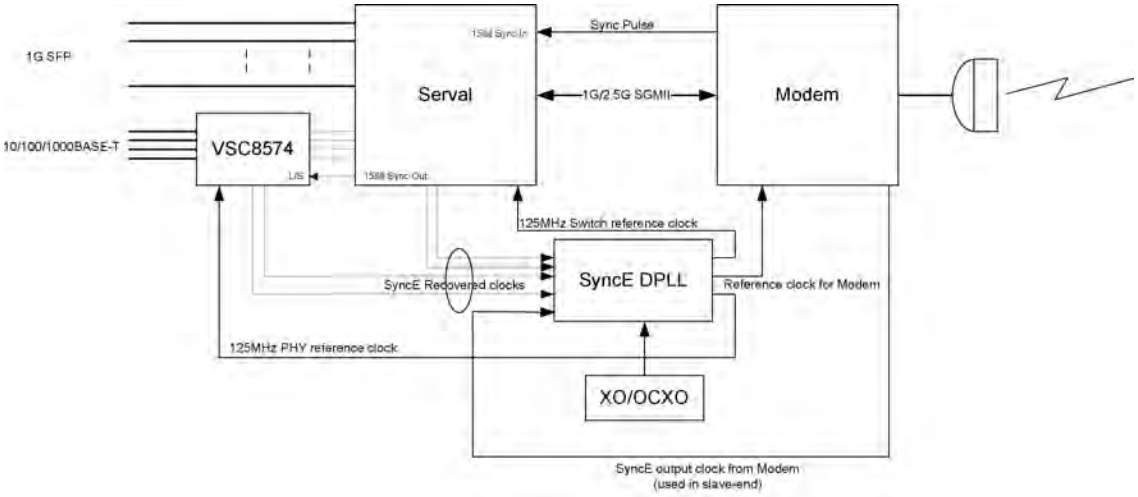
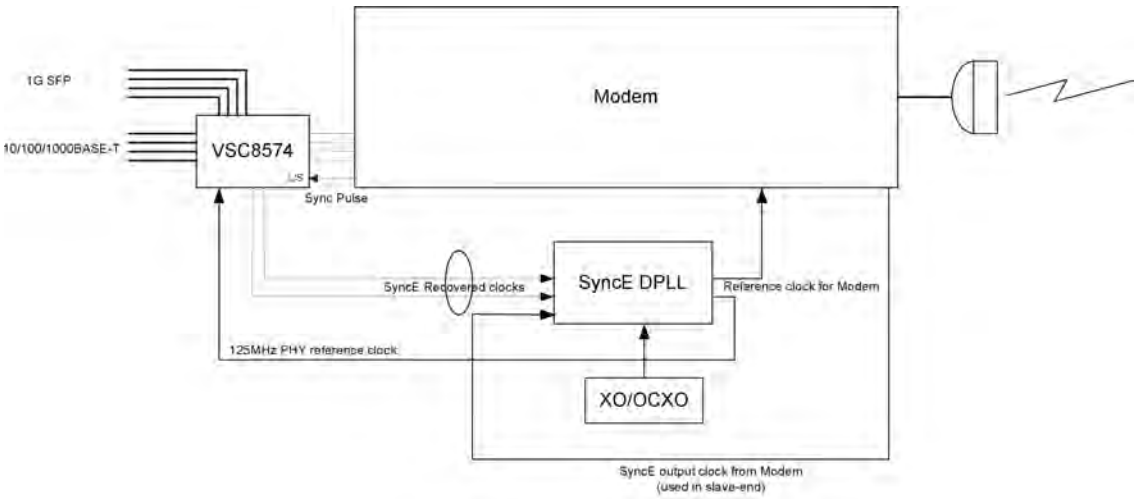


Figure 5 • SyncE and Sync Pulse Connections Using 1588 PHYs



4.2.1.1 Local Time Synchronization Protocol

Having synchronization pulses at both ends of the link is not enough. The devices also need to agree on the time. This is done by the use of a simple synchronization protocol that runs on the internal CPU of the Microsemi switches (part of the Microsemi software). Also, if the PHYs are used, the protocol runs on CPUs at each end of the microwave link that are able to communicate together. A simplified protocol is described as follows:

1. Startup–master/slave resolution: A protocol must run between the master and the slave microwave port to agree on the timing flow direction. This determines which station is the master and which station is the slave. This can also be provisioned. The timing flow direction should match the SyncE and sync pulse timing flow direction. If part of a ring structure, the SyncE direction could be reversed.
2. Time and frequency sync: When the master/slave identification has been completed and the clock of the two switches/PHYs has been synchronized using SyncE, the CPU systems in the master and slave stations configure the local time counters (LTC) in the Microsemi switches/PHYs (don't enable TC operation yet). The master then configures the Microsemi switches/PHYs to save the LTC time on the next synchronization input pulse.
   When the LTC value (MASTER_VALUE) has been saved, the master sends a frame to the slave containing the saved LTC value (MASTER_VALUE) using a local communication channel of choice. The slave then programs the Microsemi switches/PHYs to load a LTC value on the next rising edge of the synchronization pulse that is the sum of the following: MASTER_VALUE, spacing between the synchronization pulses, and known latency between the sync pulses between the master and the slave (based on modem latency and latency though the air).
   The synchronization pulse of the slave is always later than the synchronization pulse of the master. When the value has been saved at the 1588 PHY of the slave, the two PHYs are in phase lock.
3. Run-time synchronization: When the Microsemi switches/PHYs at the master and slave are in sync, the Microsemi switches/PHYs can be configured to enable the TC operation on the PTP traffic flowing over the link.
   SyncE should keep the two ends in lock, but keep synchronization information flowing between the master and slave—perform "save LTC time" on every synchronization pulse. This will enable the slave to monitor if the two stations are still in sync and if not, adjust the LTC time of the 1588 PHY by issuing 1 ns up/down corrections. If the synchronization pulse accuracy is normally distributed, it can also calculate the mean error and make adjustments to the 1588 LTC time to a mean error of 0 ns.

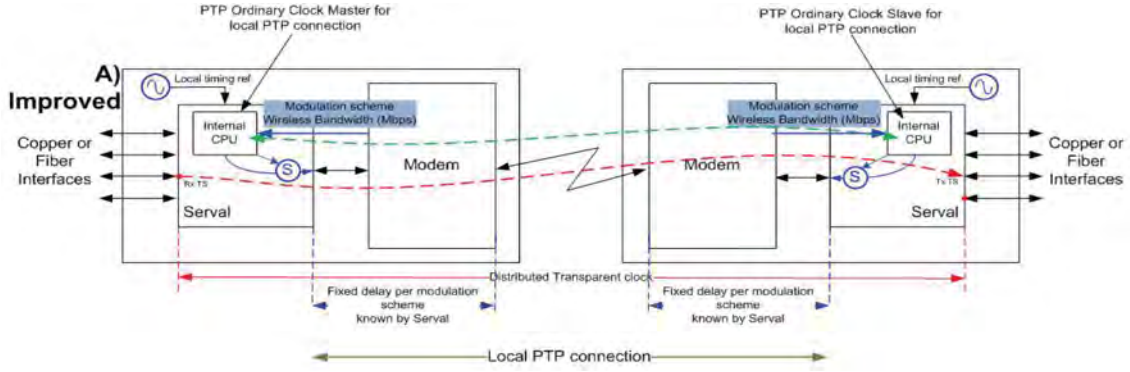
4.2.2 Fixed Modem Latency per Modulation Scheme

If the microwave modem has a fixed and known Rx/Tx latency, either on a separate low bandwidth side-channel or for the main traffic path, then Caracal or Serval-1 can use a local PTP connection to synchronize the two ends of the microwave link.

This method requires that the Rx and Tx latency is both fixed and known for each modulation scheme used by the modem—no frame buffering is being done in the modem. The internal CPU in Caracal /Serval-1 will be configured with the latency on the port towards the modem, the timestamping done on the local PTP communication compensates for the latency through the modem. The modem will inform the CPU in case of any modulation scheme changes (for instance, interrupt), so that a different latency value can be used. A traffic shaper is configured in Caracal/Serval-1. The modem only receives the amount of traffic that the current modulation scheme supports.

This method does not require any knowledge about the distance between the microwave units, it relies on a fixed latency through the modem for each modulation scheme, and can be difficult to achieve in the modem design. Any static error in one of the latency values will result in asymmetry and a static time synchronization error equal to one-half of this error.

Figure 6 • Fixed Latency Modem



If SyncE is used to lock the frequencies of the two Caracal/Serval-1 devices and the latency in the modem is static, then the amount of PTP traffic needed to keep the two ends of the microwave in sync is low (16 frames per second or less). If the modem latency is not 100% fixed for each modulation scheme, then increased PTP traffic may be required in order to support advanced PDV filtering of the local PTP frames.

In case SyncE is not supported over the microwave link, the reference clock to Caracal/Serval-1 must be very stable. This means that an OCXO/TCXO designed for 1588 applications is needed as the reference clock source.

4.2.3 Variable Latency in the Modem

If the latency through the modem is variable and no means of getting a synchronization pulse between the two ends, then it is still possible to implement a Distributed Transparent Clock using Caracal or Serval-1, but the accuracy will be lower than the other methods.

The method used is the same as in Fixed Modem Latency per Modulation Scheme, but the local PTP protocol needs to use an advanced PDV filtering algorithm that is targeted at the PDV that was introduced by the microwave modems. This algorithm uses only the PTP frames that experience the lowest latency through the modem, and must detect the jumps in latency caused by modulation shifts. It will try to keep the two ends in sync using this information, without any information from the modem it can be very difficult. The asymmetry in latency in the two directions can cause the distributed TC to add an offset to the time.

If the Caracal/Serval-1 switch modem has access to information from the modem, such as current modulation scheme and the minimum latency for this scheme, then it can compensate for asymmetry. When using a higher packet rate, to allow use of only the “fastest” packets, it can achieve a solid phase lock between the two devices.

This solution is still better than having no PTP support in the modems, as it would be the PTP slaves that need to filter PDV noise on the received frames. Without PTP in the modem, the PDV at the slaves will contain all errors introduced by the microwave link(s), as well as any PDV noise from other equipment in the path between the PTP master and the PTP slave.

If SyncE is implemented in the modems, it would also be possible to “lock” the two Caracal/Serval-1 switches in time/phase before traffic was enabled on the modems. This will allow the latency through the modems to be “fixed and symmetric” during the local PTP time sync and SyncE will ensure that they stay in phase lock when traffic is later enabled. This does require that the SyncE phase lock between the two microwave modems to be stable, any phase drift between the SyncE clocks in the two units will result in a time error introduced in the equipment.

5 Selecting the Right Microsemi Solution

The optimal solution for a given microwave design must take the following into consideration:

- Does the modem need to support Carrier Ethernet switching?
- What bandwidth and how many Ethernet ports are required?
- What types of Ethernet ports are required?
- Does the system need to support some of the advanced Carrier Ethernet switch features provided by Caracal or Serval-1?
- Does the modem technology support SyncE?
- Does/can the modem technology support some kind of synchronization pulse generation?
- Does the modem technology support a fixed latency for each modulation scheme?
- Is it required to support Distributed TC with integrated Ordinary Clock slave or Boundary Clock functionality as well?

This list does not cover all the things to consider, but will give an indication of the optimal solution.

Table 1 • Solution Table

	1588 PHY VSC8574	Caracal VSC7428	Serval-1 VSC7418
Modem supports Sync pulse generation	X	X	X
Modem only supports fixed latency per modulation scheme		X	X
Modem does not support fixed latency or sync pulse		X[1]	X[1]
Carrier Ethernet switching is required		X	X
10/100/1000BASE-T ports	X	X	X[2]
SFP ports	X	X	X
Microsemi distributed TC software		X	X
Microsemi API	X	X	X
Microsemi PTP software (Distr. TC, BC, Slave)		X	X
PTP using Ethernet or Ethernet IP/UDP	X	X	X
PTP encapsulation in MPLS	X		X

1. Requires the use of an advanced filtering algorithm.
2. Requires the use of an external VSC8574 PHY.

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