VSC8582

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8582 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8582 in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Twisted Pair Media Interface"
- Section 5.0, "SerDes Media Interface"
- Section 6.0, "QSGMII/SGMII/SerDes MAC Interface"
- Section 7.0, "Device Clocks"
- Section 8.0, "1588 Support"
- Section 9.0, "Digital Interface and I/O"
- Section 10.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8582 implementor should have the following documents on hand:

- *VSC8582-11 Data Sheet*
- VSC8582 Evaluation Design Files

These documents can be found at www.microchip.com/VSC8582.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

3.0 POWER

Table 3-1 shows the power supply pins for VSC8582.

TABLE 3-1: POWER SUPPLY PINS

Name	Pin	Description	Comments
VDD_MDIO	P3	1.2 V or 2.5 V power for SMI pins	Digital, no ferrite bead
VDD1_[1:18]	E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12,M5, M12, N5, N12	1.0V digital core power supply	Digital, no ferrite bead
VDD1A_[1:10]	C7, C8, C9, C13, P6, P7, P8, P9, P10, P11	1.0V analog core power supply. Associated with the QSGMII/SGMII MAC receiver output pins.	Analog, use ferrite bead
VDD25_[1:4]	H13, M4, M13	2.5V general digital power supply. Associated with the LED, GPIO, JTAG, and recovered clock pins.	Digital, no ferrite bead
VDD25A_[1:10]	C2, C4, C6, C11, C14, E4, E13, P5, P12, P13	2.5V general analog power supply	Analog, use ferrite bead
VSS_[1:4]	B1, B16, C5, C12	Ground	—
VSS_[6:68]	D5, D6, D7, D8, D9, D10, D11, D12, E6, E7, E8, E9, E10, E11, F4, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, M6, M7, M8, M9, M10, M11, N6, N7, N8, N9, N10, N11	Ground	—
VSS_70	R16	Ground	—

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. (See Table 3-2 for different system configuration.) Note that the current values in the table need an additional margin of 25-30%.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Maximum Current Consumption		1V Digital			1V	2.5V	2.5V	Unit
Mode	**Interface**	**Base**	**w/ 1588**	**w/ MACsec**				
Reset	N/A	885	N/A	N/A	190	11	4	mA
Power down	N/A	975	N/A	N/A	255	11	23	
1000BASE-T	2-port SGMII	1130	+80	+160	275	11	240	
100BASE-TX	2-port SGMII	—	—	—	—	—	—	
10BASE-T	2-port SGMII	—	—	—	—	—	—	
10BASE-Te	2-port SGMII	—	—	—	—	—	—	
1000BASE-X	2-port SGMII	1010	+80	+160	325	12	23	
100BASE-FX	2-port SGMII	995	+35	+120	320	12	23	
1000BASE-T	2-port QSGMII	1095	+80	+160	230	12	240	
100BASE-TX	2-port QSGMII	—	—	—	—	—	—	
10BASE-T	2-port QSGMII	—	—	—	—	—	—	
10BASE-Te	2-port QSGMII	—	—	—	—	—	—	
1000BASE-X	2-port QSGMII	1040	+80	+160	285	12	23	
100BASE-FX	2-port QSGMII	1000	+35	+120	280	11	23	

3.2 Power Supply Planes

- The VSC8582 requires two power rails: 2.5V and 1.0V. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Bulk Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

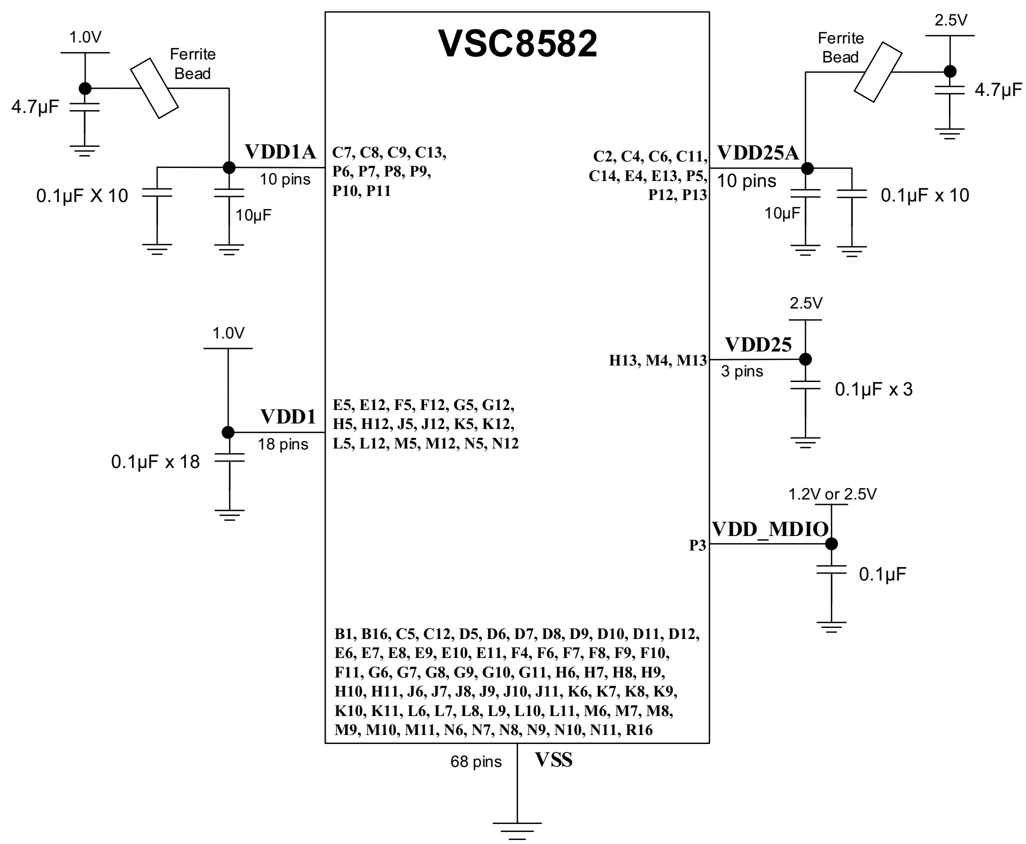
- The analog power supplies are: VDD25A and VDD1A.
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite

beads with 0Ω resistors once a thorough evaluation of system performance is completed.

- Ferrite beads are not recommended on digital supplies **VDD1**,**VDD25**, and **VDDMDIO**.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8582's power pins for every pin.
- Make sure that bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail of power supply.
- If the VSC8582 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 TWISTED PAIR MEDIA INTERFACE

4.1 10/100/1000 Mbps Interface Connection

The VSC8582 has two GPHY ports, PHY 0 and PHY 1 for port 1 and port 2. Detailed pin numbers from PHY 0 to PHY 1 sequence and descriptions are as follows:

- **TXVNA [0:1]** (pins B14 and B10): These pins are the transmit/receive negative (–) connection from pair A of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPA [0:1]** (pins A14 and A10): These pins are the transmit/receive positive (+) connection from pair A of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNB [0:1]** (pins B15 and B11): These pins are the transmit/receive negative (–) connection from pair B of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPB [0:1]** (pins A15 and A11): These pins are the transmit/receive positive (+) connection from pair B of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNC [0:1]** (pins C15 and B12): These pins are the transmit/receive negative (–) connection from pair C of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPC [0:1]** (pins C16 and A12): These pins are the transmit/receive positive (+) connection from pair C of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVND [0:1]** (pins D15 and B13): These pins are the transmit/receive negative (–) connection from pair D of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPD [0:1]** (pins D16 and A13): These pins are the transmit/receive positive (+) connection from pair D of the internal PHY 0 to PHY 1. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

There are two 10/100/1000 Mbps channel connection solutions: (1) Solution #1 is for an external environment with no electrical noise and no ESD to be considered (see Figure 4-1), and (2) Solution #2 is for an external environment with electrical noise and with ESD to be considered (see Figure 4-2).

FIGURE 4-1: SOLUTION #1 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS

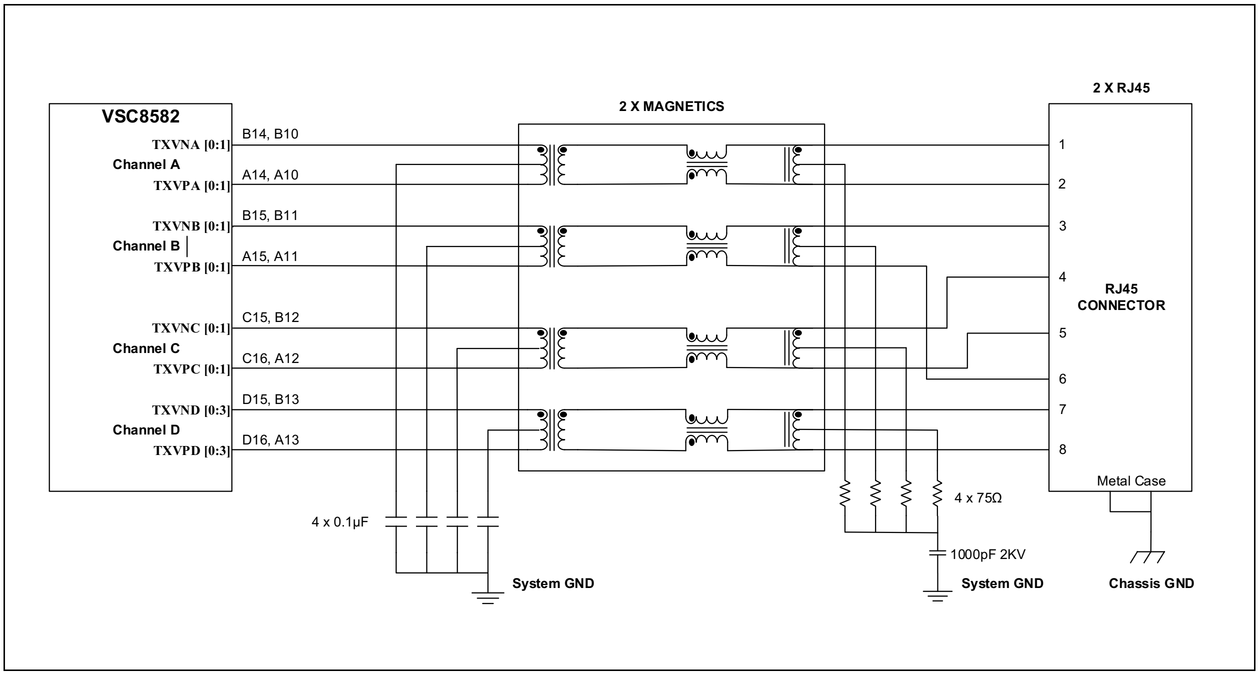
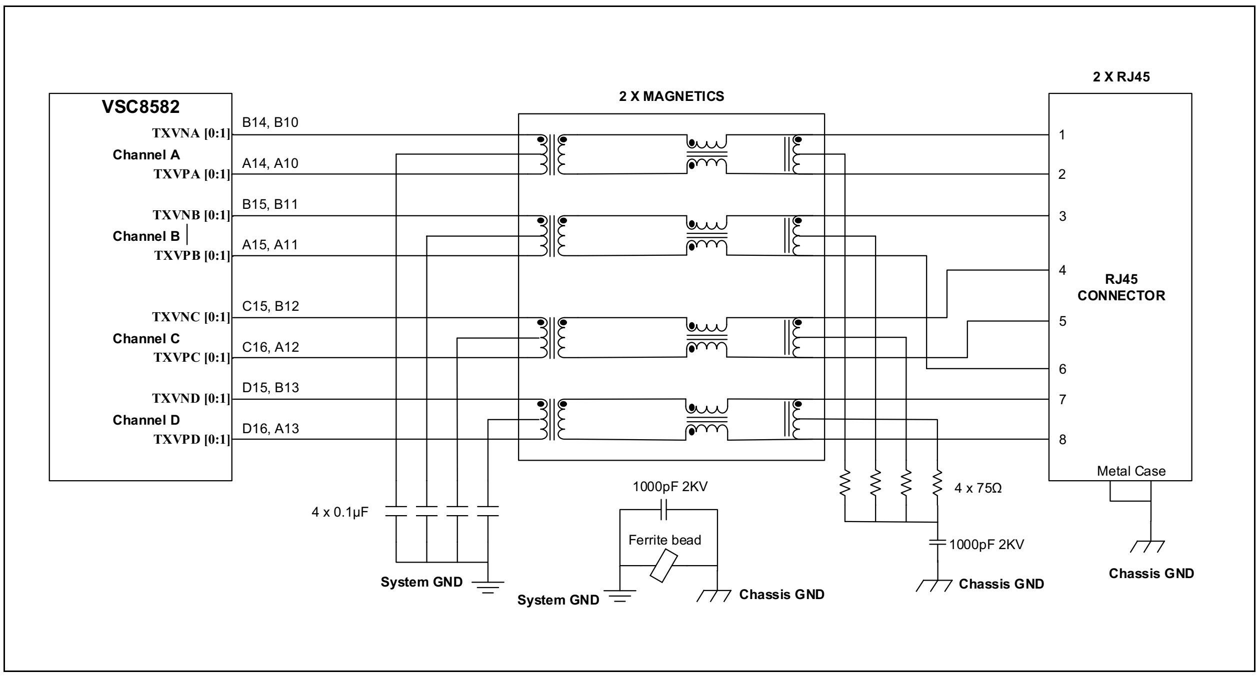


FIGURE 4-2: SOLUTION #2 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection and RJ45 Connection

- The center tap connection on the VSC8582 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8582 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8582 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8582 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps of the magnetics of all four pairs should not be connected together without the 0.1 µF capacitors to ground. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground, it is shared by PHY 0 and PHY 1 for port 1 and port 2.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, "PCB Layout Considerations" for guidance on how chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on Microchip Technology product page) for reference.

4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss requiring the PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of pairs A, B, C, and D should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8582 device or other sensitive devices in the PCB layout placement for better ESD.

5.0 SERDES MEDIA INTERFACE

5.1 Fiber and Copper SFP Interface Pins and Descriptions

- The VSC8582 device SerDes media interface supports 1000BASE-X fiber ports with 1000BASE-X family SFPs, or 100BASE-FX fiber ports with 100BASE-FX SFPs, or 10/100/1000BASE-T copper ports with 10/100/1000BASE-T copper SFPs.
- For the details of SFP-related pin numbers and descriptions of the SerDes media interface, see Table 5-1. For SerDes media SFP interface connections, see Figure 5-1 and Figure 5-2.

TABLE 5-1: SFP-RELATED PIN NUMBERS AND DESCRIPTIONS FOR SERDES MEDIA INTERFACE

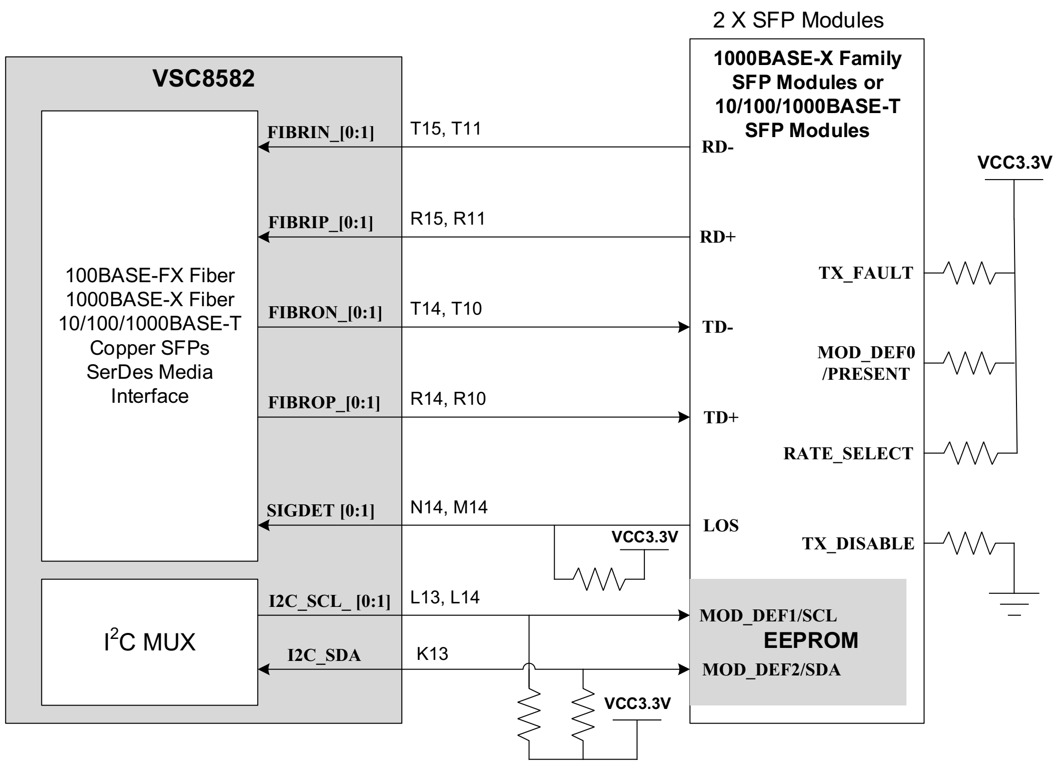
Pin Name	Pin Number	Type	Description
SerDes Media Interface Pins			
FIBRIN_[0:1]	T15, T11	Input	SerDes media interface receiver input pairs
FIBRIP_[0:1]	R15, R11	Input	
FIBRON_[0:1]	T14, T10	Output	SerDes media interface transmitter output pairs
FIBROP_[0:1]	R14, R10	Output	
SIGDET [0:1]	N14, M14	Input	If SIGDET is used as signal detect for SFP
I^2C Two-Wire Serial Controller Pins			
I2C_SCL_[0:1]	L13, L14	Output	I^2C two-wire serial controller clock pins
I2C_SDA	K13	I/O	I^2C two-wire serial controller data pin

5.2 SerDes Media Interface Connecting to 1000BASE-X Fiber or 1000BASE-T Copper SFPs

To connect the VSC8582 device to a 1000BASE-X fiber SFP or 10/100/1000BASE-T copper SFP, use the following guidelines and reference schematic:

- The RD+/– and TD+/– differential pairs must be able to perform 100Ω impedance control in the PCB layout and FAB.
- The **SIGDET** input pin of the PHY should be connected to the **LOS** output pin of the SFP connector.
- The MII register should be set to 19E.0 = 1 in order to set the **SIGDET** pin to active-low. This will set the pin to properly receive the LOS behavior without additional glue logic.
- The SFP’s Present, SCL, SDA, TX_DIS, TX_FAULT, and RX_LOS signals may be connected to the Switch/MAC/ASIC or the GPIO pins of the VSC8582. If using multiple SFPs, it may be best to implement an I^2C controller as all SFP devices have an I^2C address = 00000.
- One of the port LED pins should be used and LINK/ACTIVITY be selected and connected to the CATHODE pin of an LED. This can be used to indicate when the SFP is linked and has data activity present.
- If there is no 0.1 µF AC coupling capacitors in SFP, then four external 0.1 µF AC coupling capacitors must be added for RD+/– and TD+/– differential pairs. Usually, almost all SFPs have internal termination resistors and AC coupling capacitors.
- All pull-up resistors should have a value between 4.7 kΩ to 10 kΩ.

FIGURE 5-1: SERDES MEDIA INTERFACE TO 1000BASE-X FAMILY FIBER SFP OR 10/100/1000BASE-T COPPER SFP REFERENCE CONNECTION

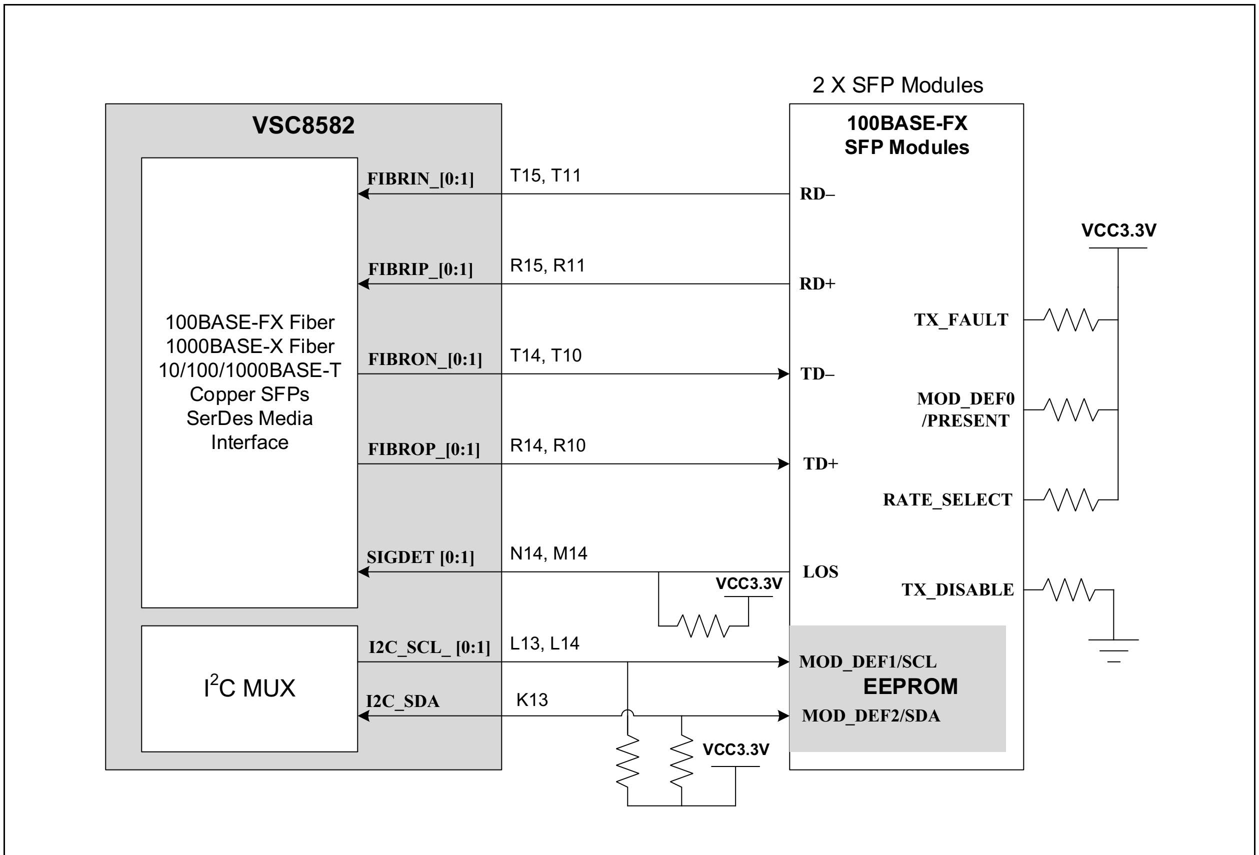


5.3 SerDes Media Interface Connecting to 100BASE-FX Fiber SFPs

To connect VSC8582 device to a 100BASE-FX fiber SFP, use the following guidelines and reference schematic:

- The RD+/– and TD+/– differential pairs must be able to perform 100Ω impedance control in the PCB layout and FAB.
- The **SIGDET** input pin of the PHY should be connected to the **LOS** output pin of the SFP connector.
- The MII register should be set to 19E.0 = 1 in order to set the **SIGDET** pin to active-low. This will set the pin to properly receive the LOS behavior without additional glue logic.
- The SFP's Present, SCL, SDA, TX_DIS, TX_FAULT, and RX_LOS signals may be connected to the Switch/MAC/ASIC or the GPIO pins of the VSC8582. If using multiple SFPs, it may be best to implement an I^{2}C controller as all SFP devices have an I^{2}C address = 00000.
- If there are no **TX_FAULT** and **RATE_SELECT** pins on some of 100BASE-FX SFPs or they are invalid pins, they should be left not connected.
- One of the port LED pins should be used and LINK/ACTIVITY be selected and connected to the CATHODE pin of an LED. This can be used to indicate when the SFP is linked and has data activity present.
- If there is no 0.1 µF AC coupling capacitors in SFP, four external 0.1 µF AC coupling capacitors must be added for RD+/– and TD+/– differential pairs. Usually, almost all SFPs have internal termination resistors and AC coupling capacitors.
- All pull-up resistors should have a value between 4.7K kΩ to 10 kΩ.

FIGURE 5-2: SERDES MEDIA INTERFACE WITH TWO 100BASE-FX FIBER SFP MODULES



6.0 QSGMII/SGMII/SERDES MAC INTERFACE

6.1 QSGMII/SGMII/SerDes MAC Pins and Connection

- The VSC8582 device supports one QSGMII MAC, two SGMII MACs, or two SerDes MACs.
- For detailed pin numbers and description and connection of QSGMII/SGMII/SerDes MAC interface, see Table 6-1 and Figure 6-1 to Figure 6-3.

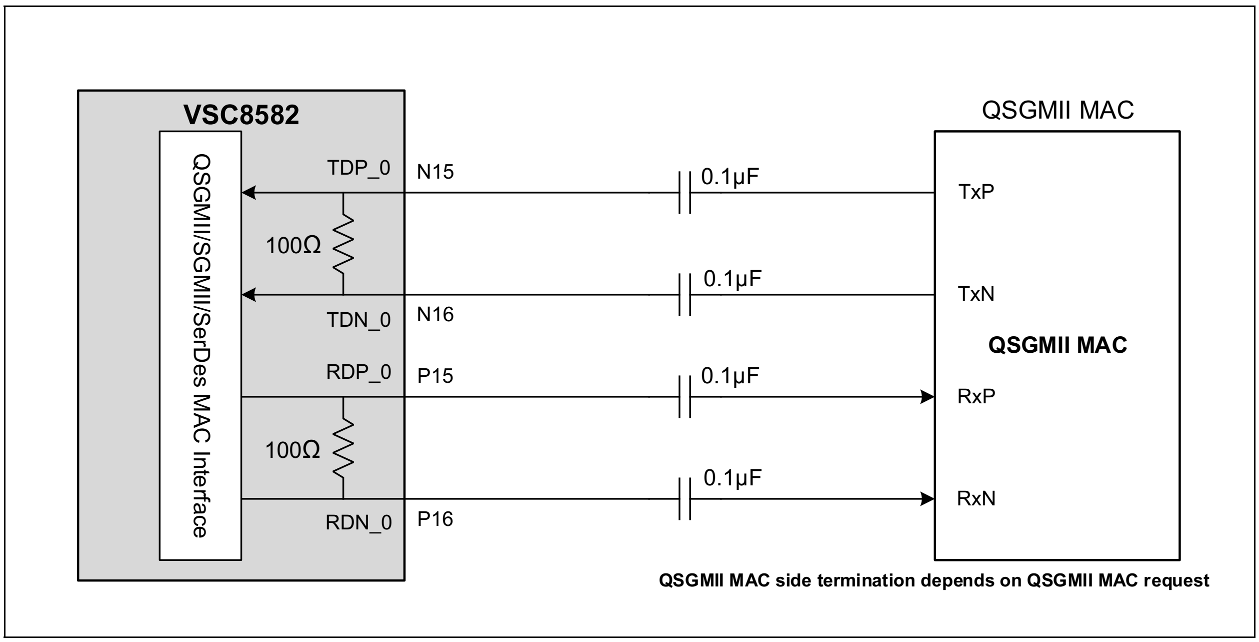
TABLE 6-1: QSGMII/SGMII/SERDES INTERFACE PINS

Pin Name	Pin Number	Type	Description
RDN_[0:1]	P16, T12	Output	QSGMII/SGMII/SerDes MAC receiver output pairs
RDP_[0:1]	P15, R12	Output	
TDN_[0:1]	N16, T13	Input	QSGMII/SGMII/SerDes MAC transmitter input pairs
TDP_[0:1]	N15, R13	Input	

6.2 QSGMII MAC

- The VSC8582 device supports a QSGMII MAC to convey two ports of network data and port speed from 10/100/1000 Mbps.

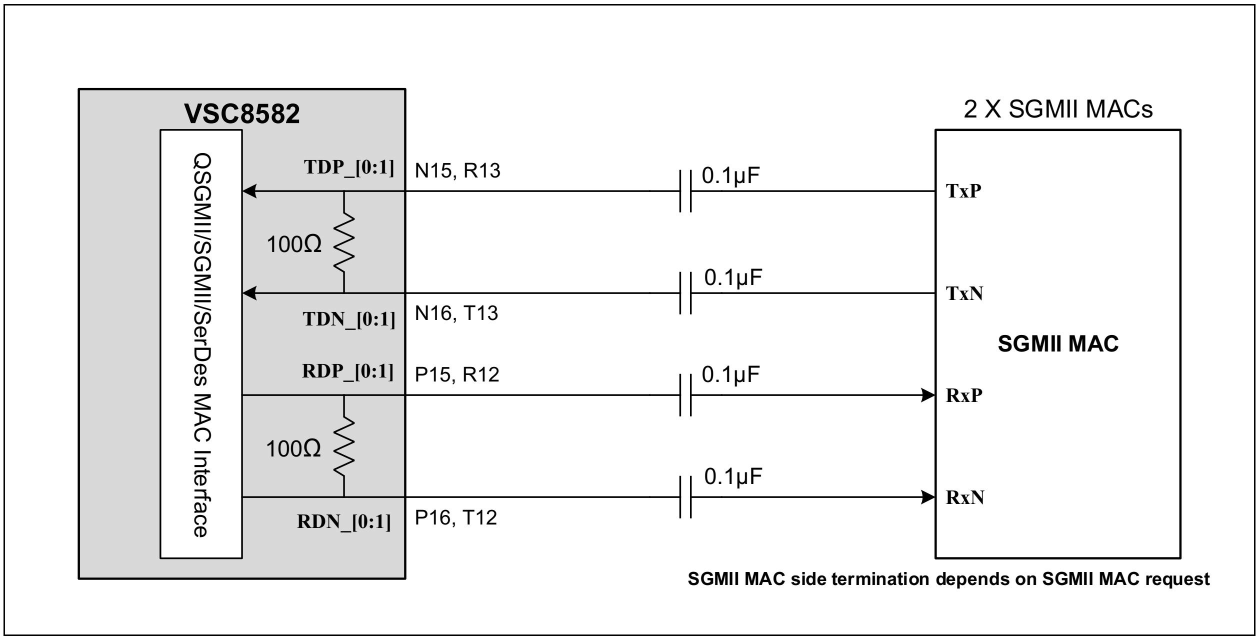
FIGURE 6-1: QSGMII MAC INTERFACE CONNECTIONS



6.3 SGMII MAC

- When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8582 device can be connected to an SGMII-compatible MAC.

FIGURE 6-2: SGMII MAC INTERFACE CONNECTIONS



6.4 SerDes MAC

- When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8582 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported.
- Figure 6-3 shows the SerDes MAC interface connection. Figure 6-4 shows the SerDes MAC interface connection to 1000BASE-X SFP or 1000BASE-T SFP.

FIGURE 6-3: SERDES MAC INTERFACE CONNECTIONS

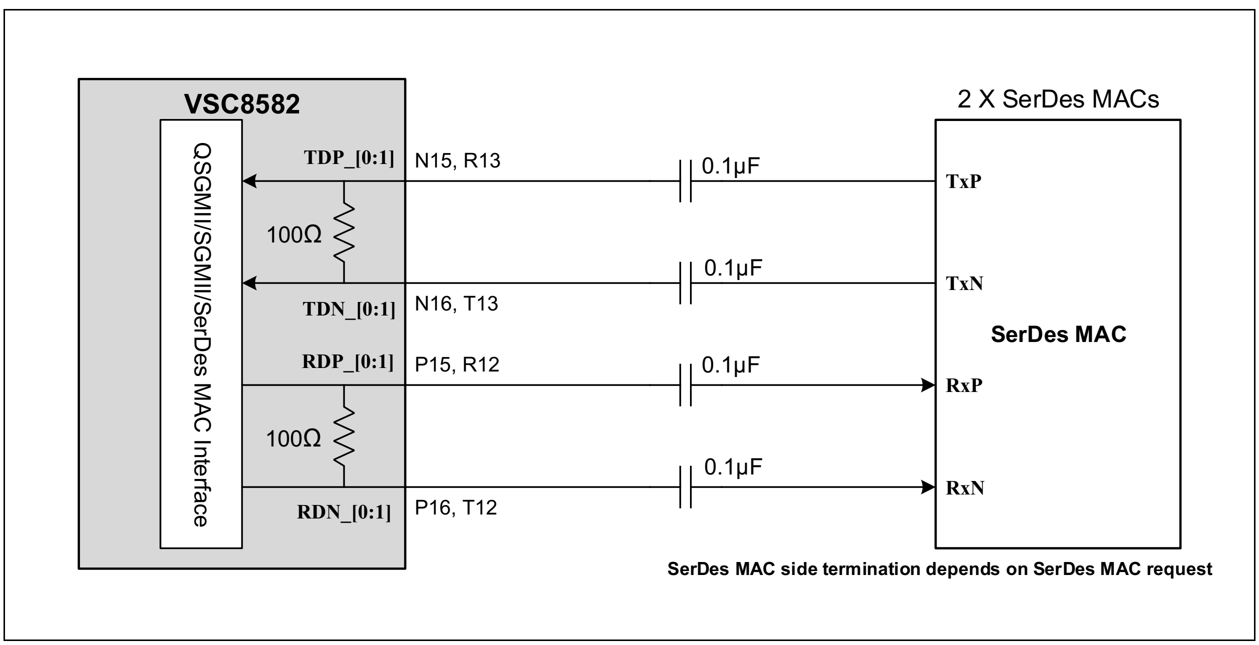
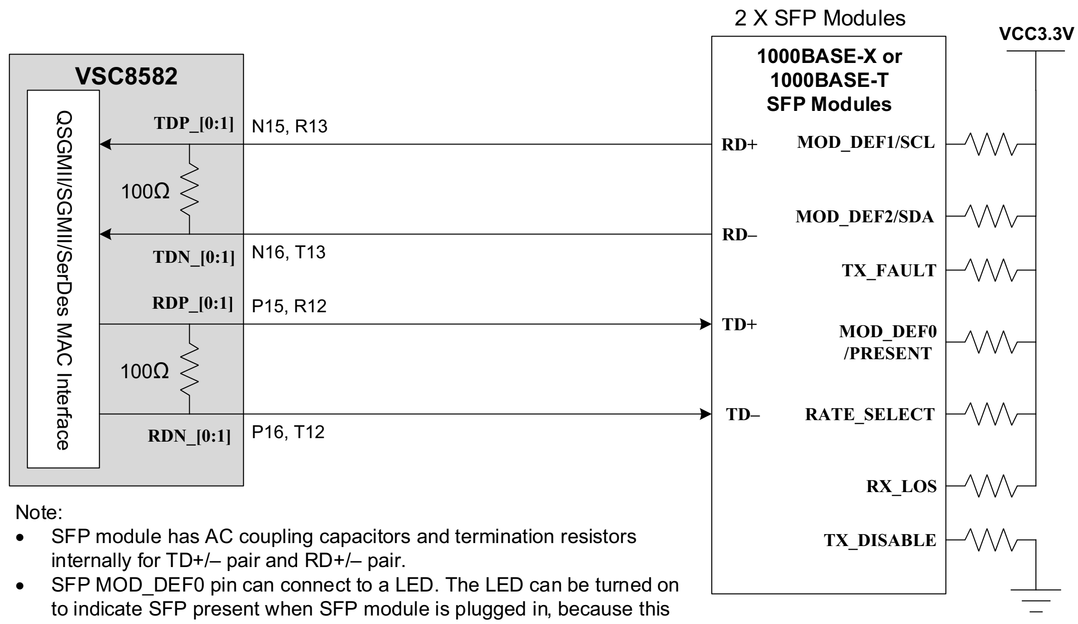


FIGURE 6-4: SERDES MAC INTERFACE TO 1000BASE-X SFP OR 1000BASE-T SFP CONNECTION



Note:
- SFP module has AC coupling capacitors and termination resistors internally for TD+/– pair and RD+/– pair.
- SFP MOD_DEF0 pin can connect to a LED. The LED can be turned on to indicate SFP present when SFP module is plugged in, because this MOD_DEF0 pin has an internal about 100Ω pull-down resistor.

6.5 QSGMII/SGMII/SerDes MAC Design Rules

- Use AC coupling with 0.1 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If the SGMII/SerDes port is unused, both the **RDx** pair and **TDx** pair pins can be left floating (No Connect).

7.0 DEVICE CLOCKS

7.1 Reference Clock

- The device reference clock supports both 25 MHz and 125 MHz clock signals. The reference clocks can be either differential or single-ended. If differential, they must be capacitively coupled and LVDS-compatible.
- Refer to Table 7-1 for the reference clock pins and system clock frequency selection.

TABLE 7-1: REFERENCE CLOCK PINS

Pin Name	Pin Number	Type	Description
REFCLK_P	D1	ADIFF	Differential reference clock input pair
REFCLK_N	C1	ADIFF	
REFCLK_SEL2	E1	I, PU	Selects the reference clock speed: 0: 25 MHz (Pull down to VSS) 1: 125 MHz (Default or pull up to 2.5V) Use 125 MHz for typical applications.

When reference clocks are used, ensure that:

- The jitter requirements in the data sheet are met.
- The amplitude specifications in the data sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 µF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC8582 side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- For QSGMII operation of the PHY, 25 MHz reference clock is not recommended.

7.2 Single-Ended REFCLK Input

To use a single-ended reference clock, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK, with the clock centered at 1V and a 500 mV peak-to-peak swing, are shown in Figure 7-1.

FIGURE 7-1: SINGLE-ENDED REFCLK INPUT RESISTOR DIVIDER

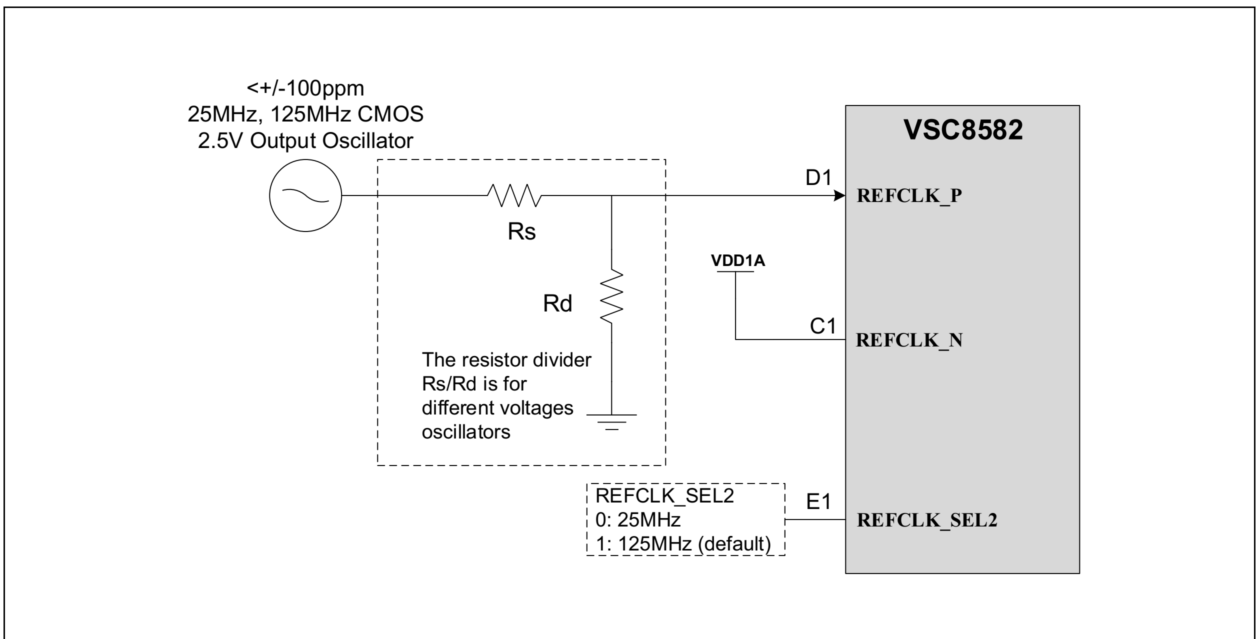


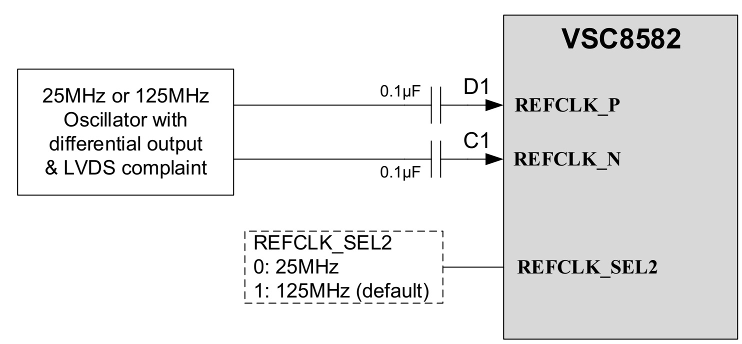
TABLE 7-2: SINGLE-ENDED REFCLK INPUT RESISTOR DIVIDER

Oscillator CMOS Output Voltage	Resistor Divider Rs Value (Ω)	Resistor Divider Rd Value (Ω)
2.5V	220	910
3.3V	270	430
5V	430	300

7.3 Differential REFCLK Input

AC coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS compatible. Figure 7-2 shows the configuration.

FIGURE 7-2: AC COUPLING FOR REFCLK DIFFERENTIAL INPUT

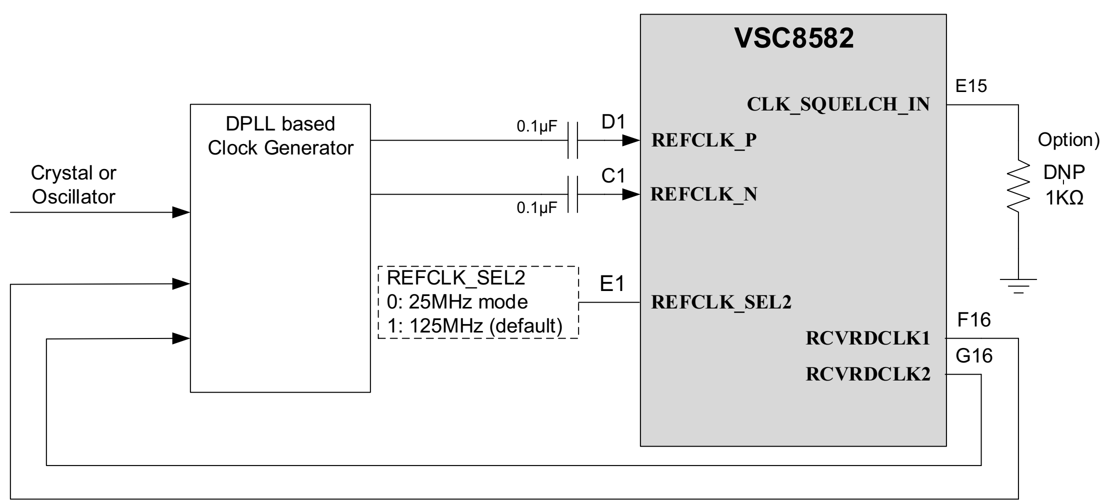


7.4 Media Recovered Clock Output

For Synchronous Ethernet applications, the VSC8582 includes two recovered clock output pins.

- **RCVRDCLK1** (pin F16) is controlled by register 23G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
- **RCVRDCLK2** (pin G16) is controlled by register 24G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
  - To enable recovered clock output, set register 23G or 24G, bit 15 to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 125 MHz), and squelch conditions.
- **CLK_SQUELCH_IN** (pin E15) is the input control to squelch the recovered clock. Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The **CLK_SQUELCH_IN** pin controls the squelching of the clock. Both **RCVRDCLK1** and **RCVRDCLK2** are squelched when the **CLK_SQUELCH_IN** pin is high. This pin should not be left floating when using Synchronous Ethernet applications.
- For using Synchronous Ethernet applications, see Figure 7-3 for reference.

FIGURE 7-3: TYPICAL SYNCHRONOUS ETHERNET CLOCK CONFIGURATION



Note:

- **One or both RCVRDCLK recovered clocks**
- **CLK_SQUELCH_IN pin has internal pull-up (PU) to squelch the RCVRDCLK1/2 outputs always, add a pull-down (PD) DNP resistor in design to disable squelch as an option if not using this feature to squelch always.**

8.0 1588 SUPPORT

8.1 1588_DIFF_INPUT_CLK Configuration

- The default configuration of the **1588_DIFF_INPUT_CLK_P/N** pins sets the device to use an internal clock for the LTC. To configure these pins correctly in order to use an external clock for LTC, write 0xb71c to register 30E1588 and 0x7ae0 to register 29E1588. Set these two registers to 0x0 when an internal clock is used for LTC.
- The local time counter keeps the local time for the device and the time is monitored and synchronized to an external reference by the CPU. The source clock for the counter can be selected as internal or external. When internal is selected, the clock freq is 250 MHz. When external is selected, the clock freq can be 250 MHz, 200 MHz, 125 MHz, or some other supported frequency. The clock may be a line clock or the dedicated **1588_DIFF_INPUT_CLK_P/N** pins. The clock source is selected in register LTC_CTRL.LTC_CLK_SEL. See Table 8-1 for pins detail.

TABLE 8-1: 1588 DIFFERENTIAL CLOCK PIN PAIR

Pin Name	Pin Number	Type	Description
1588_DIFF_INPUT_CLK_N	J16	ADIFF	Differential reference clock input pair For IEEE-1588 applications, a quality oscillator is recommended. Use A/C coupling because the differential clock pair is self-biased to VDD1A. No external termination is required, as there is an internal termination.
1588_DIFF_INPUT_CLK_P	J15	ADIFF	

8.2 1588 Serial Timestamp Interface

- For each 1588 Processor 0 and 1, timestamp information stored in the Egress direction can be read through either the register interface SMI or through the Serial Timestamp interface 1588 SPI. These two ways to read registers are mutually exclusive. While enabling/disabling the serial interface is done on a Processor level, only one serial interface exists. This means that the serial interface can be enabled for Processor 0, while the timestamp FIFO can be read through registers for Processor 1. If the serial interface is enabled for both Processors 0 and 1, then the serial interface will arbitrate between two Egress Timestamp FIFOs in Processors 0 and 1 and push the data out. The timestamp FIFO serial interface block writes, or pushes, timestamp/frame signature pairs that have been enqueued and packed into timestamp FIFOs to the external chip interface consisting of three output pins: **1588_SPI_DO**, **1588_SPI_CLK**, and **1588_SPI_CS**. There is one interface for all channels.
- The serial timestamp interface can be enabled in register TS_FIFO_SI_CFG. Bit [0] TS_FIFO_SI_ENA.
- Refer to Table 8-2 and Figure 8-1 for additional pins and using 1588 serial timestamp interface.

TABLE 8-2: 1588 SUPPORT PINS

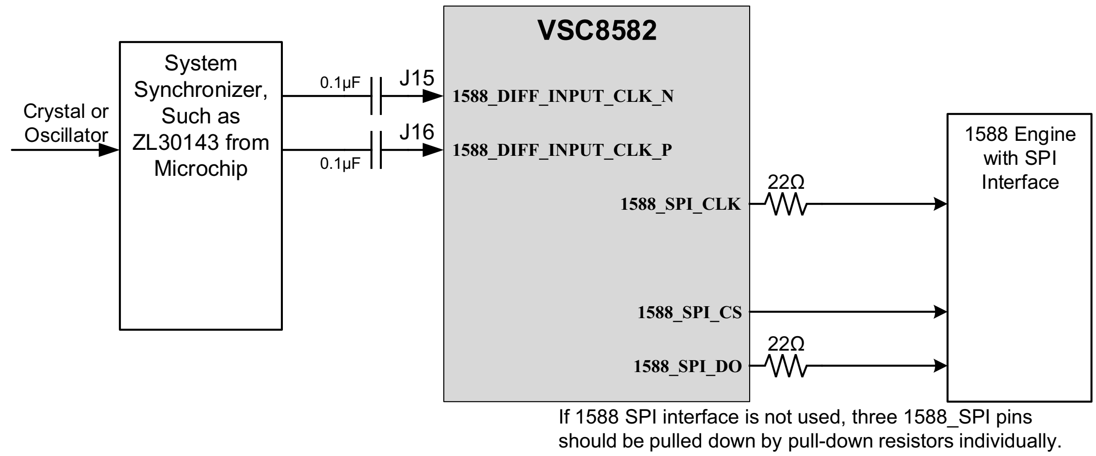
Pin Name	Pin	Type	Description
1588_SPI_DO/GPIO13	H14	I/O, PU, 3V	Optional use. May be left floating if unused. A 3-pin TS pushout SPI data out and typically used in 2-step mode. Can be configured to serve as General Purpose Input/Output (GPIO).
1588_SPI_CS/GPIO12	J14	I/O, PU, 3V	Optional use. May be left floating if unused. A 3-pin TS pushout SPI chip select and typically used in 2-step mode. If used as a GPIO, verify that the drive strength meets the application.
1588_SPI_CLK	E16	O	1588 SPI clock

TABLE 8-2: 1588 SUPPORT PINS (CONTINUED)

Pin Name	Pin	Type	Description
1588_PPS_RI	E14	I/O, PU, 3V	Optional use (for calibration only). Tie to GND if not used. PPS return input signal
1588_PPS_3/1588_SPI_IN_DI	L2	I/O, PU, 3V	Optional use. May be left floating if unused. 1588 local timer 3 PPS fixed to local timestamp counter PHY3. (If used as a PPS signal, take note of the trace length and skew to other PPS signals.) If used as a 1588 SPI input data for daisy-chained time-stamping content, ensure length matching to achieve setup/hold.
1588_PPS_2/1588_SPI_IN_CS	N4	I/O, PU, 3V	Optional use. May be left floating if unused. 1588 local timer 2 PPS fixed to local timestamp counter PHY2. (If used as a PPS signal, take note of the trace length and skew to other PPS signals.) If used as a 1588 SPI input chip select for daisy-chained timestamping content, ensure length matching to achieve setup/hold.
1588_PPS_1/1588_SPI_IN_CLK	N3	I/O, PU, 3V	Optional use. May be left floating if unused. If used as a PPS signal, take note of the trace length and skew to other PPS signals. If used as a 1588 SPI input clock for daisy-chained time-stamping content, ensure length matching to achieve setup/hold.
1588_PPS_0/GPIO11	K16	I/O, PU, 3V	Optional use. May be left floating if unused. 1588 local timer 0 PPS configurable to local timestamp counter PHY0 through PHY3. (If used as a PPS signal, take note of the trace length and skew to other PPS signals.) If used as a GPIO, verify that the drive strength meets the application.
1588_LOAD_SAVE/GPIO10	K15	I/O, PU, 3V	Sync signal to load the time to the 1588 engine. Rising edge triggered. Can be configured to serve as GPIO.

Note: The SPI 1588 Timestamping hardware interface requires three connections to the external (slave) receiver: 1588_SPI_DO, 1588_SPI_CS and 1588_SPI_CLK. Connections to 1588_SPI_IN_DI, 1588_SPI_IN_CS and 1588_SPI_IN_CLK are not required. These optional signals exist for convenience, to daisy-chain multiple SPI Timestamping interfaces on VSC8582/VSC8584/VSC8575 (1588-enabled PHYs) together in order to relieve routing congestion for multi-PHY PCBs.

FIGURE 8-1: 1588 DIFFERENTIAL CLOCK AND 1588 SPI CONFIGURATION



9.0 DIGITAL INTERFACE AND I/O

9.1 Serial Management Interface (SMI) Pins

- The VSC8582 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its **MDC** and **MDIO** pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.
- Energy Efficient Ethernet (EEE) control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For information, see the *VSC8582 Data Sheet*.
- The SMI is a synchronous serial interface with input data to the VSC8582 on the MDIO pin that is clocked on the rising edge of the **MDC** pin. The output data is sent on the **MDIO** pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2 kΩ pull-up resistor is required on the **MDIO** pin. See Table 9-1 for SMI interface pin numbers and more information.

TABLE 9-1: SMI INTERFACE PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
MDC	P2	I, PD	A maximum of 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	N2	I/O, TS	Management data input/output pin (TS, Tri-State). Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.
MDINT	M2	I/O, OD, OS	Management interrupt signal. Upon reset the device will configure these pins as active-low (OD, open drain) or active-high (OS, open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.

9.2 GPIO Pins

- VSC8582 provides 15 multiplexed general-purpose input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers. Table 9-2 shows an overview of the register controls for GPIO pins.
- These GPIO pins have internal pull-up (PU). Any unused GPIO pins can be left floating (No Connect).

TABLE 9-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Alternative Use
GPIO0	N14	13G [1:0]	15G.0	16G.0	17G.0	SIGDET0
GPIO1	M14	13G [3:2]	15G.1	16G.1	17G.1	SIGDET1
GPIO2	M15	13G [5:4]	15G.2	16G.2	17G.2	SIGDET2
GPIO3	M16	13G [7:6]	15G.3	16G.3	17G.3	SIGDET3
GPIO4	L13	13G [9:8]	15G.4	16G.4	17G.4	I2C_SCL_0
GPIO5	L14	13G [11:10]	15G.5	16G.5	17G.5	I2C_SCL_1
GPIO6	L15	13G [13:12]	15G.6	16G.6	17G.6	I2C_SCL_2
GPIO7	L16	13G [15:14]	15G.7	16G.7	17G.7	I2C_SCL_3
GPIO8	K13	14G [1:0]	15G.8	16G.8	17G.8	I2C_SDA

Note 1: For all GPIO-related register bits in the table, defaults are ‘0’ or ‘00’, and write ‘1’ or ‘11’ is valid.

TABLE 9-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL (CONTINUED)

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Alternative Use
GPIO9	K14	14G [3:2]	15G.9	16G.9	17G.9	FASTLINK_FAIL
GPIO10	K15	14G [5:4]	15G.10	16G.10	17G.10	1588_LOAD_SAVE
GPIO11	K16	14G [7:6]	15G.11	16G.11	17G.11	1588_PPS_0
GPIO12	J14	14G [15:14]	15G.12	16G.12	17G.12	1588_SPI_CS
GPIO13	H14	14G [15:14]	15G.13	16G.13	17G.13	1588_SPI_DO

Note 1: For all GPIO-related register bits in the table, defaults are ‘0’ or ‘00’, and write ‘1’ or ‘11’ is valid.

9.3 JTAG Pins

- If JTAG is not used, **TRST** should be pulled low. The other pins may be left floating (No Connect). See Table 9-3 for JTAG pin information.

TABLE 9-3: JTAG PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
TCK	F3	I, PU	Boundary scan, test clock input. Internally pulled high.
TDI	F2	I, PU	Boundary scan, test data input. Internally pulled high.
TDO	F1	O	Boundary scan, test data output
TMS	E2	I, PU	Boundary scan, test mode selection. Internally pulled high.
TRST	E3	I, PU	Boundary scan, test Reset input. Internally pulled high. **Note:** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation.

10.0 MISCELLANEOUS

10.1 Reset

- The VSC8582 must be reset at power-up. One option is to hold **NRESET** low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **NRESET** low for a minimum 100 ns after power-up. **NRESET** is typically driven by a voltage monitor device or by the management processor or FPGA. See Table 10-1 for more information on this pin.

TABLE 10-1: RESET PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
NRESET	M3	I, PD	Device reset. Active low input that powers down the device and sets all register bits to their default state.

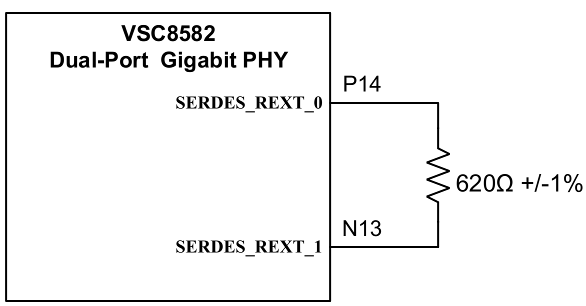
10.2 Reference Resistor

- Connect a 620Ω ±1% resistor between **SERDES_REXT_0** and **SERDES_REXT_1** as shown in Figure 10-1. See Table 10-2 for additional details on the pins.

TABLE 10-2: REFERENCE RESISTORS DESCRIPTIONS

Pin Name	Pin Number	Type	Description
SERDES_REXT_0	P14	ABIAS	SerDes bias pins. Connect to a 620Ω 1% resistor.
SERDES_REXT_1	N13	ABIAS	

FIGURE 10-1: SERDES BIAS RESISTOR



10.3 LED Pins

- The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits [13:10]. The default polarity is active low. The register 25G, register 29 and 30 can be configured for different LED modes.
- The VSC8582 LED pins are for dual-port status; refer to Table 10-3 for all indicator LED pins.
- Using 330Ω to 510Ω current limit resistor is recommended and VDD25 for LED power.

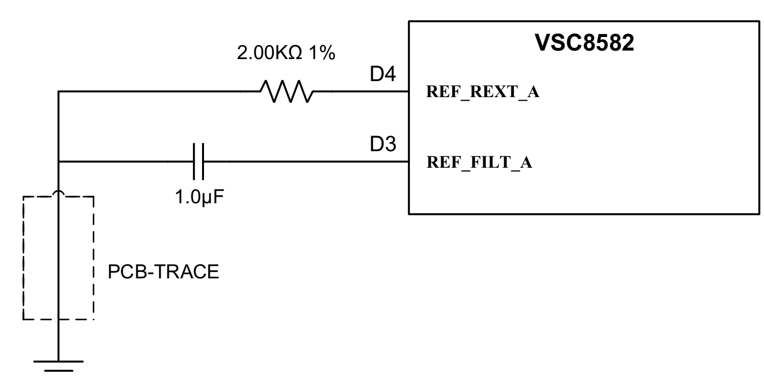
TABLE 10-3: LED PINS AND BASIC DEFAULT FUNCTION

Pin Name	Pin Number	Type	Description
LED0_[0:1]	G1, H1	O	LED0 is for PHY [0:1]. LED0 default is LED mode 1 for link 1000/Activity and can be changed by register 29 bits [3:0].
LED1_[0:1]	G2, H2	O	LED1 is for PHY [0:1]. LED1 default is LED mode 2 for link 100/Activity and can be changed by register 29 bits [7:4].
LED2_[0:1]	G3, H3	O	LED2 is for PHY [0:1]. LED2 default is LED mode 0 for link/Activity and can be changed by register 29 bits [11:8].
LED3_[0:1]	G4, H4	O	LED3 is for PHY [0:1]. LED3 default is LED mode 8 for Duplex/Collision and can be changed by register 29 bits [15:12].

10.4 Analog Bias Pins for Voltage Reference

- The **REF_REXT_A** pin (pin D4) on the VSC8582 device should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0% and minimum 1/16W. This pin is used to set up critical bias currents for the Ethernet physical device.
- The **REF_FILT_A** pin (pin D3) on the VSC8582 device should connect to the system ground through a 1 µF capacitor with 10% tolerance; NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in Figure 10-2. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8582.
- Refer to Figure 10-2 for the analog bias pins connection.

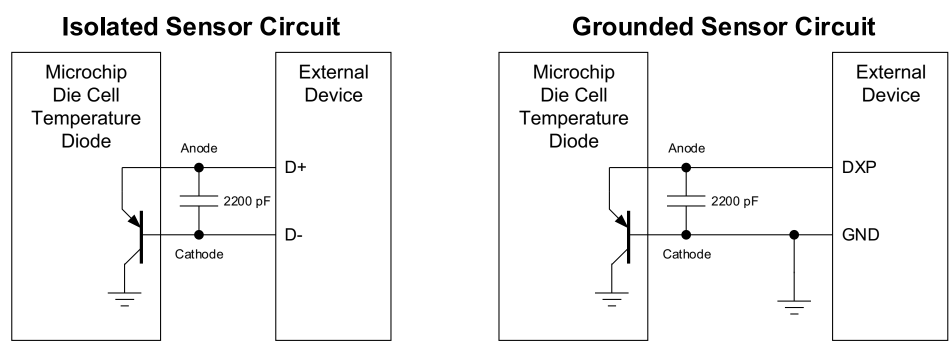
FIGURE 10-2: VOLTAGE REFERENCE SCHEMATIC



10.5 Temperature Sensor Diode

- The temperature sensor diode pins provide access to an on-die diode and internal circuitry for monitoring die temperature. To use it, connect an external thermal sensor located on the board or in a stand-alone measurement kit. The feature can be as an option in application.
- The **THERMDA** pin (pin C3) is the Thermal Diode Anode pin, which needs to be pulled down by a pull-down resistor if not used.
- The **THERMDC_VSS** pin (pin D2) is the Thermal Diode Cathode pin connected to system ground. The temperature sensor must be chosen accordingly. This pin needs to be pulled down by a pull-down resistor if not used.
- Temperature measurement using a thermal diode is very sensitive to noise. Figure 10-3 illustrates a generic application design.

FIGURE 10-3: THERMAL DIODE CONNECTIONS



Note: Microchip does not support or recommend operation of the thermal diode under reverse bias.

10.6 PHY Address Pins

- The VSC8582 device includes three external PHY address pins, **PHYADD [4:2]**, to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9. See Table 10-4 for more information on the PHY address.

TABLE 10-4: PHY ADDRESS PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
PHYADD1	F13	I, PU	Device SMI Address Bit 1. Normally tied to VSS unless an address offset of 0x2 is used by the system's station manager.
PHYADD2	G13	I, PD	PHYADD [4:2] for access each PHY's registers through SMI interface.
PHYADD3	G14	I, PD	
PHYADD4	F14	I, PD	

10.7 SPI Slave (Optional Use)

Use slave SPI I/O for 1588 and MACsec register access.

Note: Highly recommended for MACsec applications.

TABLE 10-5: SPI SLAVE INTERFACE PINS

Pin Name	Pin Number	Type	Description
SPI_IO_CLK	H15	I/O, PU, 3V	Serial peripheral interface clock input from external device
SPI_IO_CS	J13	I/O, PU, 3V	Serial peripheral interface chip select
SPI_IO_DI	G15	I/O, PU, 3V	Serial peripheral interface data input
SPI_IO_DO	F15	I/O, PU, 3V	Serial peripheral interface data output

10.8 Other Pins

- The **COMA_MODE** (pin L3) provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of reset. Hence, this pin should be pulled down by a pull-down resistor. When this pin is asserted high, all PHYs are held in a powered down state. When deasserted low, all PHYs are powered up and resume normal operation.
- The **FASTLINK_FAIL** (pin K14) provides a Fast Link Failure indication signal. The register 17G bit [9] can enable this feature, and the register 19G bits [3:0] can select the source PHY for fast link failure indication. If this feature is not used, this pin **FASTLINK_FAIL/GPIO_9** can be floating.

10.9 Unused and No Connection Pins

- The **RESERVED_[1:8]** pins (pins C10, D13, L4, P4, L1, M1, N1, and P1) are reserved signals. Leave them unconnected (floating).
- The **NC_[1:4]** pins (pins A1, A16, T1, and T16) are unconnected pins. Leave them floating.

10.10 General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 kΩ resistor is recommended to use.
- If there is no pull-down resistor value specified, a 1 kΩ or 4.7 kΩ resistor is recommended to use.

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if a single ground reference as a system ground is used for all ground pins. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Refer to Table 3-1 to ensure that the power pins are correct. Select the correct power supply components with at least about 25-30% margin based on Table 3-2 for the system power design.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection, decoupling capacitors, and filtering.		
	Section 3.4, "Bulk Decoupling Capacitors"	If doing PCB layout, see this section for the bulk decoupling capacitor required.		
Section 4.0, "Twisted Pair Media Interface"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pins connection for dual-port circuit design based on product design requirement to select the design of Figure 4-1 or Figure 4-2.		
	Section 4.2, "10/100/1000 Magnetics Connection and RJ45 Connection"	Verify the magnetics and the common-mode capacitors connection based on Figure 4-1 or Figure 4-2.		
	Section 4.3, "PCB Layout Considerations"	Refer to this section for PCB layout design reference to check if the Gigabit copper port PCB layout request is met.		
Section 5.0, "SerDes Media Interface"	Section 5.1, "Fiber and Copper SFP Interface Pins and Descriptions"	Refer to Table 5-1 to make sure correct pins for SerDes Media interface are used in the design.		
	Section 5.2, "SerDes Media Interface Connecting to 1000BASE-X Fiber or 1000BASE-T Copper SFPs"	Refer to Figure 5-1 for SerDes media interface to connect to 1000BASE-X fiber SFPs design or to connect to 10/100/1000BASE-T copper SFPs design.		
	Section 5.3, "SerDes Media Interface Connecting to 100BASE-FX Fiber SFPs"	Refer to Figure 5-2 for SerDes media interface to connect to 100BASE-FX fiber SFPs design.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "QSGMII/SGMII/SerDes MAC Interface"	Section 6.1, "QSGMII/SGMII/SerDes MAC Pins and Connection"	Refer to Table 6-1 to make sure correct pins for QSGMII MAC interface are used in the design.		
	Section 6.2, "QSGMII MAC"	Refer to Figure 6-1 for QSGMII MAC interface to connect to two external QSGMII MACs in the design.		
	Section 6.3, "SGMII MAC"	Refer to Figure 6-2 for SGMII MAC interface to connect to two external SGMII MACs in the design.		
	Section 6.4, "SerDes MAC"	Refer to Figure 6-3 and Figure 6-4 for SerDes MAC interface to connect to two external SerDes MACs in the design or connect to 1000BASE-X SFPs or connect to 1000BASE-T SFPs in the design.		
	Section 6.5, "QSGMII/SGMII/SerDes MAC Design Rules"	Refer to this section for QSGMII/SGMII/SerDes MAC Interface PCB design.		
Section 7.0, "Device Clocks"	Section 7.1, "Reference Clock"	Refer to Table 7-1 to select the reference clock frequency and the correct reference clock pins in the design. Follow the layout required in PCB design.		
	Section 7.2, "Single-Ended REFCLK Input"	Refer to Figure 7-1 for single-ended reference input clock circuit design and use the correct resistor divider in the circuit based on Table 7-2 for correct resistors values.		
	Section 7.3, "Differential REFCLK Input"	Refer to Figure 7-2 for the differential reference input clock circuit design and use the correct capacitor AC coupling in the design.		
	Section 7.4, "Media Recovered Clock Output"	Refer to Figure 7-3 for a typical recovered clock circuit design and use the correct recovered clock pins and correct configuration.		
Section 8.0, "1588 Support"	Section 8.1, "1588_DIFF_INPUT_CLK Configuration"	Refer to Table 8-1 to select the correct 1588 differential clock pins pair in the design.		
	Section 8.2, "1588 Serial Timestamp Interface"	Refer to Table 8-2 to use the correct 1588 serial timestamp interface pins in the design. Refer to Figure 8-1 for 1588 serial timestamp interface reference design connection.		
Section 9.0, "Digital Interface and I/O"	Section 9.1, "Serial Management Interface (SMI) Pins"	Refer to Table 9-1 and the descriptions in this section for SMI interface circuit design.		
	Section 9.2, "GPIO Pins"	Refer to Table 9-2 and the descriptions in this section for all GPIO pins in the circuit design.		
	Section 9.3, "JTAG Pins"	Refer to Table 9-3 and the descriptions in this section for all JTAG pins in the circuit design.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 10.0, "Miscellaneous"	Section 10.1, "Reset"	Refer to Table 10-1 to use the correct reset pin and see if the designed reset circuit to meet the reset time requirement.		
	Section 10.2, "Reference Resistor"	Refer to Table 10-2 to select the correct SerDes biasing pins in the design. Make sure to connect a 620Ω ±1% resistor between the **RERDES_REXT_0** and **RERDES_REXT_1** pins. See Figure 10-1 for the design reference.		
	Section 10.3, "LED Pins"	Check if correct LED pins are used based on Table 10-3, current limit resistors, and LED power.		
	Section 10.4, "Analog Bias Pins for Voltage Reference"	Check if the correct pull-down resistor value is used for **REF_REXT_A** pin and the correct pull-down capacitor value is used for **REF_FILT_A** pin based on Figure 10-2.		
	Section 10.5, "Temperature Sensor Diode"	If designing with the temperature sensor diode, see Figure 10-3 as the design reference.		
	Section 10.6, "PHY Address Pins"	Check if the correct PHY address pins are used based on Table 10-4 to configure the correct PHY address the design requires.		
	Section 10.7, "SPI Slave (Optional Use)"	Highly recommended for MACsec applications with more than two slaves on the MDIO bus. Allows 1588 and MaCsec register access.		
	Section 10.8, "Other Pins"	For **COMA_MODE** and **FASTLINK_FAIL** pins, check this section for the correct design.		
	Section 10.9, "Unused and No Connection Pins"	Verify all reserved pins and NC pins are unconnected.		
	Section 10.10, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005011A (05-12-23)	Initial release	

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