Dual Watchdog Timer

HIGHLIGHTS

This section of the manual contains the following major topics:

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Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices. Some dsPIC33/PIC24 devices are dual core and contain both a Master and Slave CPU core. For single core dsPIC33/PIC24 devices, disregard any Slave-specific references.

Please consult the note at the beginning of the **"Watchdog Timer"**, **"Power-Saving Features"** and **"Special Features"** chapters in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

1.0 INTRODUCTION

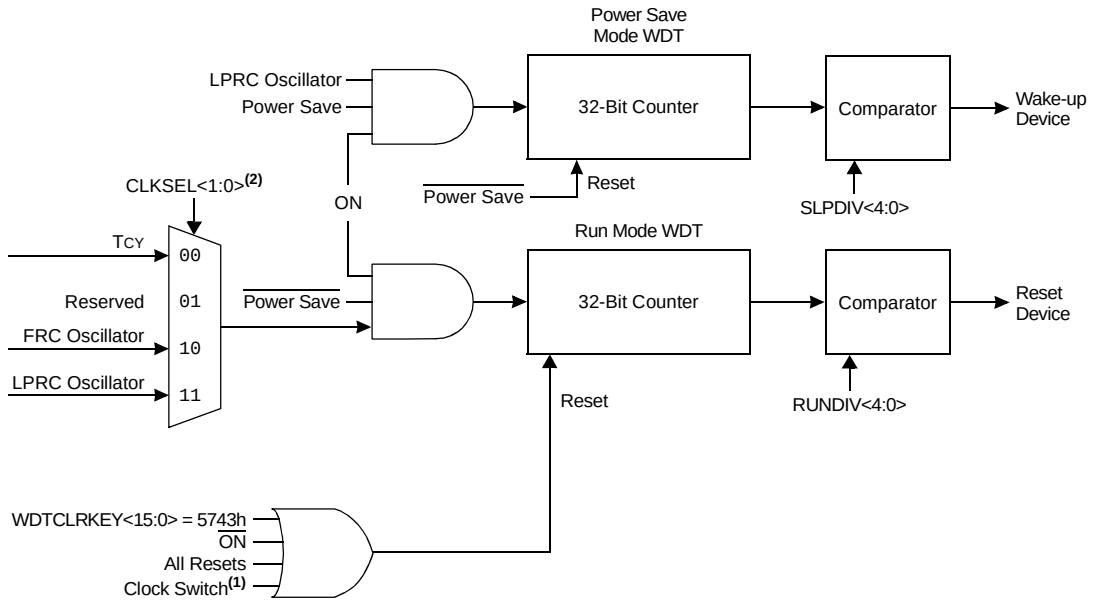
The dsPIC33/PIC24 Dual Watchdog Timer (WDT) is described in this section. Refer to Figure 1-1 for a block diagram of the WDT.

The WDT, when enabled, operates from the internal Low-Power RC (LPRC) oscillator clock source or selectable clock source in Run mode. The WDT can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. The WDT can be configured in Window mode or Non-Window mode. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode (Power Save mode).

The following are some of the key features of the WDT modules:

- Configuration or software controlled
- Separate user-configurable time-out periods for Run and Sleep/Idle modes
- Can wake the device from Sleep or Idle mode
- User-selectable clock source in Run mode
- Operates from LPRC in Sleep/Idle mode

Figure 1-1: Watchdog Timer Block Diagram



Note 1: WDT Reset behavior following a specific clock switch event is device-dependent. Please refer to the **"Watchdog Timer"** section in the specific device data sheet for a description of clock switch events that clear the WDT.

2: The available clock sources are device-dependent.

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2.0 WATCHDOG TIMER CONTROL REGISTERS

The WDT modules consist of the following Special Function Registers (SFRs):

- **WDTCONH: Watchdog Timer Key Register**
  This register is used to clear the WDT to prevent a time-out.
- **WDTCONL: Watchdog Timer Control Register**
  This register is used to enable or disable the Watchdog Timer and enables or disables the windowed operation.
- **RCON: Reset Control Register(2)**
  This register indicates the cause of a Reset.

2.1 Register Map

Table 2-1 provides a brief summary of the related WDT module registers. The corresponding registers appear after the summary, followed by a detailed description of each register.

Table 2-1: Watchdog Timers Register Map

Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTCONH	15:0	WDTCLRKEY<15:0>															
WDTCONL	15:0	ON(3)	—	—	RUNDIV<4:0>(2)					CLKSEL<1:0>(2)		SLPDIV<4:0>(2)					WDTWINEN(3)
RCON(5)	15:0	TRAPR(1)	IOPUWR(1)	—	—	VREGSF(1)	—	CM(1)	VREGS(1)	EXTR(1)	SWR(1)	SWDTEN(1,4)	WDTO	SLEEP	IDLE(1)	BOR(1)	POR(1)

Legend: — = unimplemented, read as '0'.

Note 1: These bits are not associated with the WDT module.

2: These bits reflect the value of the Configuration bits.

3: These bits reflect the status for the Configuration bit if set. If the bit is clear, the value is controlled by software.

4: If the WDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

5: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

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Register 2-1: WDTCONH: Watchdog Timer Key Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
WDTCLRKEY<15:8>							
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
WDTCLRKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to this location using a single 16-bit write.

Register 2-2: WDTCONL: Watchdog Timer Control Register

R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
ON(1,2)	—	—	RUNDIV<4:0>(3)				
bit 15							bit 8

R	R	R-y	R-y	R-y	R-y	R-y	R/W-0, HS
CLKSEL<1:0>(3,5)		SLPDIV<4:0>(3)					WDTWINEN(4)
bit 7							bit 0

Legend:	HS = Hardware Settable bit	y = Value from Configuration bit on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
1 = Enables the Watchdog Timer if it is not enabled by the device configuration
0 = Disables the Watchdog Timer if it was enabled in software

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** WDT Run Mode Postscaler Status bits(3)

bit 7-6 **CLKSEL<1:0>:** WDT Run Mode Clock Select Status bits(3,5)
11 = LPRC oscillator
10 = FRC oscillator
01 = Reserved
00 = SYSCLK

bit 5-1 **SLPDIV<4:0>:** Sleep and Idle Mode WDT Postscaler Status bits(3)

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit(4)
1 = Enables Window mode
0 = Disables Window mode

Note 1: A read of this bit will result in a '1' if the WDT is enabled by the device configuration or by software.

2: The user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

3: These bits reflect the value of the Configuration bits.

4: The WDTWINEN bit reflects the status of the Configuration bit if the bit is set. If the bit is cleared, the value is controlled by software.

5: The available clock sources are device-dependent. Please refer to the **"Watchdog Timer"** chapter in the specific device data sheet for availability.

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Register 2-3: RCON: Reset Control Register(2)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR(1)	IOPUWR(1)	—	—	VREGSF(1)	—	CM(1)	VREGS(1)
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR(1)	SWR(1)	—	WDTO	SLEEP	IDLE(1)	BOR(1)	POR(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit(1)
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit(1)
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit(1)
1 = Flash voltage regulator is active during Sleep
0 = Flash voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit(1)
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit(1)
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit(1)
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit(1)
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

Note 1: These bits are not associated with the WDT module.
2: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

Register 2-3: RCON: Reset Control Register(2) (Continued)

bit 2 **IDLE:** Wake-up from Idle Flag bit(1)
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: These bits are not associated with the WDT module.

2: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

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3.0 WATCHDOG TIMER OPERATION

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction, or wake-up the processor in the event of a time-out while in Sleep or Idle.

The WDT consists of two independent timers, one for operation in Run mode and the other for operation in Power Save mode. The clock source for the Run mode WDT is user-selectable. Each timer has an independent, user-programmable postscaler. Both timers are controlled via a single ON bit; they cannot be operated independently.

If the WDT is enabled, the appropriate WDT counter will increment until it overflows or “times out”. A WDT time-out in Run mode will generate a device Reset. To prevent a WDT Time-out Reset in Run mode, the user application must periodically service the WDT. A time-out in a Power Save mode will wake-up the device.

Note:	The LPRC oscillator is automatically enabled whenever it is being used as a WDT clock source and the WDT is enabled.

3.1 Modes of Operation

The WDT has two modes of operation: Non-Window mode and Programmable Window mode.

In Non-Window mode, software must periodically clear the WDT at any time less than that of the WDT period to prevent a WDT Reset (Figure 3-1). Non-Window mode is selected by clearing the Watchdog Timer Window Enable (WDTWINEN) bit (WDTCONL<0>).

In Programmable Window mode, software can clear the WDT only when the counter is in its final window before a time-out occurs. Clearing the WDT outside this window will cause a WDT Reset (Figure 3-2). There are four window size options: 25%, 37.5%, 50% and 75% of the total WDT period. The window size is set in the device configuration. Programmable Window mode is not applicable when in Power Save mode.

Figure 3-1: Non-Window WDT Mode

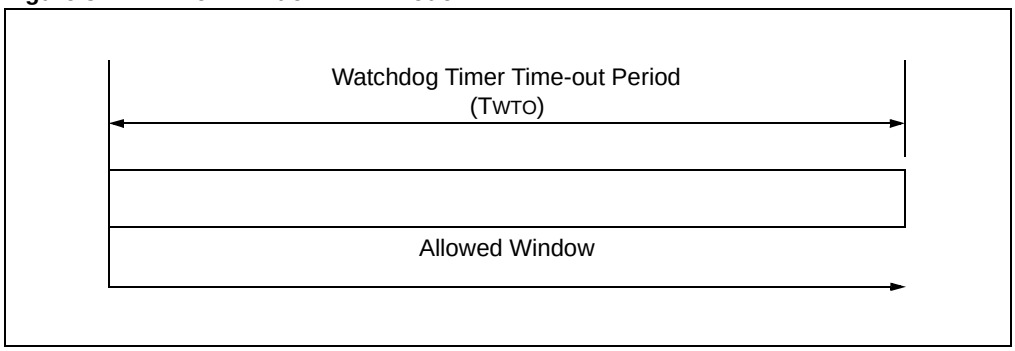
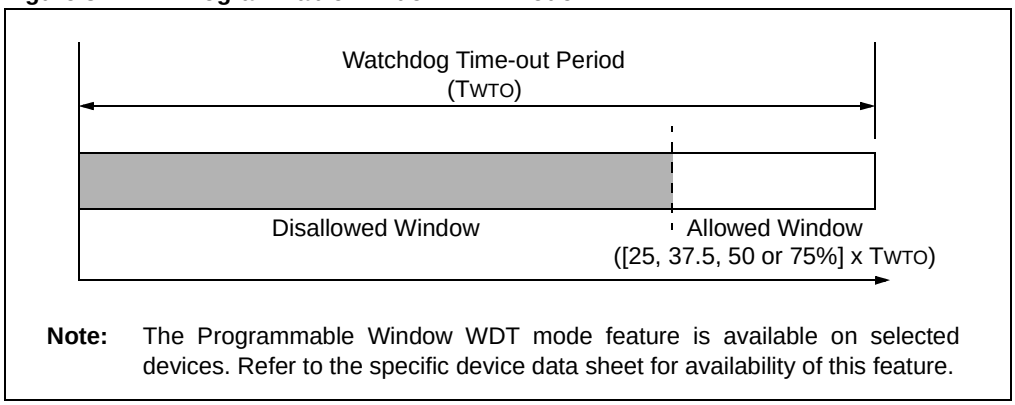


Figure 3-2: Programmable Window WDT Mode



Note:	The Programmable Window WDT mode feature is available on selected devices. Refer to the specific device data sheet for availability of this feature.

3.2 Watchdog Timer Programmable Window

The window size is determined by the Configuration bits, WDTWIN<1:0> and WDTPS<3:0>. In the Programmable Window mode (WDTWINEN = 1), the WDT should be cleared based on the setting of the Window Size Configuration bits, WDTWIN<1:0> (see Figure 3-2). These bit settings are:

- 11 = WDT window is 25% of the WDT period
- 10 = WDT window is 37.5% of the WDT period
- 01 = WDT window is 50% of the WDT period
- 00 = WDT window is 75% of the WDT period

If the WDT is cleared before the allowed window, or if the WDT is allowed to time-out, an NMI is immediately generated and the NMI timer is started. The Window mode is useful for resetting the device during unexpected quick or slow execution of a critical portion of the code. Window operation only applies to the WDT Run mode. The WDT Sleep mode always operates in Non-Window mode.

3.3 Enabling and Disabling the WDT

The WDT is enabled or disabled by the device configuration, or controlled through software by writing a '1' to the ON bit (WDTCONL<15>). See Register 2-2 for more details.

3.3.1 DEVICE CONFIGURATION CONTROLLED WDT

If the FWDTEN Configuration bit is set, the WDT is always enabled. The ON control bit (WDTCONL<15>) will reflect this by reading a '1'. In this mode, the ON bit cannot be cleared in software. The FWDTEN Configuration bit will not be cleared by any form of Reset. To disable the WDT, the configuration must be rewritten to the device. Window mode is enabled by clearing the WINDIS bit in the device configuration. Setting the WINDIS bit enables Window mode.

Note:	The WDT is enabled by default on an unprogrammed device.

3.3.2 SOFTWARE CONTROLLED WDT

If the FWDTEN Configuration bit is '0', the WDT module can be enabled or disabled (the default condition) by software. In this mode, the ON bit (WDTCONL<15>) reflects the status of the WDT under software control; '1' indicates the WDT module is enabled and '0' indicates it is disabled.

3.4 WDT Postscaler

The WDT has 2 user-programmable postscalers: one for Run mode and the other for Power Save mode. The RWDTPS<4:0> Configuration bits set the Run mode postscaler and the SWDTPS<4:0> Configuration bits set the Power Save mode postscaler.

Note:	The Configuration bit names for the postscaler value may vary. Refer to the specific device data sheet for details.

3.4.1 DEVICE CONFIGURATION CONTROLLED WINDOW MODE

Window mode can be disabled by setting the Configuration bit, WINDIS, and can be enabled by clearing the Configuration bit, WINDIS. When the WDT Window mode is enabled by the device configuration, the WDTWINEN bit (WDTCONL<0>) will be set and cannot be cleared by software.

3.4.2 SOFTWARE CONTROLLED WINDOW MODE

If the WINDIS Configuration bit is '0', the WDT Programmable Window mode can be enabled or disabled by the WDTWINEN bit (WDTCONL<0>). A '1' indicates that Programmable Window mode is enabled and a '0' indicates that Programmable Window mode is disabled.

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3.5 WDT Postscaler and Period Selection

The WDT has two independent 5-bit postscalers, one for Run mode and the other for Power Save mode, to create a wide variety of time-out periods. The postscalers provide 1:1 through 1:2,147,483,647 divider ratios (see Table 3-1). The postscaler settings are selected using the device configuration. The WDT time-out period is selected by the combination of the WDT clock source and the postscaler. Refer to Equation 3-1 for the WDT period calculation.

Equation 3-1: WDT Time-out Period Calculation

$$WDT\ Time\text{-}out\ Period = (WDT\ Clock\ Period) \bullet 2^{Postscaler}$$

In Sleep mode, the WDT clock source is LPRC and the time-out period is determined by the SLPDIV<4:0> setting. The LPRC, with a nominal frequency of 32 kHz, creates a nominal time-out period for the WDT of 1 millisecond when the postscaler is at the minimum value.

In Run mode, the WDT clock source is selectable. The time-out period is determined by the WDT clock source frequency and the RUNDIV<4:0> setting.

Note: The WDT module time-out period is directly related to the frequency of the WDT clock source. The nominal frequency of the clock source is device-dependent. The frequency may vary as a function of the device operating voltage and temperature. Please refer to the specific device data sheet for clock frequency specifications.

The available clock sources for Run mode are device-dependent. Please refer to the **"Watchdog Timer"** chapter in the specific device data sheet for available sources.

3.6 WDT Operation in Run Mode

When the WDT expires or is cleared outside the window in Window mode, a device Reset is generated when the NMI counter expires.

3.7 WDT Clock Sources

The WDT Run mode clock source is user-selectable. The clock source is selected by the RCLKSEL<1:0> device bits. The WDT Power Save mode uses LPRC as the clock source.

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3.8 Resetting the WDT(1)

The Run mode WDT counter is cleared by any of the following:

- Any device Reset
- Execution of a DEBUG command
- Detection of a correct write value (0x5743) to the WDTCLRKEYx bits (WDTCONH<15:0>) (refer to Example 3-1)
- A clock switch:(2)
  - Firmware initiated clock switch
  - Two-Speed Start-up
  - Fail-Safe Clock Monitor (FSCM) event
  - Clock switch after wake from Sleep when an automatic clock switch occurs due to oscillator configuration and Two-Speed Start-up is enabled by the device configuration

The Sleep mode WDT counter is reset upon entry into Sleep.

Note 1: The Run mode WDT is not reset when the device enters a Power-Saving mode.

2: WDT Reset behavior following a specific clock switch event is device-dependent. Please refer to the **"Watchdog Timer"** section in the specific device data sheet for a description of clock switch events that clear the WDT.

Example 3-1: Sample Code to Clear the WDT

```
main()
{
   volatile    unsigned *wdtKey;
   wdtKey = (&WDTCONH);

   while(1)
   {
      ... User code ...

      *wdtKey = 0x5743;    // clear WDT by performing a 16-bit write to WDTCON
   }
}
```


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Table 3-1: WDT Time-out Period Settings

Prescaler Values	Time-out Period Based on WDT Clock		
	32 kHz	8 MHz	25 MHz
00000	1 ms	4 μs	1.28 μs
00001	2 ms	8 μs	2.56 μs
00010	4 ms	16 μs	5.12 μs
00011	8 ms	32 μs	10.24 μs
00100	16 ms	64 μs	20.48 μs
00101	32 ms	128 μs	40.96 μs
00110	64 ms	256 μs	81.92 μs
00111	128 ms	512 μs	163.84 μs
01000	256 ms	1.024 ms	327.68 μs
01001	512 ms	2.048 ms	655.36 μs
01010	1.024s	4.096 ms	1.31072 ms
01011	2.048s	8.192 ms	2.62144 ms
01100	4.096s	16.384 ms	5.24288 ms
01101	8.192s	32.768 ms	10.48576 ms
01110	16.384s	65.536 ms	20.97152 ms
01111	32.768s	131.072 ms	41.94304 ms
10000	0:01:06 hms	262.144 ms	83.88608 ms
10001	0:02:11 hms	524.288 ms	167.77216 ms
10010	0:04:22 hms	1.048576s	335.54432 ms
10011	0:08:44 hms	2.097152s	671.08864 ms
10100	0:17:29 hms	4.194304s	1.34217728s
10101	0:34:57 hms	8.388608s	2.68435456s
10110	1:09:54 hms	16.777216s	5.36870912s
10111	2:19:49 hms	33.554432s	10.73741824s
11000	4:39:37 hms	0:01:07 hms	21.47483648s
11001	9:19:14 hms	0:02:14 hms	42.94967296s
11010	18:38:29 hms	0:04:28 hms	0:01:26 hms
11011	1 day 13:16:58 hms	0:08:57 hms	0:02:52 hms
11100	3 days 2:33:55 hms	0:17:54 hms	0:05:44 hms
11101	6 days 5:07:51 hms	0:35:47 hms	0:11:27 hms
11110	12 days 10:15:42 hms	1:11:35 hms	0:22:54 hms
11111	24 days 20:31:24 hms	2:23:10 hms	0:45:49 hms

4.0 INTERRUPTS AND RESET GENERATION

4.1 WDT Time-out in Run Mode

When the WDT times out in Run mode, a device Reset is generated.

Firmware can determine if the cause of the Reset was the WDT time-out in Run mode by testing the WDTO bit (RCON<4>).

Note:	Refer to the “Resets” and “Interrupt Controller” chapters in the specific device data sheet. Also, refer to the **“Reset”** (DS39712) and **“Interrupts”** (DS70000600) sections in the *“dsPIC33/PIC24 Family Reference Manual”* for details.

4.2 WDT Time-out in Power Save Mode

When the WDT module times out in Power Save mode, it wakes the device and the WDT Run mode resumes counting.

To detect a WDT wake-up, the WDTO bit (RCON<4>), SLEEP bit (RCON<3>) and IDLE bit (RCON<2>) can be tested. If the WDTO bit is ‘1’, the event was due to a WDT time-out in a Power Save mode. The SLEEP and IDLE bits can then be tested to determine if the WDT event occurred while the device was awake or if it was in Sleep or Idle mode.

Note:	Refer to the “Resets” and “Interrupt Controller” chapters in the specific device data sheet. Also, refer to the **“Reset”** (DS39712) and **“Interrupts”** (DS70000600) sections in the *“dsPIC33/PIC24 Family Reference Manual”* for details.

4.3 Wake from Power Save Mode by a Non-WDT Event

When the device is awakened from a Power Save mode by a non-WDT NMI interrupt, the Power Save mode WDT is held in Reset and the WDT Run mode continues counting from the prepower save count value.

5.0 RESETS CAUSE AND EFFECT

5.1 Determining the Cause of a Reset

To determine if a WDT Reset has occurred, the WDTO bit (RCON<4>) can be tested. If the WDTO bit is ‘1’, the Reset was due to a WDT time-out in Run mode. Software should clear the WDTO bit to allow correct determination of the source of a subsequent Reset.

5.2 Effects of Various Resets

Any form of device Reset will clear the WDT. The Reset will return the WDTCONH/L registers to the default value and the WDT will be disabled unless it is enabled by the device configuration.

Note:	After a device Reset, the WDT ON bit (WDTCONL<15>) will reflect the state of the FWDTEN bit (FWDT<15>).

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6.0 OPERATION IN DEBUG AND POWER-SAVING MODES

6.1 WDT Operation in Power-Saving Modes

The WDT, if enabled, will continue operation in Sleep mode or Idle mode and can be used to wake-up the device. This allows the device to remain in Sleep or Idle mode until the WDT expires or another interrupt wakes the device. If the device does not re-enter Sleep or Idle mode following a wake-up, the WDT must be disabled or periodically serviced to prevent a WDT Run mode NMI.

6.1.1 WDT OPERATION IN SLEEP MODE

The WDT module may be used to wake the device from Sleep mode. When entering Sleep mode, the WDT Run mode counter stops counting and the Power Save mode WDT begins counting from the Reset state, until it times out, or the device is woken up by an interrupt. When the WDT times out in Sleep mode, the device wakes up and resumes code execution, sets the WDTO bit (RCON<4>), and resumes the Run mode WDT.

6.1.2 WDT OPERATION IN IDLE MODE

The WDT module may be used to wake the device from Sleep mode. When entering Idle mode, the WDT Run mode counter stops counting and the Power Save mode WDT begins counting from the Reset state, until it times out, or the device is woken up by an interrupt. The device wakes up and resumes code execution, sets the WDTO bit (RCON<4>), and resumes the Run mode WDT.

6.2 Time Delays During Wake-up

There will be a time delay between the WDT event in Sleep and the beginning of code execution. The duration of this delay consists of the start-up time for the oscillator in use. Unlike a wake-up from Sleep mode, there are no time delays associated with wake-up from Idle mode. The system clock is running during Idle mode; therefore, no start-up delays are required at wake-up.

6.3 WDT Clock Sources in Power Save Mode

The WDT clock source for Power Save mode is not user-selectable. The clock source is LPRC.

6.4 WDT Operation in Debug Mode

The WDT should be disabled in Debug mode to prevent a time-out.

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7.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Dual Watchdog Timer module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 family of devices.

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8.0 REVISION HISTORY

Revision A (March 2016)

This is the initial version of this document.

Revision B (June 2018)

Changes device family name to dsPIC33/PIC24.

Removes the Advance Information watermark from page footers.

NOTES:

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