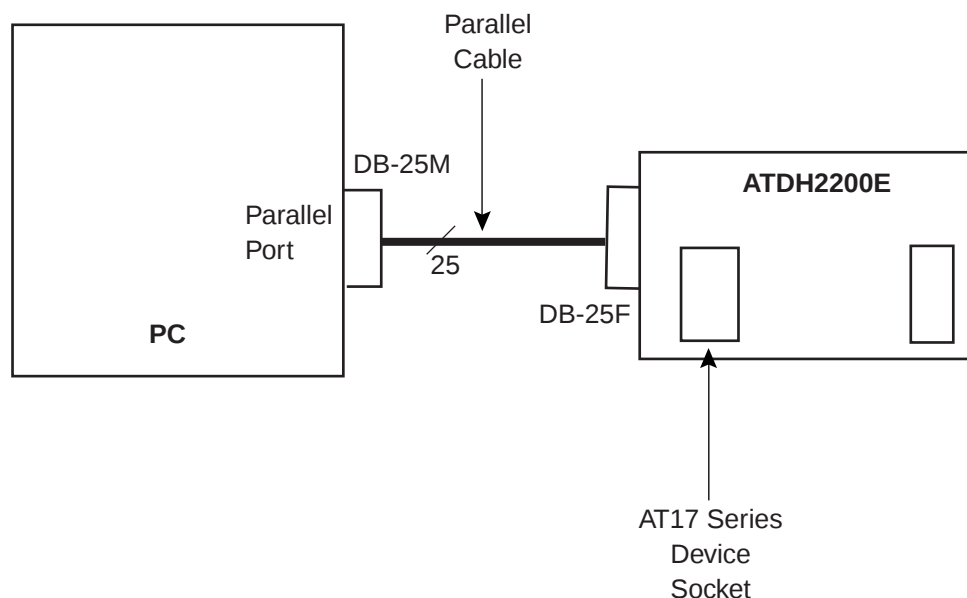


Drop-In/Stand-alone Programming Circuits for AT17 Series Configurators with Atmel and Xilinx® FPGAs

Atmel AT17 ⁽¹⁾ series configurators use a simple serial-access procedure to configure one or more Field Programmable Gate Arrays (FPGAs) or Field Programmable System Level Integrated Circuits (FPSLIC™) devices.

This application note provides the drop-in/stand-alone programming circuits for AT17 Series devices with Atmel and Xilinx FPGAs. For Drop-In/Stand-alone Programming, the configurator is programmed before dropping into the circuit that will configure the FPGA, FPSLIC™ or the microcontroller, see Figure 1.

Figure 1. ATDH2200E Stand-alone Device Programming



1. AT17 = AT17LV/FXXX

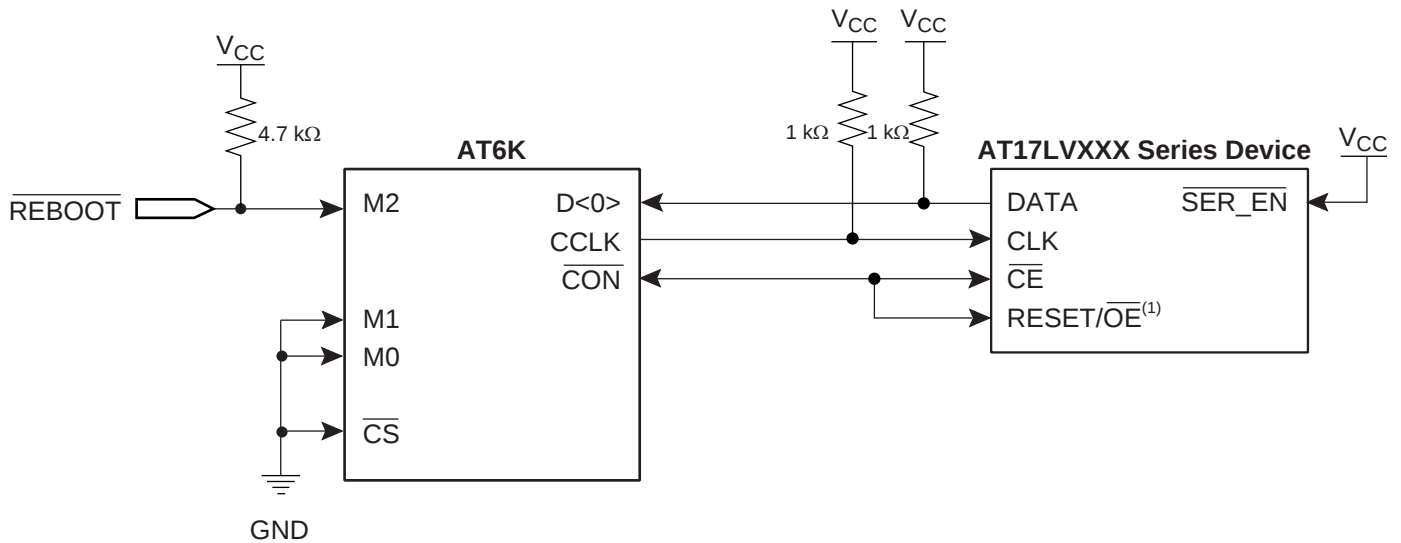


AT17 Series FPGA Configuration Memory

Application Note

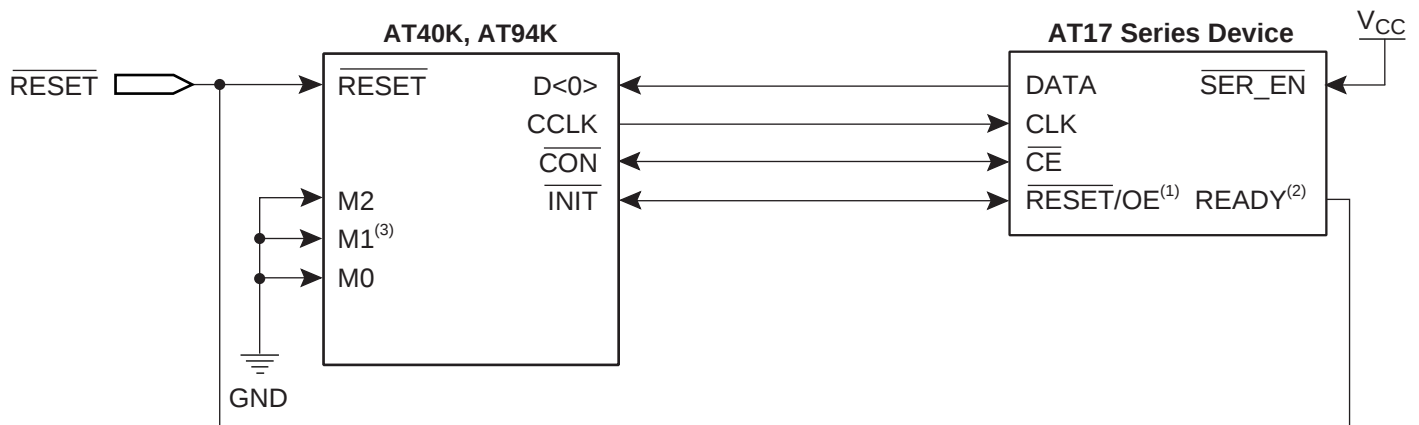


Figure 2. Drop-In Programming of AT17LVXXX Series EEPROMs for AT6K FPGA Applications



Note: 1. Reset polarity level of the configurator must be set to active High ($\overline{\text{RESET/OE}}$) by a programmer.

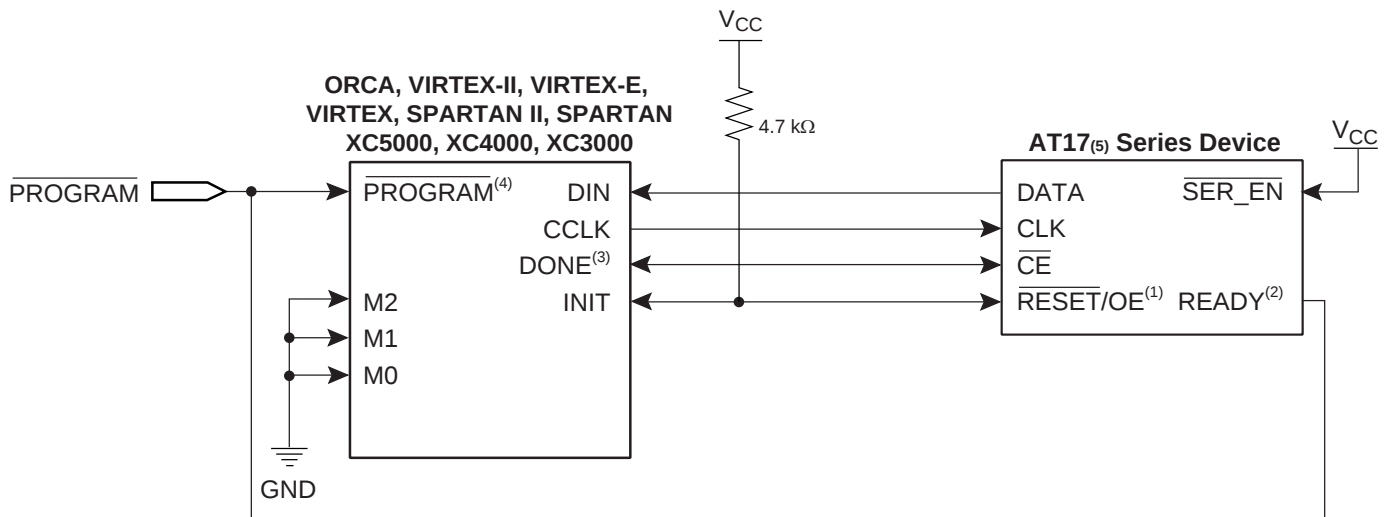
Figure 3. Drop-In Programming of AT17 Series EEPROMs for AT40K FPGA and AT94K FPSLIC Applications



- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by a programmer if an AT17LVXXX or an ATFSXXX series configurator is used.
 2. Use of the READY pin is optional.
 3. Pin M1 is not available for AT94K devices.
 4. ATFSXXX series configurator can be used in this circuit for AT94K FPSLIC applications.

Drop-In/Stand-alone Circuits for Atmel and Xilinx FPGAs

Figure 4. Drop-In Programming of AT17⁽⁵⁾ Series EEPROMs for Xilinx and Lattice® Applications



- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by a programmer if an AT17LVXXX or an AT17NXXX series configurator is used.
 2. Use of the READY pin is optional.
 3. A 330Ω external pull-up resistor on the DONE pin is required for Virtex® and Virtex-II FPGAs. Xilinx FPGAs can use $\overline{\text{LDC}}$ instead of the DONE pin.
 4. Xilinx FPGAs can use $\overline{\text{RESET}}$ instead of the $\overline{\text{PROGRAM}}$ pin. ORCA® FPGAs can use $\overline{\text{PRGM}}$ instead of the $\overline{\text{PROGRAM}}$ pin.
 5. AT17NXXX series configurator could also be used.



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