

Complementary Output Generator Technical Brief

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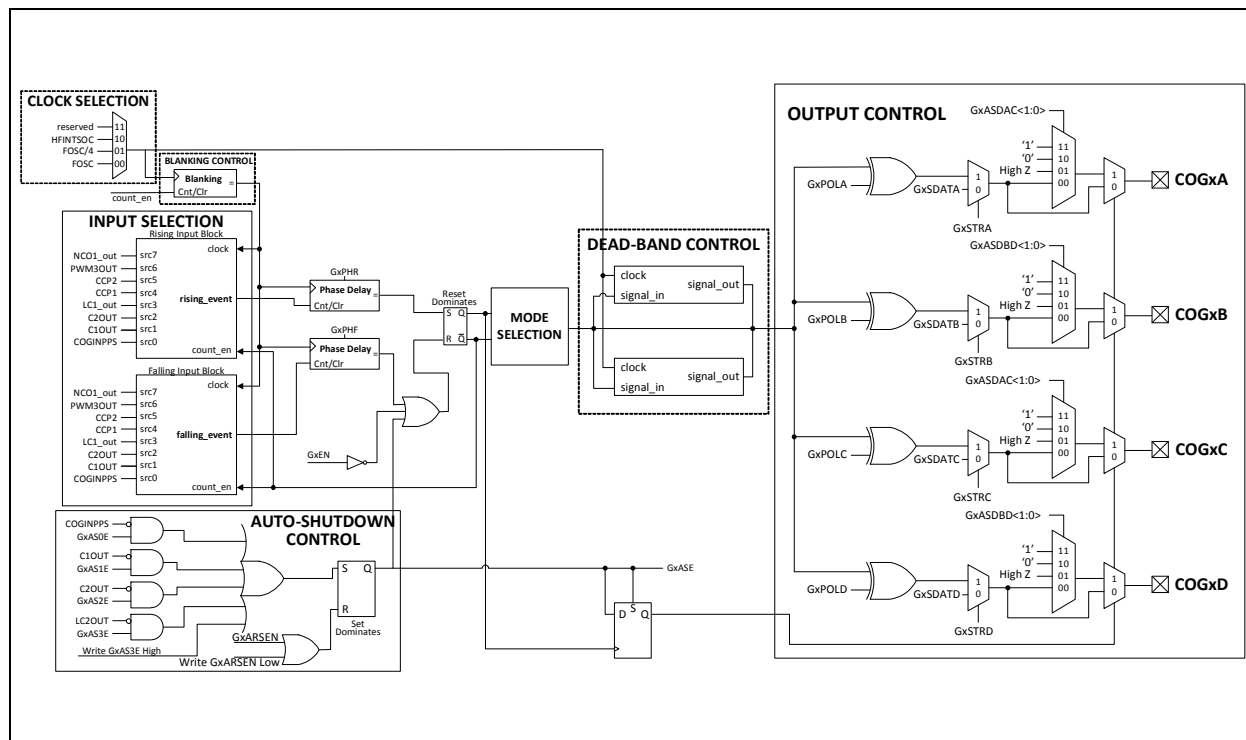
INTRODUCTION

The ability to manipulate the period and duty cycle of a single or complementary PWM output by the two independent input sources is a powerful feature of a waveform generator. This feature, together with fine control of key parameters such as dead band, blanking, phase, polarity, auto-shutdown and auto-recovery, make the waveform generator an excellent candidate for power converter applications. The Complementary Output Generator (COG) in Microchip's 8-bit microcontrollers offers these features with no processor overhead. This technical brief describes the COG features, method of configuration, and calculation of important values.

BLOCK DIAGRAM

Figure 1 shows the simplified block diagram of the COG peripheral. Each block in Figure 1 represents the COG's features. The rising and falling event sources can be selected independently to produce a single or complementary output waveform. The complementary output can be further modified in different modes of operation such as Push-Pull, Half-Bridge, Full-Bridge and Steering PWM. Various clock sources can be selected and used as a reference to generate phase, dead band and blanking times. Each COG output pin has individual output enable control and the polarity of these pins can be controlled individually as well. In addition, the COG output can be terminated immediately during a Fault event and can also be recovered when the Fault event is removed.

FIGURE 1: COG SIMPLIFIED BLOCK DIAGRAM



INPUT SOURCE SELECTION

The COG combines two selectable independent sources to generate single or complementary PWM outputs. The two independent sources are categorized as rising event sources and falling event sources. The rising and falling event sources can be an external input to the COGxIN pin or an output from another internal peripheral. The rising event controls the PWM output period while the falling event controls the PWM output duty cycle. The rising event source is selected by setting the Rising Event Input Source bits (GxRIS) in the COGxRIS register and the falling event source is selected by setting the Falling Event Input Source bits (GxFIS) in the COGxFIS register. When the rising and falling events are selected with the same input source and no delays, the desired PWM output period and duty cycle are the same as the selected input source. The COG's input sources and bit selection settings may vary from device to device. Some of the available peripherals used as input sources are the following: Comparator, CCP (Capture, Compare, PWM), NCO (Numerically Controlled Oscillator) and CLC (Configurable Logic Cell) output. The selected peripheral should be configured first, before using it as the COG's input. For a device that has Peripheral Pin Select (PPS), the COGxIN input pin can be moved to other input pins, using the PPS Input Selection register (xxxPPS). By changing the "xxx" notation in the register name to COGxIN, any available I/O pin can be selected as COGxIN. For example, to use RC0 as the COGxIN pin, the xxxPPS becomes COGxINPPS. And this register should be set to a corresponding value defined in the data sheet to assign RC0 as COGxIN pin.

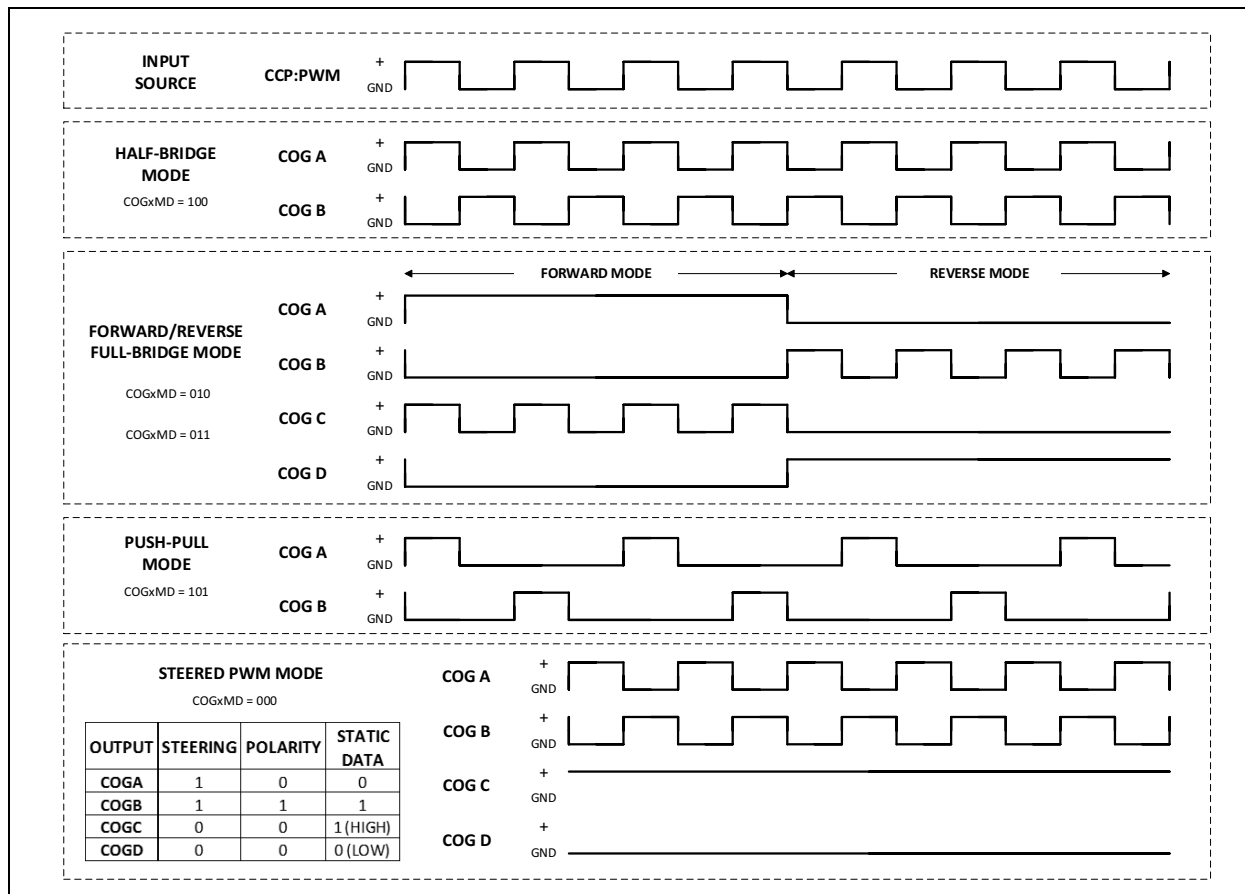
In addition to selectable input event sources, the methods of detection can also be selected in each individual input source. The event input detection may be selected as level or edge-sensitive. The COGxRSIM register is used to select the method detection for rising event input while COGxFSIM is used to select the method of detection for falling event input. In general, events that are driven from a periodic source should be edge-detected and events that are derived from voltage thresholds at the target circuit should be level-sensitive.

MODE SELECTION

The COG output can be modified in different modes. These modes are:

- Half-Bridge mode
- Forward Full-Bridge mode
- Reverse Full-Bridge mode
- Push-Pull mode
- Steering PWM mode

These modes can be selected by setting the COG Mode Selection bits (GxMD). [Figure 2](#) shows COG output in different modes of operation. In Half-Bridge mode, two output signals are generated as true and inverted version of the input. In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth output replicates the input data signal. To change between Forward and Reverse Full-Bridge mode, it only requires toggling the MD<0> bit of COGxCON0. In Push-Pull mode, the output signals generated are alternating copies of the input. In Steered PWM mode, enabling the Steering Control bits (GxSTRA:D) allows the input event signal to be replicated to any or all of the four COG outputs (COGxA:D). When Steering Enable bits (GxSTRA:D) are cleared, the COG output (COGxA:D) signal is determined by the Static Output Data bits (GxSDATA:D). Using a Synchronous Steering mode, the next rising input event is required, before the changes on GxSTRA:D bits take effect. While in Non-Synchronous Steering mode, changes on GxSTRA:D bits take effect on the next instruction cycle.

FIGURE 2: COG MODE OF OPERATIONS

CLOCK SOURCE SELECTION

The reference clock for dead band, phase, and blanking control can be selected from several different clock sources. This is possible by using the COG Clock Selection bits (GxCs). Like input sources, the available clock sources may vary from device to device.

When the selected clock source is HFINTOSC (16 MHz) and the input source selected remain active, the COG can still operate even when the device is put into Sleep mode.

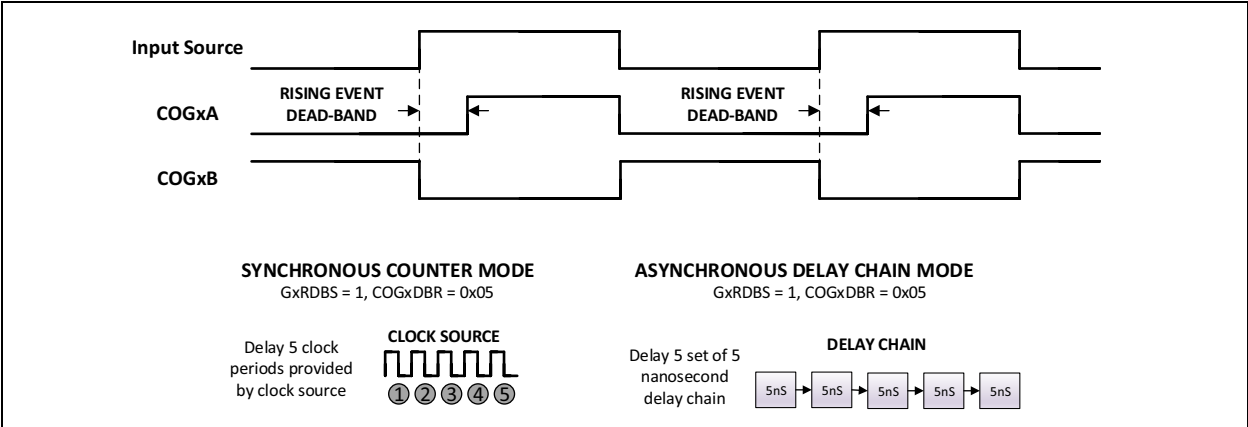
DEAD-BAND CONTROL

Dead-band control provides non-overlapping output signals during Half-Bridge mode and changing direction during Full-Bridge mode. The non-overlapping signal prevents the cross conduction of external power switches. A maximum of a 6-bit value can be written in Rising Dead-Band Counter register (COGxDBR) and Falling Dead-Band Counter register (COGxDBF) to indicate the count delay. When the Dead-Band Timer mode is selected as Synchronous Counter through Rising/Falling Timing Source Select bits (GxRDBS/GxFDBS) of the COGxCON1 register, the dead band is timed by counting COG clock source period from zero to a value written in the dead-band counter register. On the other hand, when Dead-Band Timer mode is selected as Asynchronous Delay Chain through Rising/Falling Timing Source Select bits (GxRDBS/GxFDBS) of the COGxCON1 register, the dead band is timed by counting the desired number of delay elements set in dead-band counters. Each delay element has a nominal five nanoseconds.

DEAD-BAND RISING EDGE CONTROL

In [Figure 3](#), when COGxB goes low, the rising edge dead band starts to count and delay the COGxA before it goes high.

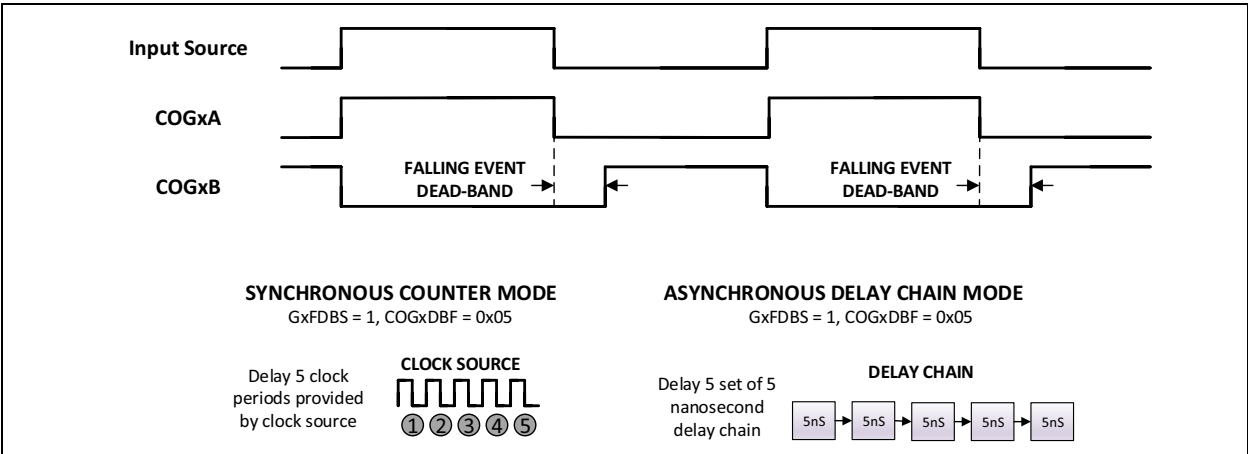
FIGURE 3: RISING EVENT DEAD BAND



DEAD-BAND FALLING EDGE CONTROL

In [Figure 4](#), when COGxA goes low, the falling edge dead band starts to count and delay the COGxB before it goes high.

FIGURE 4: FALLING EVENT DEAD BAND

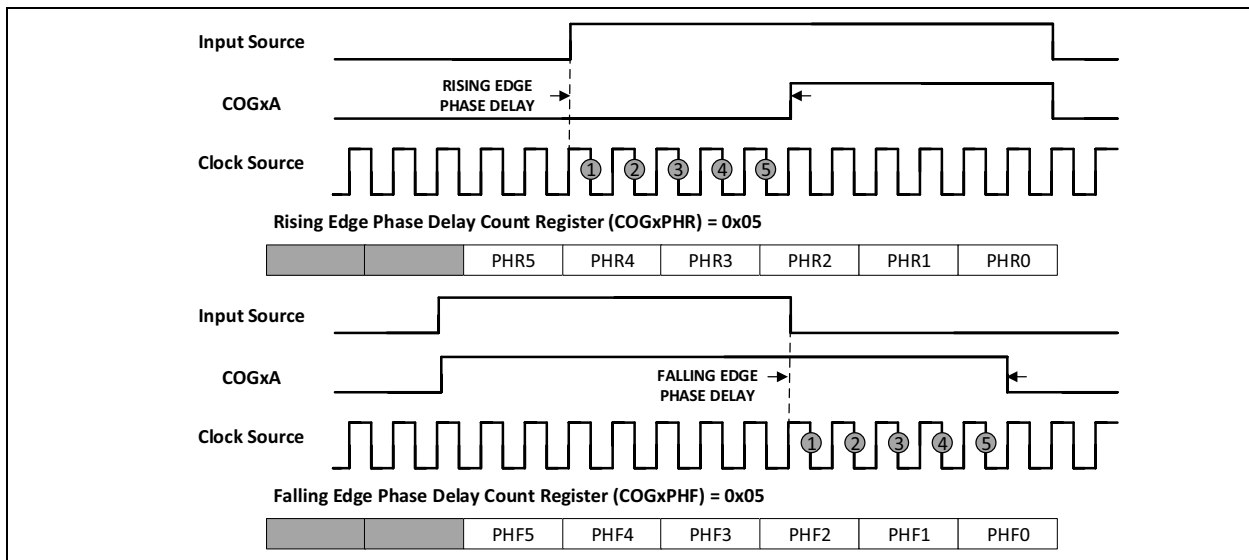


PHASE-DELAY CONTROL

As the name implies, the phase-delay control delays the phase or the assertion of either or both rising and falling input events. This can be accomplished by writing a non-zero to maximum 6-bit value in the Rising Edge Phase-Delay Count register (COGxPHR) and Falling Edge Phase-Delay Count register (COGxPHF). The value in the COGxPHR or COGxPHF registers indicates the count of the clock delay period before the rising or falling event is asserted, respectively.

As shown in Figure 5, when the rising input event source goes high, the rising edge phase delay starts to delay the rising of COGxA. Also, when the falling input event source goes low, the falling edge phase delay starts to delay the falling of COGxA.

FIGURE 5: PHASE-DELAY CONTROL



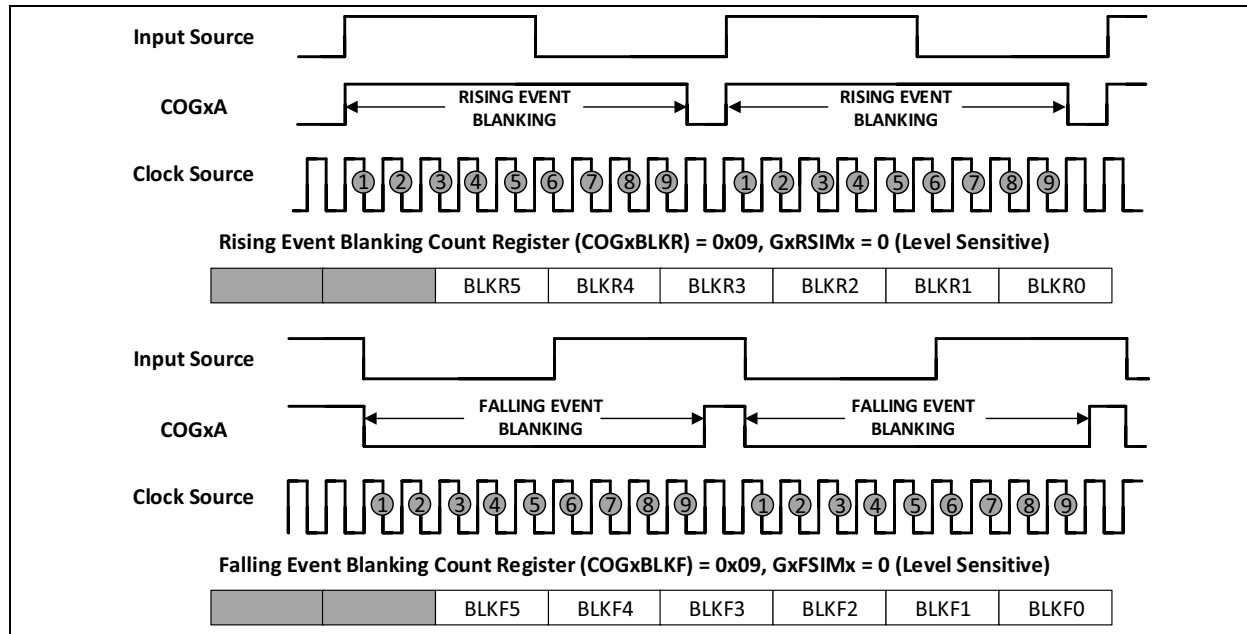
BLANKING CONTROL

Input blanking allows the rising and/or falling event inputs to be ignored, masked or blanked for a short period of time. This function is useful when counting off the false triggering signal, which is usually generated by the switching of external power components. Input blanking is made possible by writing a non-zero to maximum 6-bit value in the Rising Event Blanking Count register (COGxBLKR) and Falling Event Blanking Count register (COGxBLKF). The value in the COGxBLKR or COGxBLKF registers indicates the count of the clock delay to inhibit the rising and falling event inputs from triggering the falling and rising event, respectively.

As shown in Figure 6, when the rising edge of the input event source goes high, the rising event blanking starts to count to inhibit the falling event input from triggering the input falling event. Also in Figure 6, when the falling

edge of the input event source goes low, the falling event blanking starts to count to inhibit the rising event input from triggering the rising event.

FIGURE 6: RISING EVENT BLANKING CONTROL



The COGxDBR, COGxDBF, COGxPHR, COGxPHF, COGxBLKR, and COGxBLKF are double-buffered registers. When COG Enable bit (GxEN) is '0', writing these registers loads the buffers immediately. However, when EN is '1', then software must set the Load Buffer bit (GxLD) of the COGxCON0 register, and the buffers will be loaded at the next falling edge of the COG input signal. This operation allows the changes to the dead band, phase and blanking registers to occur simultaneously and avoid unintended operation that may happen as a result of delays between each delay write.

AUTO-SHUTDOWN

Auto-shutdown can be triggered by one of the available Fault event sources or by software execution. The Fault event source can be selected using Auto-Shutdown Control register (COGxASD1).

Auto-shutdown is an active-low operation. When the selected Fault event goes low, the output pin will be in shutdown state. The output pin shutdown state can be selected as forced-low, forced-high, tri-state or inactive by setting the Auto-Shutdown Override Level Select bits (GxASDBD/GxASDAC). Also, setting the GxASE bit of the Auto-Shutdown Control register (COGxASD0) in software will force the output into a shutdown state.

The shutdown state can be held until cleared by the software or cleared automatically. Clearing the auto-shutdown automatically requires enabling auto-restart. Auto-restart can be enabled using the Auto-Restart Enable bit (GxARSEN).

OUTPUT ENABLE

Each COG output pin has individual output pin enable control. When an output pin enable is cleared, the COG has no connection to the output pin. When the output enable is set, the override value or active waveform is applied to the pin per the internal port priority selection. The output control can be completely disabled by clearing the module enable bit. Output enables are selected in the COG using the Output Enable bits (OEA:D). Setting the bit enables the output. By default, the complementary drive is configured as inactive in output COGxA/C while the complementary drive is configured as active in the COGxB/D output.

Some devices allow the COG output to be moved to its alternate pins. Using the Alternate Pin Function register (APFCON), the COG output function can be moved between its default and alternate pins.

For the device that has Peripheral Pin Select (PPS), there is no output control available. Instead, each device pin has an individual output selection controlled by the PPS register. When the output is not selected in the PPS register, the peripheral has no connection to the output pin.

POLARITY CONTROL

Polarity control can be set to invert the output signal. The polarity of each COG output can be selected independently. When the output polarity bit is set, the corresponding output will become active-low. Clearing the output polarity bit configures the corresponding output as active-high. Therefore, in the case of two complementary outputs, inverting either one of the outputs generates two of the exact same output signals. Output polarity is selected using the Output Polarity bits (GxPOLA:D).

DEAD BAND, PHASE DELAY, AND BLANKING TIME CALCULATION AND UNCERTAINTY

Using Equation 1, the dead band, phase delay and blanking time can be calculated.

EQUATION 1: TIME CALCULATION

$$Time_{(min)} = \frac{Count}{Frequency_{(Clock\ Source)}}$$

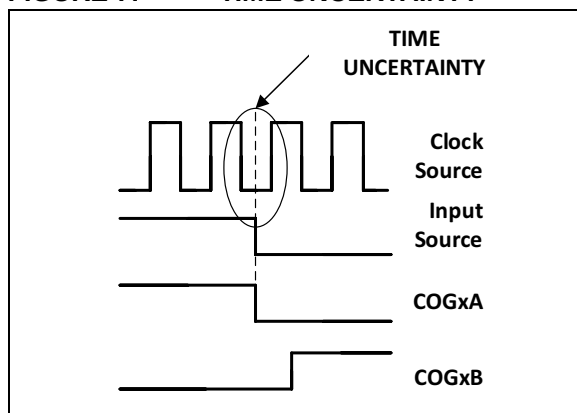
$$Time_{(max)} = \frac{Count + 1}{Frequency_{(Clock\ Source)}}$$

Where:

TIME	COUNT
Rising Dead-Band	COGxDBR
Falling Dead-Band	COGxDBF
Rising Phase Delay	COGxPHR
Falling Phase Delay	COGxPHF
Rising Event Blanking	COGxBLKR
Falling Event Blanking	COGxBLKF

However, there are instances that the time calculation is not accurate. This is referred to as time uncertainty, see Figure 7.

FIGURE 7: TIME UNCERTAINTY



When the rising and falling sources that trigger these timers come from asynchronous inputs such as the external input to COGxIN pin, it creates an uncertainty in the time. Time uncertainty can be calculated using Equation 2.

EQUATION 2: TIME UNCERTAINTY CALCULATION

$$Time_{(uncertainty)} = Time_{(max)} - Time_{(min)}$$

$$Time_{(uncertainty)} = \frac{1}{Frequency_{(Clock\ Source)}}$$

IMPLEMENTING COG USING MICROCHIP CODE CONFIGURATOR (MCC)

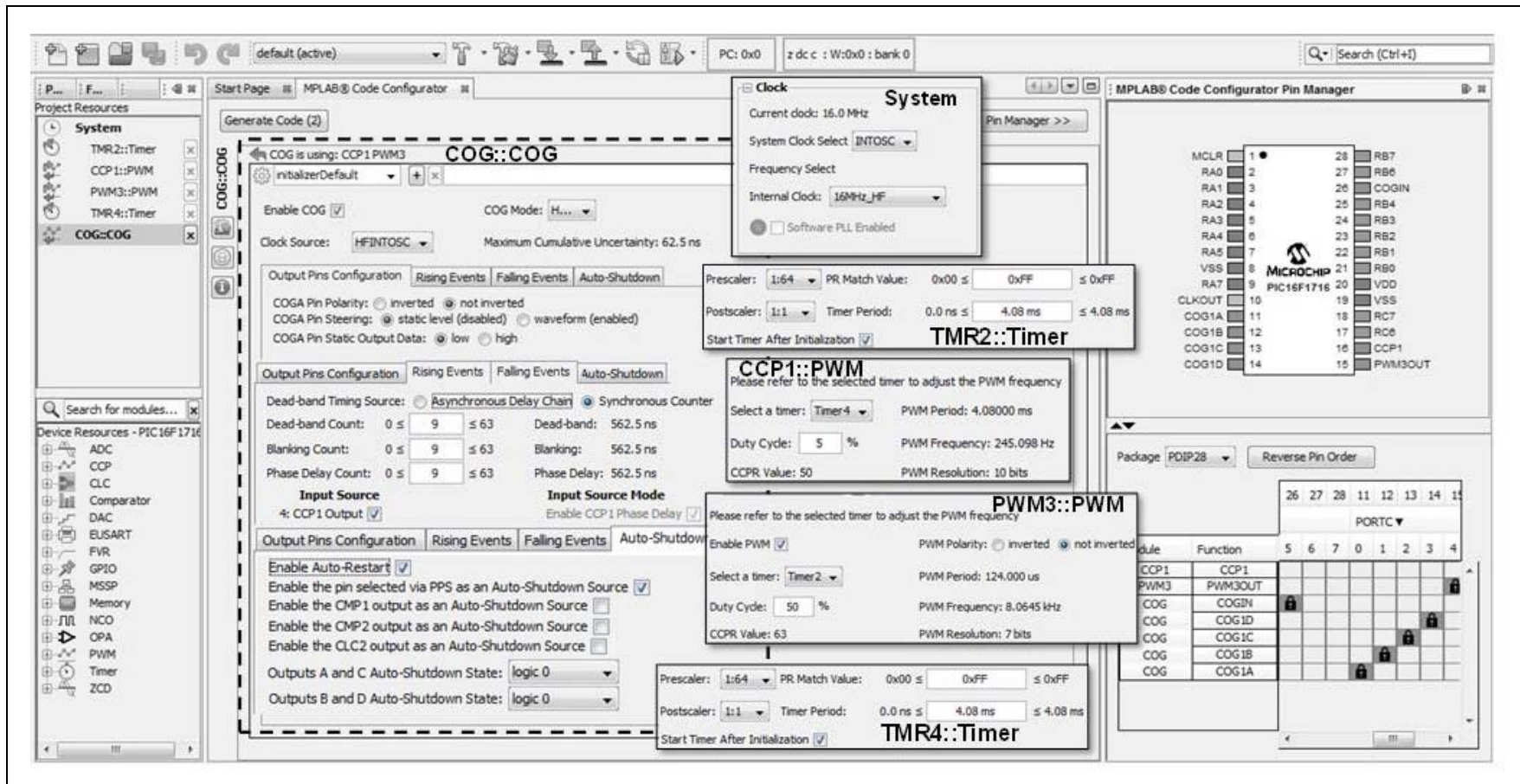
In this section, MPLAB® Microchip Code Configurator (MCC) is utilized to easily configure the COG module. The MPLAB Code Configurator (MCC) is a user-friendly plug-in tool for MPLAB® X IDE, which generates drivers for controlling and driving peripherals of PIC® microcontrollers, based on the settings and selections made in its Graphical User Interface (GUI). For information on how to install and setup the MCC in MPLAB® X IDE, refer to “MPLAB® Microchip Code Configurator User Guide”, which can be found at www.microchip.com.

The following steps will guide on how to configure the COG module in PIC16F1716 using MCC. The CCP1's Pulse-Width Modulation (PWM) output signal is used as the rising event input source and the Pulse-Width Modulation 3 (PWM3) output signal as the falling event input source. The High-Frequency Internal Oscillator (HFINTOSC) is used as the reference clock for dead band, blanking and phase-delay time. After a successful configuration, the COG produces two pair of complementary waveform outputs, which can be terminated using an active-low external switch connected in COGxIN for shutdown control.

1. Navigate to: “**Tools – Embedded – MPLAB Code Configurator**” to launch the MCC.
2. Set the desired Configuration registers and the system clock source on the “**System**” label inside of MPLAB X under the “**Project Resources**” window.
3. Configure the rising event input source to be used:
 - **CCP Configuration**
 - Under the device resources panel. Expand “**CCP1**” and then double-click on “**PWM**” to bring the module up to the “**Project Resources**” panel.

- In the center panel, after clicking the **"PWM2::PWM"** in the **"Project Resources"**, set the duty cycle to be 50% and Timer2 as timer source. When Timer2 is selected as timer source for CCP1, the configurator will automatically add it in **"Project Resources"**.
- **Timer4 Configuration**
 - In the center panel, after clicking the **"TMR4::Timer"** in the **"Project Resources"**, set the Prescaler to 1:64 in the drop-down menu and the **"PR Match Value"** to 0xFF.
 - Check the **"Start Timer After Initialization"** checkbox.
- 4. Configure the falling event input source to be used.
- **PWM3 Configuration**
 - Under the device resources panel. Expand **"PWM"** and then double-click on **"PWM3::PWM"** to bring the module up to the **"Project Resources"** panel.
 - In the center panel, after clicking the **"PWM3::PWM"** in the **"Project Resources"**, set the duty cycle to be 50% and Timer2 as timer source. When Timer2 is selected as timer source for PWM, the configurator will automatically add it in **"Project Resources"**.
- **Timer2 Configuration**
 - In the center panel, after clicking the **"TMR2::Timer"** in the **"Project Resources"**, set the Prescaler to 1:64 in the drop-down menu and the **"PR Match Value"** to 0xFF.
 - Check the **"Start Timer After Initialization"** checkbox.
- 5. After configuring the rising/falling event input source, COG can now be configured by bringing the module up to the **"Project Resources"** panel. The next instructions will configure the COG.
- 6. In the center panel, after clicking the **"COG::COG"** in the **"Project Resources"**, check the **"Enable COG"** checkbox and set the **'COG Mode'** as Half-Bridge mode in the drop-down menu.
- 7. Under the **"Rising Events"** tab, check the **"CCP1 Output"** to configure it as the Input Source for rising event. Also, under the **"Falling Events"** tab, check the **"PWM3 Output"** to configure it as the Input Source for falling event.
- 8. Set HFINTOSC (16 MHz) in the dropdown menu of **"Clock Source"** as reference clock source.
- 9. To enable the COG output, expand the **"MPLAB® Code Configurator Pin Manager"** on the right side of the screen. Click the blue lock next to COG1A/B/C/D to assign them to the following: COG1D = PortC3 (RC3), COG1C = PortC2 (RC2), COG1B = PortC1 (RC1), COG1A = PortC0 (RC0).
- In the center panel under the **"Output Pins Configuration"**, select **"not inverted"** for COGA/B/C/D Pin Polarity.
- The **"COGA/B/C/D Pin Steering"** and **"COGA/B/C/D Pin Static Output Data"** only apply on steered PWM mode and asynchronous steered PWM mode. Setting the COGA/B/C/D Pin Steering to **"static level (disabled)"** will override the COG output with the value set on the **"COGA/B/C/D Pin Static Output Data"**. On the other hand, setting the COGA/B/C/D Pin Steering to **"waveform (enable)"** will enable the input event signal to be replicated on the output pin.
- 10. Under the **"Auto-Shutdown"** Tab, check the **"Enable the pin select via PPS as an Auto-Shutdown Source"** and **"Enable Auto-Restart"** checkbox to activate the auto-shutdown and restart feature.
 - To choose which I/O pin will be used as COGxIN, expand the **"MPLAB® Code Configurator Pin Manager"** on the right side of the screen. Click the blue lock on PortB5 (RB5) next to COGIN. To avoid shutdown, drive the COGIN (RB5) pin to high.
 - Set the **"Outputs A and C Auto-Shutdown State"** and **"Outputs B and D Auto-Shutdown State"** to logic 0 in the drop-down menu.
- 11. In configuring the dead band, blanking and phase-delay control, under the **"Rising Events"** and **"Falling Events"** tab, assign any value from 1-63 on **"Dead-band Count"**, **"Blanking Count"** and **"Phase-Delay Count"**. Also, check the **"Enable CCP1 Phase Delay"** and **"Enable PWM3 Phase Delay"** checkbox under the **"Rising Events"** and **"Falling Events"** tab to enable the phase delay.
- 12. Click the **"Generate Code"** button in the top left corner of the center panel. This will generate a **'main.c'** file to the project automatically. It will also initialize each module and leaves an empty while(1) loop for custom code entry. See [Figure 8](#) for the MCC User Interface for COG, and [Example 1](#) for the generated initialization code for the COG module.

FIGURE 8: MCC USER INTERFACE FOR COG



EXAMPLE 1: MCC GENERATED CODE FOR COG

```
void COG_initializerDefault(void)
{
    // Reset double buffered register COG1CON0
    COG1CON0 = 0x00;
    // Set the COG to the options selected in MPLAB® Code Configurator
    // G1POLA Active high; G1POLC Active high; G1POLB Active high; G1POLD Active high;
    // G1FDBS COGx_clock and COGxDBF; G1RDBS COGx_clock and COGxDBR;
    COG1CON1 = 0x00;
    // G1RIS1 disabled; G1RIS3 disabled; G1RIS0 disabled; G1RIS2 disabled; G1RIS5 disabled;
    // G1RIS4 enabled; G1RIS7 disabled; G1RIS6 disabled;
    COG1RIS = 0x10;
    // G1RSIM0 immediate; G1RSIM1 immediate; G1RSIM2 immediate; G1RSIM3 immediate;
    // G1RSIM4 after rising event phase delay; G1RSIM5 immediate; G1RSIM6 immediate; G1RSIM7
    // immediate;
    COG1RSIM = 0x10;
    // G1FIS6 enabled; G1FIS7 disabled; G1FIS1 disabled; G1FIS0 disabled; G1FIS5 disabled;
    // G1FIS4 disabled; G1FIS3 disabled; G1FIS2 disabled;
    COG1FIS = 0x40;
    // G1FSIM2 immediate; G1FSIM1 immediate; G1FSIM0 immediate; G1FSIM6 after falling event
    // phase delay; G1FSIM5 immediate; G1FSIM4 immediate; G1FSIM3 immediate; G1FSIM7
    // immediate;
    COG1FSIM = 0x40;
    // G1ASDBD logic 0; G1ARSEN enabled; G1ASDAC logic 0; G1ASE not shutdown;
    COG1ASD0 = 0x68;
    // G1AS2E disabled; G1AS3E disabled; G1AS1E disabled; G1AS0E enabled;
    COG1ASD1 = 0x01;
    // G1SDATB static data low; G1SDATC static data low; G1SDATD static data low; G1SDATA
    // static data low; G1STRA static level; G1STRB static level; G1STRC static level; G1STRD static
    // level;
    COG1STR = 0x00;
    // G1DBR 10;
    COG1DBR = 0x0A;
    // G1DBF 10;
    COG1DBF = 0x0A;
    // G1BLKR 10;
    COG1BLKR = 0x0A;
    // G1BLKF 10;
    COG1BLKF = 0x0A;
    // G1PHR 10;
    COG1PHR = 0x0A;
    // G1PHF 10;
    COG1PHF = 0x0A;
    // G1LD transfer complete; G1EN enabled; G1MD Half-Bridge mode; G1CS HFINTOSC;
    COG1CON0 = 0x94;
}
```

TABLE 1: SUMMARY OF 8-BIT MICROCONTROLLER FAMILY WITH COG MODULE

Family	Input Sources	Clock Sources	Shutdown Sources	Modes
PIC1X(L)F752/3	HLT2 HLT1 TMR2 COG1IN (COG1FLT) CCP1 C2 C1	HFINTOSC Fosc/4 Fosc	LC1OUT COG1IN	Push-Pull Steering mode
PIC16(L)F170X	PWM3 CCP2 CCP1 CLC1 C2 C1 COG1IN	HFINTOSC Fosc/4 Fosc	C1 C2 CLC2 COG1IN	Half-Bridge Full-Bridge Push-Pull Steering mode
PIC16(L)F171x	PWM3 CCP2 CCP1 CLC1 C2 C1 COG1IN	HFINTOSC Fosc/4 Fosc	C1 C2 CLC2 COG1IN	Half-Bridge Full-Bridge Push-Pull Steering mode

CONCLUSION

This technical brief covers the COG peripheral features and capabilities. It also provides the calculations of relevant value such as dead band, blanking and phase-delay time. The configuration of COG is demonstrated using code configurator MCC and example initialization code is generated using MCC, as well.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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