AN1194

Recommended Usage of Microchip UNI/O® Bus-Compatible Serial EEPROMs

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INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry-standard serial communication protocols for the UNI/O® bus, two-wire (I^2C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

There are a number of conditions that could potentially result in nonstandard operation. The details of these conditions depend greatly on the serial protocol used.

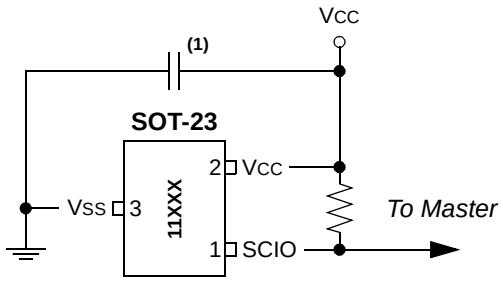
This application note provides assistance and guidance with the use of Microchip UNI/O bus-compatible serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design.

The following topics are discussed:

- Power Supply
- Checking for Acknowledge
- Write Protection Features
- Write-In-Process (WIP) Polling
- Increasing Data Throughput
- Bus Pull-Up Resistor
- Device Address Polling

Figure 1 shows the suggested connections for using Microchip UNI/O bus-compatible serial EEPROMs. The basis for these connections will be explained in the sections that follow.

FIGURE 1: RECOMMENDED CONNECTIONS FOR 11XXX SERIAL EEPROM



Note 1: A decoupling capacitor (typically 0.1 μF) should be used on VCC.

POWER SUPPLY

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on VCC.

Power-Up

On power-up, VCC should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset (POR). VCC should not linger at an ambiguous level (i.e., below the minimum operating voltage).

As further protection during power-up, once VCC has reached its normal operating level, Microchip UNI/O bus-compatible serial EEPROMs will remain in POR until a low-to-high transition is detected on SCIO. This transition must precede the standby pulse that is required before any communication can begin.

Brown-Out Conditions

For added protection, Microchip serial EEPROMs feature a Brown-out Reset circuit. However, if VCC happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that VCC be brought down fully to 0V before returning to normal operating level. This will help ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing VCC down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

Power Failure During a Write Cycle

During a write cycle, VCC must remain above the minimum operating voltage for the entire duration of the cycle (typically 5-10 ms max. for most devices). If VCC falls below this minimum voltage at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

CHECKING FOR ACKNOWLEDGE

One of the benefits of the UNI/O bus protocol is the Acknowledge sequence performed after every byte transmitted on the bus. This sequence allows both the master and slave to detect each byte whether or not the other device is still synchronized. With the exception of the start header, slave devices will always transmit a Slave Acknowledgment (SAK) after every byte if no error has occurred. This means that if the master ever detects a NoSAK, then an error has occurred. In this situation, the master is required to perform a standby pulse before initiating a new command.

A NoSAK will occur for the following events:

- Following the start header
- Following the device address, if no slave on the bus matches the transmitted address
- Following the command byte, if the command is invalid, including read, Current Address Read (CRRD), write, Write Status Register (WRSR), Set All (SETAL) and Erase All (ERAL) during a write cycle
- If the slave becomes out of sync. with the master
- If a command is terminated prematurely by using a No Master Acknowledgment (NoMAK), with the exception of immediately after the device address

WRITE PROTECTION FEATURES

To help avoid unintended writes, Microchip UNI/O bus-compatible serial EEPROMs feature a number of write protection options.

Write Enable and Disable

Microchip UNI/O bus serial EEPROMs feature a Write Enable Latch (WEL) as bit 1 of the STATUS register. This latch is used to allow write operations to occur to the array or the STATUS register. When set to a '1', writes are enabled. When set to a '0', writes are blocked. The WEL can only be set by issuing a valid Write Enable (WREN) instruction, but can be reset upon a number of conditions:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- SETAL instruction successfully executed
- ERAL instruction successfully executed

Note that for the WRITE, SETAL, ERAL, WRSR, and WRDI instructions, the WEL is only reset if the instruction is executed successfully. This means that if, for some reason, the instruction is not valid, the WEL will not be reset. For example, if a write is attempted in an area of the array protected by the Block Protect (BP) bits, then the instruction will not succeed, and the WEL will remain set.

For WRITE, WRSR, SETAL, and ERAL instructions, the WEL is cleared at the end of the write cycle.

It is highly recommended that the WEL only be set immediately before initiating an array or STATUS register write operation in order to minimize the chance of an undesired write operation.

Block Protection

The block protection feature on UNI/O bus-compatible serial EEPROMs allows selective blocks of the array to be protected from write operations. Block protection is controlled through the BP0 and BP1 bits (bits 3 and 4, respectively) in the STATUS register. This offers four different options for protection, as shown in Table 1.

It is recommended that this feature be used in order to protect crucial data in the array.

TABLE 1: ARRAY PROTECTION

BP1	BP0	Address Ranges Write-Protected	Address Ranges Unprotected
0	0	None	All
0	1	Upper 1/4	Lower 3/4
1	0	Upper 1/2	Lower 1/2
1	1	All	None

WIP POLLING

Write operations on serial EEPROMs require that a write cycle time be observed after initiating the write, allowing the device time to store the data. During this time, normal device operation is disabled, and any attempts by the master to access the memory array on the device will be ignored. Therefore, it is important that the master wait for the write cycle to end before attempting to access the EEPROM again.

Each device has a specified worst-case write cycle time, typically listed as TWC. A simple method for ensuring that the write cycle time is observed is to perform a delay for the amount of time specified before accessing the EEPROM again. However, it is not uncommon for a device to complete a write cycle in less than the maximum specified time. As such, using the previously shown delay method results in a period of time in which the EEPROM has finished writing, but the master is still waiting.

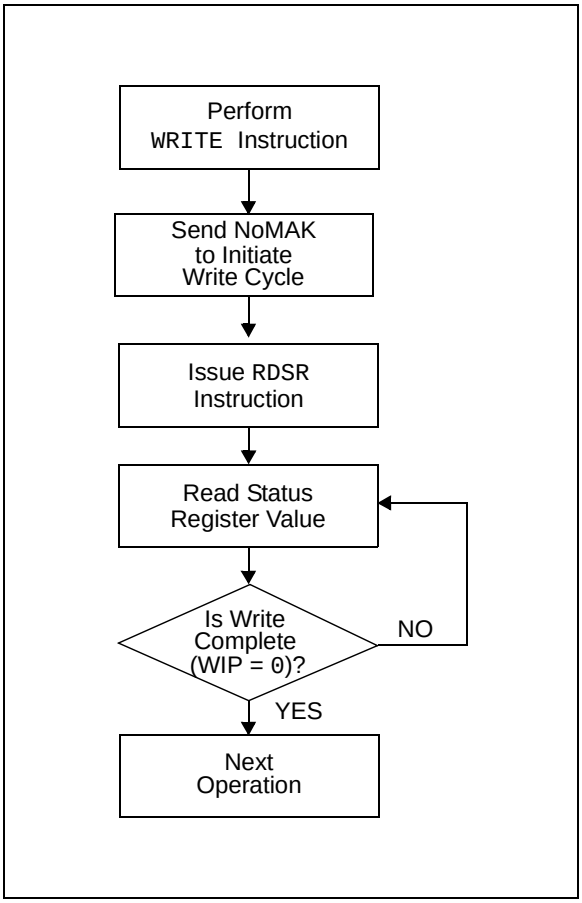
In order to eliminate this extra period of time, and therefore operate more efficiently, it is highly recommended to take advantage of the WIP polling feature.

During both an array write and a STATUS register write, the STATUS register in Microchip's UNI/O bus-compatible serial EEPROMs can still be read. This allows the user to check the state of the WIP bit. This is a read-only bit, set only while a write operation is in progress. Once the operation completes, the WIP (and the WEL) are cleared. Therefore, the STATUS register can continue to be read in order to monitor the value of the WIP bit to determine when the write cycle completes.

WIP Polling Procedure

Once the NoMAK and SAK bits have been transmitted at the end of a WRITE, WRSR, SETAL, or ERAL instruction, the device initiates the internally timed write cycle, and WIP polling can begin immediately. This involves performing a Read Status Register (RDSR) instruction and checking the value read for the WIP bit. If it is high, the device is still writing, and the master should send a MAK bit to request the STATUS register value again. If the WIP bit is low, the write cycle is complete, and the master can terminate the command with a NoMAK and proceed with the next instruction. See Figure 2 for details.

FIGURE 2: WIP POLLING FLOW



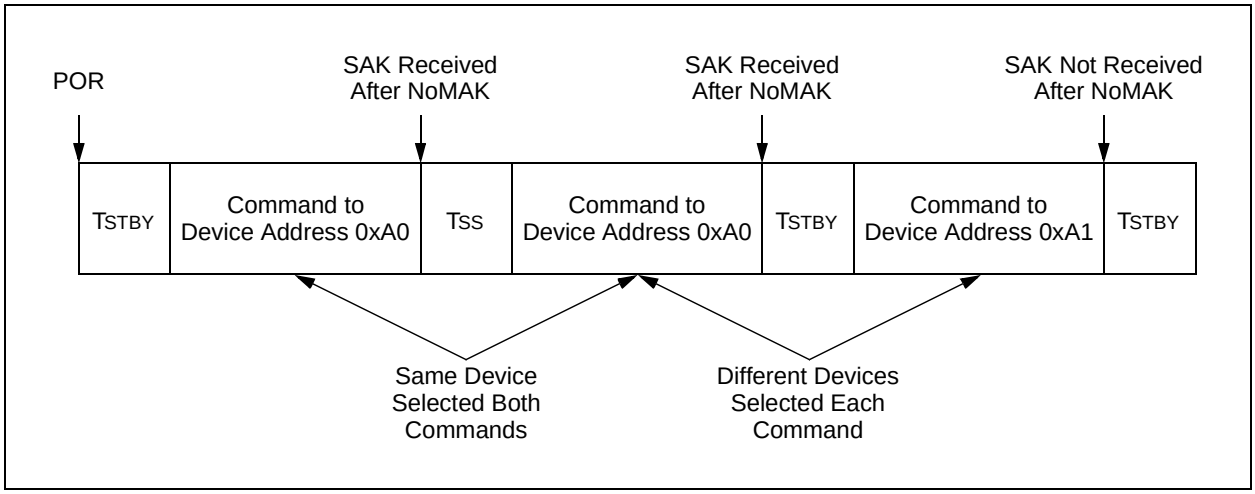
INCREASING DATA THROUGHPUT

Standby Pulse vs. Start Header Setup Time

Before initiating communication to a device not previously selected, a standby pulse (TSTBY) must be observed before beginning the start header. Once a command to a device has been completed successfully, as indicated by the combination of a NoMAK and SAK, the standby pulse is not required to begin a new command to that device. Instead, only the start header Setup Time (TSS) must be observed. If, however, an error occurs and a SAK is not received, or if a device with a different device address is being selected, a standby pulse must be generated.

Refer to Figure 3 for examples of when to use TSTBY and when to use TSS.

FIGURE 3: STANDBY PULSE AND START HEADER SETUP TIME USAGE



Set All and Erase All

When it is desired to set the entire EEPROM array to either 0xFF or 0x00, the simplest and fastest way is to use the SETAL or ERAL instructions. Both of these instructions require an extended write cycle (10 ms vs. 5 ms for a standard write), but are still considerably faster than performing the operation using byte or page writes.

Note that the entire array must be unprotected for writing by clearing both BP1 and BP0 and setting the WEL in order for either instruction to execute.

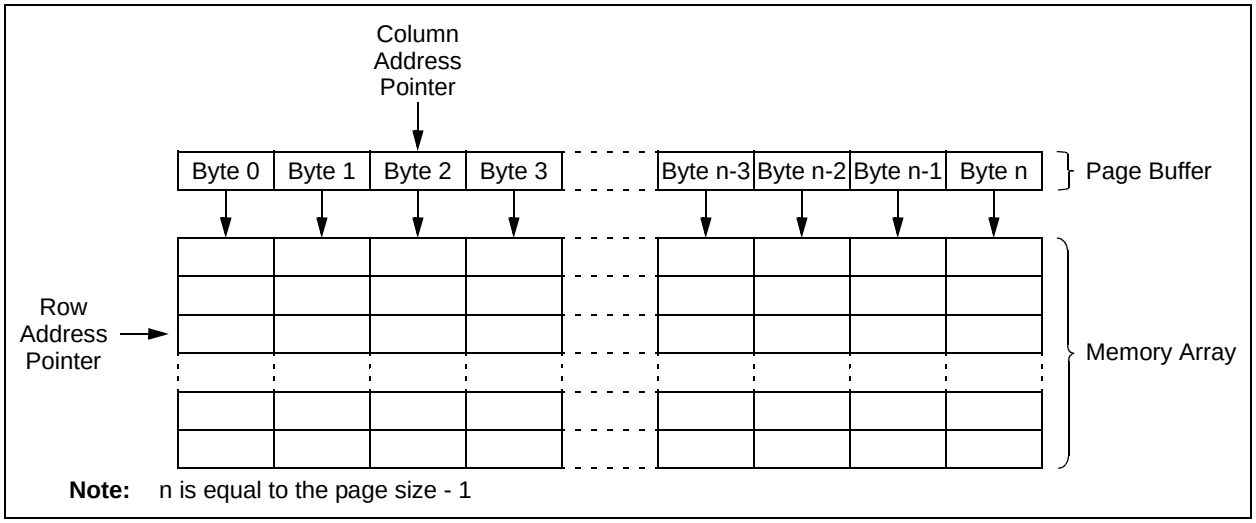
Page Writes

All Microchip UNI/O bus-compatible serial EEPROMs feature a page buffer for use during write operations. This allows the user to write any number of bytes from one to the maximum page size in a single operation. This can provide for a significant decrease in the total write time when writing a large number of bytes.

Page write operations are limited to writing within a single physical page, regardless of the number of bytes actually being written. This is because the memory array is physically stored as a two-dimensional array, as shown in Figure 4. When the word address is given at the beginning of a write operation, both the row and column Address Pointers are set. The row Address Pointer selects which row, or page, is accessed, whereas the column Address Pointer selects which byte from the chosen page is accessed first. Upon transmission of each data byte, the column Address Pointer is automatically incremented. However, during a write operation the page Address Pointer is not incremented, which means that attempting to cross a page boundary during a page write operation will result in the data being looped back to the beginning of the page.

Note that physical page boundaries start at addresses that are multiples of the page size. For example, the 11XX160 features a 16-byte page size, which means that physical pages on the device begin at addresses 0x0000, 0x0010, 0x0020 and so on.

FIGURE 4: PAGE BUFFER BLOCK DIAGRAM



Page Write Procedure

After enabling write operations by issuing a WREN command, the beginning of the WRITE instruction command, word address, and the first data byte are transmitted to the device in the same way as in a byte write operation. But instead of sending a NoMAK to end the operation, the master sends a MAK and continues transmitting additional data bytes, which are temporarily stored in the on-chip page buffer, up to the maximum page size of the device (with care being taken not to wrap around the page). As with the byte write operation, once the master sends a NoMAK, an internal write cycle will begin during which all bytes stored in the page buffer will be written.

Write Time Comparisons

In order to accurately calculate the full period of time required to write a particular amount of data to a device, two things must be considered:

- **Load time** is the amount of time needed to complete all bus operations. This includes issuing the necessary WREN instruction, as well as transmitting the start header, device address, WRITE instruction, word address, and data bytes. This amount of time is dependent on the bus clock speed and the number of data bytes to be written. The TSS time period is used before both WREN and WRITE instructions in place of the standby pulse.
- **Write cycle time** is the time during which the device is executing its internal write cycle. As described in the previous section (**"WIP Polling"**), there is a specified maximum write cycle time for each device. However, the internal write cycle typically completes in less time than specified. As such, both worst-case (5 ms) and typical (3.2 ms at TAMB = 25°C) calculations are provided in Table 2.

The following equations were used to calculate the values for Table 2:

EQUATION 1: WRITE TIME EQUATIONS

$$T_{LOAD} = \frac{10 \cdot (8 + \#\ \text{data bytes})}{F_{CLK}} + (2 \cdot (T_{SS} + T_{HDR}))$$

$$T_{TOTAL} = (T_{LOAD} + T_{WC}) \cdot \#\ \text{write operations}$$

TABLE 2: WRITE TIME COMPARISONS

Device	Page Size (bytes)	# of Bytes to Write	Write Mode(1)	Clock Speed (kHz)	Load Time Per Operation (ms)	Total Time (ms) Worst-Case(2)	Total Time (ms) Typical(3)
11LC010	16	1	Byte	10	9.03	14.03	12.23
		16	Byte	10	9.03	224.48	195.68
		16	Page	10	24.03	29.03	27.23
		1	Byte	100	0.93	5.93	4.13
		16	Byte	100	0.93	94.88	66.08
		16	Page	100	2.43	7.43	5.63

Note 1: Byte Write mode signifies that only 1 byte is written during a single write operation. Page Write mode signifies that a full page is written during a single write operation.

2: Worst-case calculations assume a 5 ms timed delay is used.

3: Typical calculations assume WIP polling is used, with typical T_{WC} = 3.2 ms, T_{AMB} = 25 °C.

From these examples, it is clear that both page writes and WIP polling can provide significant time savings. Writing 16 bytes to the 11LC160 via byte writes at 100 kHz requires roughly 95 ms worst-case. Switching to WIP polling brings that down to roughly 66 ms (assuming typical conditions), nearly a 31% decrease. Changing to page writes further lowers the time to 5.63 ms, an additional decrease of over 91%. Overall, the two techniques provide a combined time savings of over 89 ms, increasing the total data throughput nearly 17 times over.

BUS PULL-UP RESISTOR

In order to ensure bus idle during times when no device is driving the bus, a pull-up resistor is recommended on the SCIO bus. However, two limiting factors must be considered when selecting pull-up resistor (R_P) values:

- Supply voltage (V_{CC})
- Total High-Level Input Current (I_{IH})

Note that the pull-up resistor is meant only to provide a DC level during times when no device is driving the bus, and so slow slew rates due to a large bus capacitance should not adversely affect system performance.

Supply Voltage (V_{CC})

Supply voltage limits the minimum R_P value due to maximum low-level output voltage (V_{OL}) specifications. Consequently, for a given V_{CC} level, a smaller pull-up resistor value will result in a higher low-level output voltage. For Microchip UNI/O bus-compatible devices, the V_{OL} specification is a maximum of 0.4V at 300 µA for Vcc = 5.5V (200 µA for V_{CC} = 2.5V). In other words, if there is a voltage drop across R_P of V_{CC} - 0.4V, it cannot be sourcing more than 200 µA to 300 µA, depending on V_{CC}. Applying Ohm's Law yields Equation 2 for $V_{CC} > 2.5V$, and Equation 3 for $V_{CC} \leq 2.5V$.

EQUATION 2: MINIMUM R_P VALUE $V_{CC} > 2.5V$

$$R_{PMIN} = \frac{V_{CC} - V_{OL}}{I_{OL}} = \frac{V_{CC} - 0.4V}{300\ \mu A}$$

EQUATION 3: MINIMUM R_P VALUE $V_{CC} \leq 2.5V$

$$R_{PMIN} = \frac{V_{CC} - V_{OL}}{I_{OL}} = \frac{V_{CC} - 0.4V}{200\ \mu A}$$

Total High-Level Input Current (I_{IH})

The total high-level input current for a line is the total amount of current that will be flowing through the pull-up resistor when there are no contentions and the line is allowed to be pulled up by the resistor. This current consists of the sum of the input leakage currents for all devices connected to the bus, as well as any other current being sunk by the devices through the input pin.

Because some current will exist through the pull-up resistor even when no device is actively driving the bus, the effective voltage seen at the SCIO pin will be lower than V_{CC} due to the voltage drop across the resistor. This voltage drop must be small enough that the voltage at the pin will still be considered a high by the device. That is, the voltage at the pin must be higher than V_{IH}. Applying Ohm's Law once again results in Equation 4.

EQUATION 4: MAX. R_P DUE TO CURRENT

$$R_{PMAX} = \frac{V_{CC} - (V_{IH})}{I_{IH}}$$

Example Resistor Value Calculation

Here is an example of how to use the previous equations to select the appropriate pull-up resistor value. The following parameters will be used:

TABLE 3: EXAMPLE PARAMETERS

Parameter	Value	Units
V_{CC}	5.0	V
V_{IH}	3.5[1]	V
I_{IH}	10[2]	µA

Note 1: V_{IH} derived from 0.7*V_{CC} spec.

2: I_{IH} used as an example. Each system will vary based on the devices connected to the bus.

By applying Equation 2 and Equation 3, the following resistor value limits were calculated:

TABLE 4: RESISTOR VALUE LIMITS

Limit	Value	Limiting Factor
R_{PMIN}	15.33 kΩ	Supply Voltage
R_{PMAX}	150 kΩ	Input Current

Although a 15.33 kΩ resistor would be weak enough at the specified V_{CC} level to ensure the output reaches V_{OL}, choosing the smallest possible value would be a waste of power. Selecting the largest possible value, 150 kΩ in this example, leaves only the 0.05*V_{CC} margin (specified by V_{HYS}) for any noise that may occur. Therefore, a resistor value between the minimum and maximum should be selected based on power consumption requirements and noise expectations.

DEVICE ADDRESS POLLING

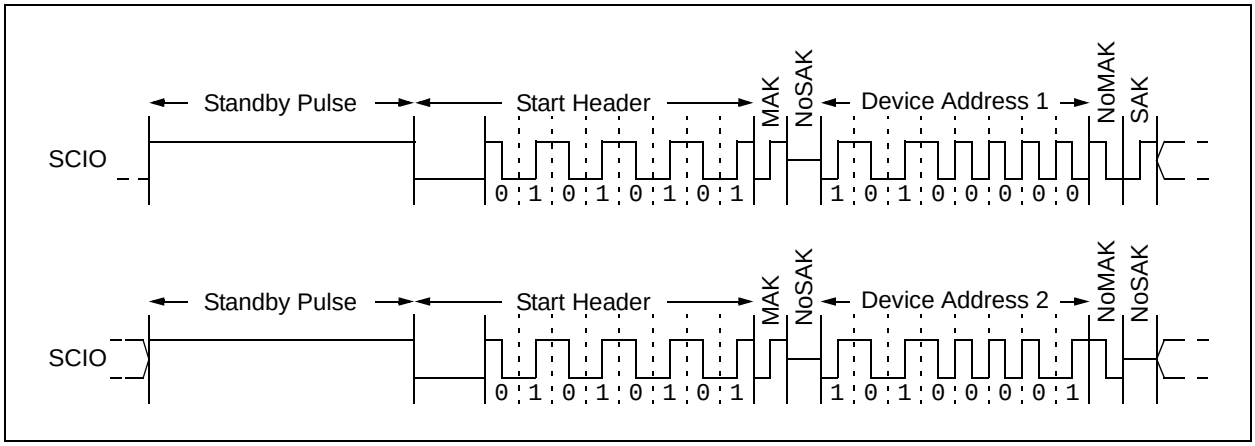
UNI/O bus devices will respond with a SAK if either a MAK or NoMAK is received following the device address, as long as the address is valid. In the case of a NoMAK, the slave device will return to Standby mode immediately following the transmission of the SAK.

This feature allows the master to perform an Address Polling sequence in order to determine what devices are connected to the bus. Such a sequence is typically used in conjunction with a list of expected device addresses to allow for added flexibility in system design.

In order to perform device address polling, the master generates a standby pulse and start header and transmits the desired device address followed by a NoMAK. The master then checks to see whether or not a corresponding slave transmits a SAK. If a SAK is received, then a slave exists with the specified device address. Note that a standby pulse must be generated before every command, because a different device is being addressed during each sequence.

Figure 5 shows an example of polling for two devices. In this example, the first device exists on the bus, and the second device does not exist.

FIGURE 5: DEVICE ADDRESS POLLING EXAMPLE



SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip UNI/O bus-compatible serial EEPROMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its serial EEPROMs and will allow the devices to operate within the data sheet parameters. It is suggested that the concepts detailed in this application note be incorporated into any system that utilizes a UNI/O bus-compatible serial EEPROM.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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