AN 18.16

PCB Design Guidelines for USB224x/i & USB225x/i Controllers

1 Introduction

This application note provides information on general printed circuit board (PCB) layout considerations for the USB224x/i and USB225x/i products.

1.1 References

- Datasheets
  - USB224x/i and USB225x/i products
  http://www.smsc.com/main/catalog/usbprods.html
- Application Notes
  - AN18.15, PCB Design Guidelines for QFN and DQFN packages
  - AN 9.18, SMSC USB 2.0 Analog Routing Guidelines
  http://www.smsc.com/main/cpappnotes.html

1.2 Audience

This application note is written for readers that are familiar with PCB design, including signal integrity and thermal management implementation concepts.

1.3 Objective

The goal of this document is to provide implementation information that is specific to designing PCBs using SMSC's USB224x/i and USB225x/i products.

1.4 Overview

Successful operation of the USB224x/i and USB225x/i Ultra Fast USB 2.0 Flash Media Controllers require special considerations for printed circuit board layout. This application note describes important items to consider for PCB layout. SMSC suggests that all implementations are confirmed through your PCB fabricator and your PCBA assembler.

2 PCB Layout Guidelines

The guidelines presented are applicable to SMSC's USB224x/i and USB225x/i Ultra Fast USB 2.0 Flash Media Controllers and supersede earlier notes.

The following recommendations are suggestions based on SMSC's experience and knowledge and may be accepted or rejected. SMSC does not guarantee any design. Each company is responsible for determining the suitability of its own design.

2.1 Ground Distribution

This family of controllers exercises the target media at very high speeds. The USB interface is also high speed. This environment requires that the ground return path from connectors and sockets to the media controller need to be substantial and contiguous.

2.1.1 Return Path

A return path must exist for each signal flowing between the device and its destinations. A solid ground plane on the layer just below the device is preferred. All ground floods should connect together. Careful consideration should be given to the integrity of the return path for each connection.

2.1.2 Reduce Inductance

All ground connections from the media controller in QFP packaging should be applied with very low inductance to the ground plane (For example, trace width => pad width and short).

2.1.3 “Flag” is the ONLY Ground

All ground connections from the media controller in QFN packaging are done through the “flag”. QFN packages generally have a row (QFN) or two (DQFN) of perimeter pads (“pads”) around a larger central pad (“flag” or “Epad”) encapsulated in a plastic body.

The flag use is two-fold:

- as the primary thermal conduction path to remove package heat,
- and for the device’s only ground.

To address these issues, the following constraints are imposed for the use of these packages:

Use as many vias as can practically fit within the flag. For example, this number should be at least eight vias for 36-pin devices and at least 16 vias for 6 mm x 6 mm flags. Use vias with a finished hole size (FHS) of 0.28 mm to 0.5 mm for best results. “Flood over” these vias rather than using isothermal pads to improve their thermal conductivity and to prevent ground plane isolation issues.

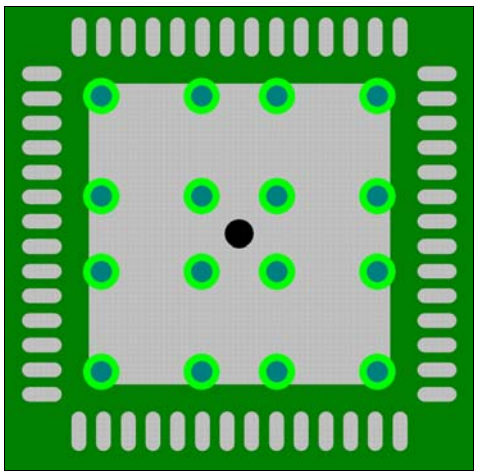

Figure 2.1 Effective Via Placement

a. The more vias that are used, the better the thermal conduction to the internal ground planes (if any exist) as well as to thermal radiation and conduction floods or features on the opposite side of the PCB.

b. The more vias placed within the flag and near its edges, the shorter the loop area to the internal device circuitry. This design method will reduce the signal return lengths. See AN 18.15 for further details (http://www.smsc.com/main/cpappnotes.html).

c. Avoid routing between the flag and the pads of a QFN device.

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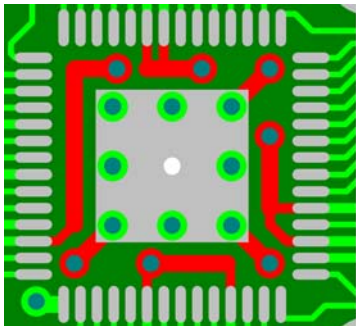

Figure 2.2 Routing Between the Flag and Pins Increases Shorting Risk - AVOID

Routing and vias between the flag and the pads can easily be shorted to either the flag or to the pads because of the physical dynamics of the solder under the device. Shorts can occur to traces and, especially, vias even if they are covered by soldermask. This condition occurs because the trace edges (crowns), via pad edges, and especially via hole edges can be exposed particularly after thermal cycling during soldering processes.

Though via tenting (capping) and via plugging can reduce the occurrences of these effects, it is less expensive and more certain to avoid putting traces or vias under the device in the first place.

2.2 Power Distribution

The USB224x/i and USB225x/i family of devices are supplied by a single +3.3 V supply. However, they use multiple power rails internally. Generally, it is easy to support these devices at PCB layout because of this device family's carefully designed power/ground pinout.

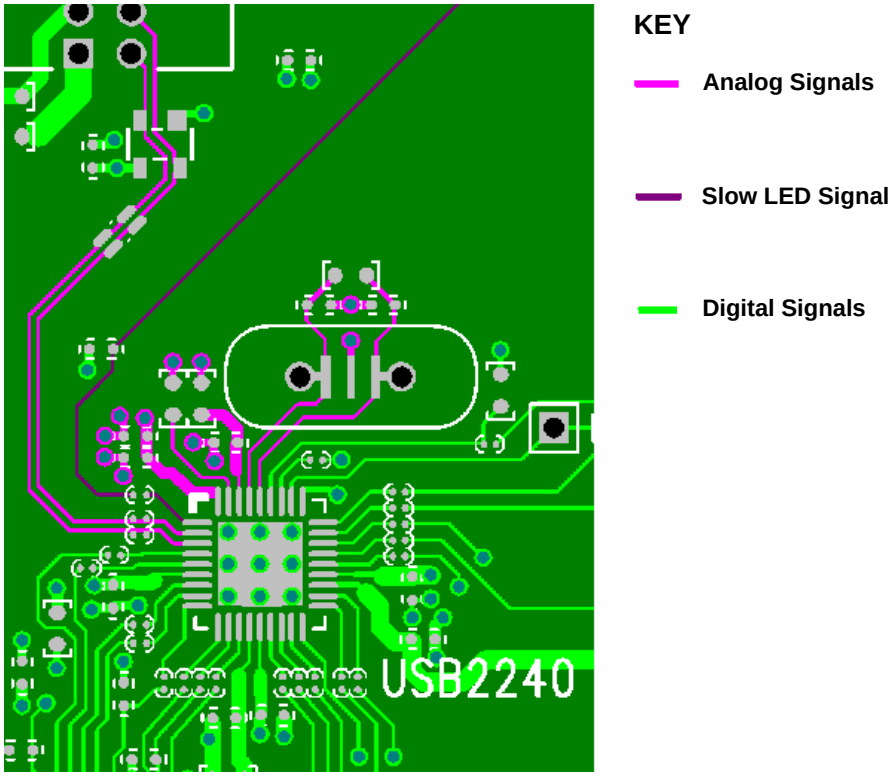

Figure 2.3 Illustrated Signal Types

2.2.1 Isolate Digital and Analog Power Paths

Currents flowing through the digital VDD circuits should not flow through the analog VDDA circuits. To achieve this condition, apply power/ground “moating”, circuit and ground isolation, or other relevant techniques as needed. The analog circuits are the crystal circuit, the RBIAS circuit, the USB I/F circuits, and the VDD18 circuits.

2.3 Bypass Capacitors

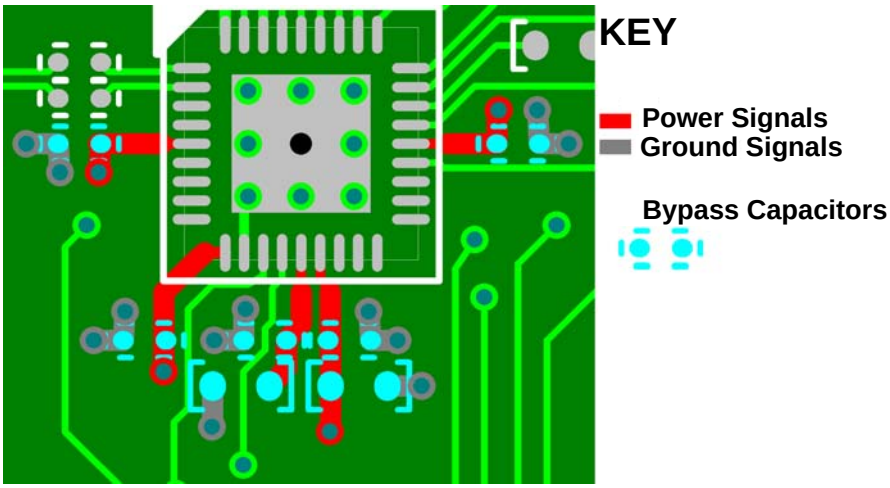

Figure 2.4 Example of Effective Bypass Routing

2.3.1 Bypass Connections

- Ideally, all of the capacitors used for bypass should be connected so that the power signal originates at the rail source, then connects to the capacitor, and finally to the media controller pin. The less the bypass routing conforms to this ideal, the less effective it will be.
- The connections between the device and the capacitors should have low inductance (ex., short and wide connections). The ground connections to these capacitors should be very low inductance. Consider using double vias for the plane connections to divide the effect of the via’s impedances.
- The 4.7 µF – 10 µF ceramic, low-ESR capacitors on VDD33 are used by the internal 1.8 V regulators and should be placed near the VDD33 pins nearest to the VDD18 pins.
- The capacitors on the VDD18 rails are used by the internal regulators and should be connected with very low inductance routing.
- Capacitors of 0.1 µF and lower value on VDD33 are digital decoupling capacitors.

2.4 CRD_PWR

Power to the media devices is provided through the media controller through internal FETs, saving cost and real estate on the PCB. These power rails need capacitors to store large enough charges to support the media that is attached to the interfaces. They also need normal bypass capacitors. The traces need to be wide enough to supply current to the attached media without significant voltage drop.

2.5 Analog Signal Considerations

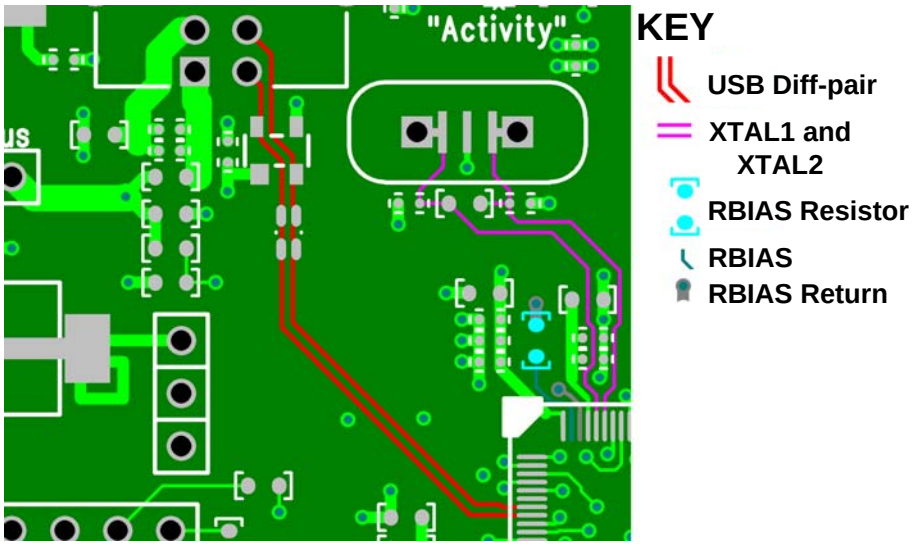

Figure 2.5 Typical Analog Signal Routing

2.5.1 RBIAS Resistor

The USB224x/i and USB225x/i products use an external resistor to set a bias current for internal circuitry like many other SMSC devices. This resistor is a very sensitive analog input.

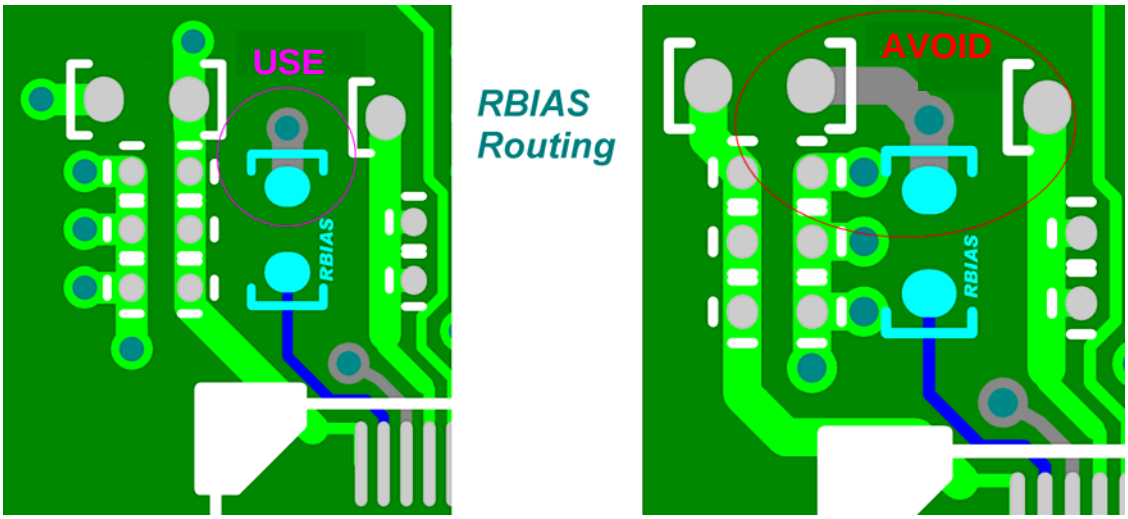

Figure 2.6 Effective vs. Defective RBIAS Resistor Routing

2.5.1.1 RBIAS Signal Routing

The resistor should be connected with a short trace to the RBIAS pin of the device to reduce signal coupling from other circuits.

2.5.1.2 RBIAS Return Routing

The return ground on the RBIAS resistor should flow directly to the VSS pin nearest to the RBIAS pin on the media controller. The ground via on the RBIAS resistor should NOT be shared with any other devices, especially bypass capacitors. On QFN packages, the return ground should connect with a low inductance connection to ground that is not shared with other circuits.

2.5.2 USB Signal Routing

The USB lines are constrained by the USB 2.0 specification. Critical conditions for the lines are detailed in this document:

2.5.2.1 Differential Impedance

The USB traces must be routed with a Zdiff of 90 Ω +/-10 Ω. Experimental data shows that traces with a Zdiff on the higher end of that range (94 Ω -100 Ω) accommodate a wider range of system issues than traces with lower Zdiff values.

2.5.2.2 Differential Routing

The USB traces must be routed as differential pairs. They must not be exposed to cross-talk from adjacent lines. Maintain a routing spacing (gap) of at least three to five times the differential spacing between USB signals and signals outside of the USB pair.

Example: If the differential spacing is 7 mils, the spacing to signals not in the USB pair will be 21 mils – 35 mils.

2.5.3 Crystal Oscillator

XTAL1 and XTAL2 are the crystal oscillator connection pins.

2.5.3.1 XTAL1 and XTAL2 Routing

The crystal oscillator pins should route directly to the crystal pins and their associated load capacitors and bias resistor. Route foreign traces no closer than five times the minimum trace spacing to these traces.

2.6 Digital Signal Considerations

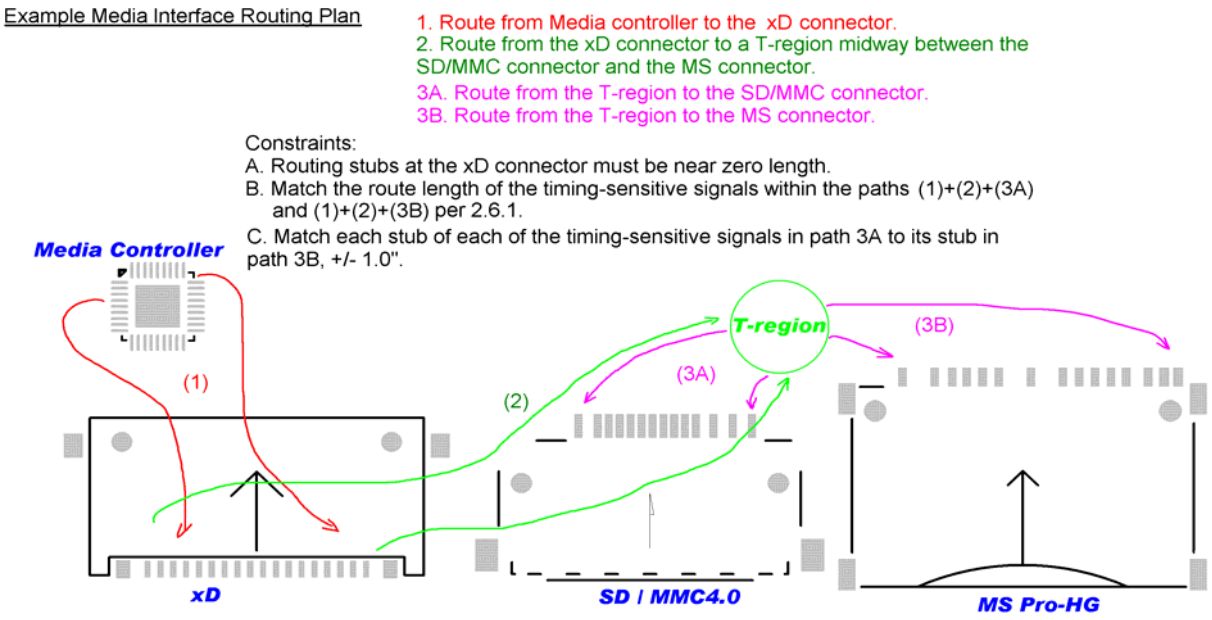

Figure 2.7 Example Routing Plan for the Media Interface Signals

2.6.1 Media Signal Trace Lengths

Signal Timing to Hi-Speed media can be critical. Route all timing-sensitive media signals so that they are the same length, +/- 0.5 inches.

2.6.2 SD_CLK

Route all other traces, including other SD interface signals, no closer than three times the minimum trace spacing to these traces. Five times the minimum spacing is even more effective.

2.6.3 MS_CLK

Route all other traces, including other MS interface signals, no closer than three times the minimum trace spacing to these traces. Five times the minimum spacing is even more effective.

2.6.4 CF_IORDY

Route all other traces, including other CF interface signals, no closer than three times the minimum trace spacing to these traces. Five times the minimum spacing is even more effective.

2.6.5 Routing Multiplexed Signals

The media interface signals on the USB224x/i are multiplexed together. This condition presents an additional challenge to the PCB designer of properly routing this multiplexed signal path. Please refer to Figure 2.7 on page 6.

1. Route the media interface signals from the media controller to the xD socket.
2. Then, route the media interface signals from the xD socket at or near zero length stubs to a T-region near the SD/MMC and MS connectors.
3. Route the stubs from the T-region to the SD/MMC connector.
4. Route the stubs from the T-region to the MS connector.

Notes: Stubs at the xD connector need to be zero or near zero in length. Stubs from the T-region to SD/MMC and MS connectors need to be minimized and balanced so that the lengths are matched per Figure 2.7 on page 6. This method reduces the reflection effects on the signals in Hi-Speed use. The CD signals (SD_nCD and MS_INS) do not require length matching.

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