KSZ8462HLI and KSZ8462FHLI Errata

Device Revision: Production
Document Revision: 0.3

1	Writing to PMCTRL Register Power Management Bits Requires Change to Host Interface Write Timing

Description:
The Write Sample Time bit in the RX Frame Data Pointer Register (0x186 – 0x187) bit [12] determines when write data is sampled on the host interface. When this bit is 1 (default), the sample time is earlier, and writes to the Power Management Mode bits in PMCTRL (0x032 – 0x033) bits [1:0] may not occur properly. For example, it may be impossible to put the device into Global Soft Power Down mode.

Workaround:
Clear the Write Sample Time bit in the RX Frame Data Pointer Register (0x186 – 0x187) bit [12]. This causes the write sample time to occur later, and eliminates the problem described above.

This bit is cleared by the driver.

160

2	Transmit Memory Available Value may Read Incorrect

Description:
The TXQ Memory Information Register (TXMIR) (0x178 – 0x179) is a read-only register that indicates the amount of unused memory space in the transmit queue. Sometimes this register returns an incorrect value of zero. Reading it again will return a correct value.

Workaround:
The software workaround is to read the register a second time whenever a zero value is read.

216

3	PTP Message Forwarding Ignores VLAN Tagging

Description:
VLAN tagging can be used to control and limit the forwarding of frames to particular ports. PTP packets are given highest priority by the switch, and are forwarded without regard for the VLAN membership. This will affect applications implementing the IEEE C37.238 profile for power system applications.

Workaround:
For PTP messages forwarded to the host port (port 3), software can examine the VLAN tag of received PTP messages and drop messages whose VLAN membership does not match that of the host. This filtering is implemented in the Micrel driver.

There is no workaround for the forwarding of PTP messages between ports 1 and 2.

266

4 All Host Generated PTP Messages are Transmitted Through a Closed Port

Description:

In certain applications, such as Spanning Tree Protocol, it may be necessary to close one switch port (by clearing the Transmit Enable and Receive Enable bits in the PnCR2 registers). IEEE 1588 requires the ability to pass peer-to-peer messages (Pdelay_Req, Pdelay_Resp and Pdelay_Resp_Follow_Up) through closed ports. The KSZ8462 allows these peer-to-peer messages to be transmitted by the host processor through the switch to a closed port, but it mistakenly also permits other PTP messages to be transmitted through a closed port.

Workaround:

The Micrel driver screens PTP messages sent by the host. If a non-peer-to-peer PTP message from the host is destined for a closed port, the driver will change the destination port field in the message to block the packet from being transmitted from the closed port.

This works only if the message is destined for both ports 1 and 2. If the message is intended for only the one closed port, then this technique won't work (because the port destination becomes '00' which is "broadcast"), and the driver has no choice but to drop the packet.

298

5 Port 1 Received PAUSE Frames

Description:

Port 1 does not respond to received PAUSE control frames, meaning that it will not suspend transmission of data frames on that port when requested to do so by its link partner sending PAUSE frames. PAUSE frames are received and are counted in the MIB RxPausePkts counter (offset 0xA), but they are not acted upon.

This issue does not affect the generation (transmission) of PAUSE frames by port 1 in response to congestion within the KSZ8462 switch fabric. Also, port 2 does not have this issue; it responds properly to received PAUSE frames.

Workaround:

There is no direct workaround for this issue. However, if port 1 and port 2 have different link partners and/or different traffic patterns, it may be possible to assign ports 1 and 2 with this asymmetry in mind, such that port 1 gets the configuration that is less likely to generate flow control requests into that port.

331

6 Disabling Auto-Negotiation

Description:

Unusual link behavior may occur if the Auto-Negotiation Enable bit (in the PxMBCR or PxCR4 register) is cleared (to disable AN) while link is already established and Energy Efficient Ethernet (EEE) is enabled. Note that EEE is enabled by default, and that auto-negotiation is controlled individually for each port.

The problem does not occur if link is down when AN Enable is cleared, or if link is to a non-EEE device.

Workaround:

To disable auto-negotiation, follow these steps:

1. Disable EEE by clearing the Next Page Enable bit(s) in the PCSEEEC Register (0x0F3): bit [0] and/or bit [1] for the desired port(s).
2. Set the Restart Auto-Negotiation bit(s) in the PxMBCR or PxCR4 registers (0x04C, 0x058, 0x07E, 0x096) for the desired port(s).
3. The Auto-Negotiation Enable bit(s) may now be cleared.

333