# Migrating from AT89C2051/C4051 to AT89S2051/S4051

## New Features

- **8-bit Pulse-width Modulation**
- **Enhanced UART Serial Port with Framing Error Detection and Automatic Address Recognition**
- **On-chip Analog Comparator with Selectable Interrupt**
- **Brown-out Reset**
- **Internal Power-on Reset**
- **Interrupt Recovery from Power-down Mode**
- **Programmable and Fuseable x2 Clock Option**
- **Four-level Enhanced Interrupt Controller**
- **Power-off Flag**
- **Flexible Programming (Byte and Page Mode)**
- **User Serviceable Signature Page (32 Bytes)**

## 1. Introduction

The purpose of this application note is to help users convert existing designs from AT89C2051/C4051 to AT89S2051/S4051. This application note describes AT89S2051/S4051 memory sizes, features, and SFR mapping register differences. More detailed information can be found in the AT89S2051/S4051 datasheet.

## 2. Memory Sizes

| Memory | AT89C2051 | AT89C4051 | AT89S2051 | AT89S4051 |
|---|---|---|---|---|
| Flash | 2K Bytes | 4K Bytes | 2K Bytes | 4K Bytes |
| RAM | 128 Bytes | 128 Bytes | 256 Bytes | 256 Bytes |

## 3. 8-bit Pulse-width Modulation

A generated waveform is output on the Timer 1 input pin. Timer 0 acts as an 8-bit prescaler to select the Pulse-width Modulation base.

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## 4. Enhanced UART Serial Port with Framing Error Detection and Automatic Address Recognition

When used for frame error detection, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON Register. Automatic Address Recognition allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparison.

## 5. On-chip Analog Comparator with Selectable Interrupt

When the positive input AIN0 (P1.0) is greater than the negative input AIN1 (P1.1), the logical output is 1; otherwise, the output is 0. The comparator can be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR in the SFR map. Three debouncing modes are provided to filter out noise caused by slow-moving analog inputs.

## 6. Brown-out Reset

When $V_{CC}$ decreases to a value below the trigger level, the Brown-out Reset is immediately activated. The Brown-out Detection ensures the system will enter reset without the possibility of errors induced by incorrect execution if $V_{CC}$ fails or dips.

When $V_{CC}$ increases above the trigger level, the Brown-out Detector will start the microcontroller after 2 ms. For the AT89C4051, the Brown-out Detector starts the microcontroller after 15 ms.

## 7. Internal Power-on Reset

When $V_{CC}$ reaches the Power-on Reset threshold voltage, an internal reset signal is generated. The Power-on Reset circuit ensures that the device is reset from power-on.

## 8. Interrupt Recovery from Power-down Mode

An enabled external interrupt (through $\overline{INT0}$ or $\overline{INT1}$) can be used to exit from the power-down mode. Two wake-up options are available to exit from power-down mode via interrupt. When bit CLKREG.2 is 0 following a falling edge on the interrupt input pin, the CPU will resume execution after a set period of time. When CLKREG.2 is 1, the wake-up mode is externally controlled by the interrupt pin and the CPU will resume execution after the rising edge of the same pin. In older derivatives, the only way to recover from the Power-down mode is to perform a hardware reset.

## 9. Programmable and Fuseable x2 Clock Option

The x2 clock option allows the microcontroller to execute one machine cycle in 6 clock periods instead of 12 clock periods. This can be set either through hardware or software.

## 10. Four-level Enhanced Interrupt Controller

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority (IP) register and in the Interrupt Priority High (IPH) register.

## 11. Power-off Flag

The Power-off Flag is in the PCON register in the SFR map and is set to “1” during power-up (i.e. cold reset). The Power-off Flag is not affected by External Reset or Brown-out Reset (i.e. warm resets) and can be used to indicate that the microcontroller has been powered down.

## 12. Flexible Programming (Byte and Page Mode)

The program memory can be programmed using the serial ISP interface while RST is strapped to $V_{CC}$. Program memory can be programmed in page mode (1 code page = 32 bytes) or byte mode.

Parallel page mode programming requires that the user load the upper 7 bits of the address before issuing the read/write command. The XTAL1 pin is used to increment the address for page read/write.

## 13. User Serviceable Signature Page (32 Bytes)

Thirty-two bytes are accessible to the user to program their own desired data. Bytes can be programmed by either parallel or serial mode.

## 14. SFR Mapping

The highlighted SFR locations are new registers for the AT89S2051/S4051 devices.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B | | | | | | | | 0F7H |
| 0E8H | | | | | | | | | 0EFH |
| 0E0H | ACC | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW | | | | | | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | | | | | | | 0C7H |
| 0B8H | IP | SADEN | | | | | | | 0BFH |
| 0B0H | P3 | | | | | | | IPH | 0B7H |
| 0A8H | IE | SADDR | | | | | | | 0AFH |
| 0A0H | | | | | | | | | 0A7H |
| 98H | SCON | SBUF | | | | | | | 9FH |
| 90H | P1 | | | | | | | ACSR | 97H |
| 88H | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | | CLKREG | 8FH |
| 80H | | SP | DPL | DPH | | | | PCON | 87H |

## 15. Register Differences

Registers and bits in AT89C2051/C4051 and the AT89S051/S4051 equivalents.

| AT89C2051/C4051 | | AT89S2051/S4051 | |
|---|---|---|---|
| **Register** | | **Register** | |
| IE | EA -- -- ES ET1 EX1 ET0 EX0 | IE | EA EC -- ES ET1 EX1 ET0 EX0 |
| IP | -- -- -- PS PT1 PX1 PT0 PX0 | IP | -- PC -- PS PT1 PX1 PT0 PX0 |
| PCON | SMOD -- -- -- GF1 GF0 PD IDL | PCON | SMOD1 SMOD0 PWDEX POF GF1 GF0 PD IDL |
| SCON | SM0 SM1 SM2 REN TB8 RB8 TI RI | SCON | SM0/FE SM1 SM2 REN TB8 RB8 TI RI |

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