How the Event System Helps to Lower CPU Load and Power Consumption in Cortex™-M0+ Microcontrollers

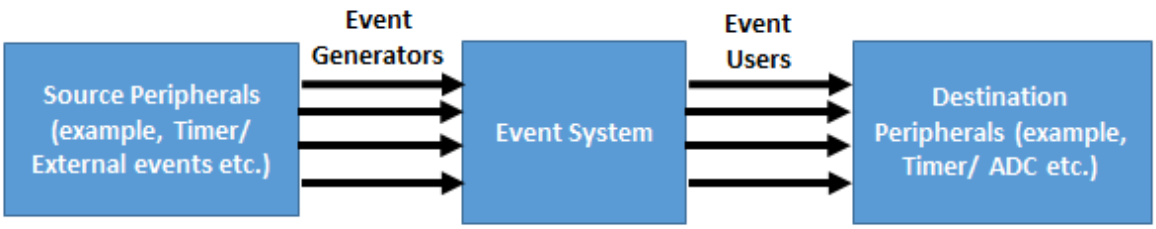
Introduction to the Event System

In Microchip's Cortex™-M0+ Microcontrollers (i.e., SAMDx, SAMLx), the Event System (EVSYS) is a feature for inter-peripheral communications. The EVSYS enables the possibility for a change of state in one peripheral to automatically trigger actions in other peripherals. The peripheral event is configurable in the software. The EVSYS allows for autonomous control of peripherals without any use of CPU bandwidth.

The Event System is comprised of the following two event resources:

- Event Generator: input events of a peripheral that will generate the events signal
- Event Users: connected to peripherals that will receive events as they are generated

Figure 1. Event System General Overview



The supported peripheral can have many event generators and many event users. For additional information, refer to the respective product data sheet.

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1. The Event System Helps in Achieving Deterministic Timing

Different triggers at the peripheral level can result in an event. With the help of the Event System, the event user can react to the event generator within a deterministic timing. The EVSYS timing is based on the event path and configuration of the Generic Clock (GCLK). Depending on the needs of the application, one of the path configurations can be selected.

Table 1-1. Event System Path Configuration

Features	Asynchronous Path	Synchronous Path	Resynchronized Path
Event Path Selection Criteria	Asynchronous connection between the event generator and user. No edge detection/ Interrupts are needed.	When edge detection or interrupts from events. Same GCLK for generator and user.	When edge detection or interrupts from events. Different GCLK for generator and user.
Example Applications	Button press triggers the timer to flash the LED.	AC triggers the TCC to change the duty cycle.	ADC conversion triggers the DMAC to store the data and generate an interrupt.
Event Generator to Event User Latency (max.)	Device dependent. If same GCLK is used for Event Generator and Event User, latency is 0 cycles of Event System GCLK.	1 cycle of Event System GCLK.	3 cycles of Event System GCLK.

After the asynchronous path latency as mentioned in the previous table, there is a delay needed for the user event to synchronize with the destination peripheral. The maximum propagation latency of a user event to the peripheral clock core domain is three peripheral clock cycles. For example, a timer tick triggers a reaction in the ADC in Asynchronous path. This is comprised of independent channels, therefore, the Event System has a fixed latency of two cycles. It will take a predictable timing to trigger an event action, and the EVSYS provides more deterministic timing.

Tips and General Guidelines

1. Not all peripheral events support all event paths. Depending on the product, some event peripherals and events are only supported in a specific path. In this instance, the ADC supports only the Asynchronous path for the SAMD21 microcontroller. Before selecting the event, refer to the User Multiplexer Selection table of the Event Systems section in the product data sheet.
2. The GCLK for the peripherals EVSYS should be correctly configured with respect to the event path, for the correct functioning of the Event System. If the path, clock, or peripheral is not correctly configured, the Event System will not trigger the events (i.e., Synchronous path is chosen, but the event generator and user are configured for different GCLK. In this case, the event triggering will not work correctly).
3. When the processor or peripheral is slow to handle events (i.e., slow ADC conversion), the next event should come only after the previous event is processed (i.e., ADC conversion is complete). To take care of this condition, the CHBUSY, USRRDY and OVR flags of each event channel need to be checked.

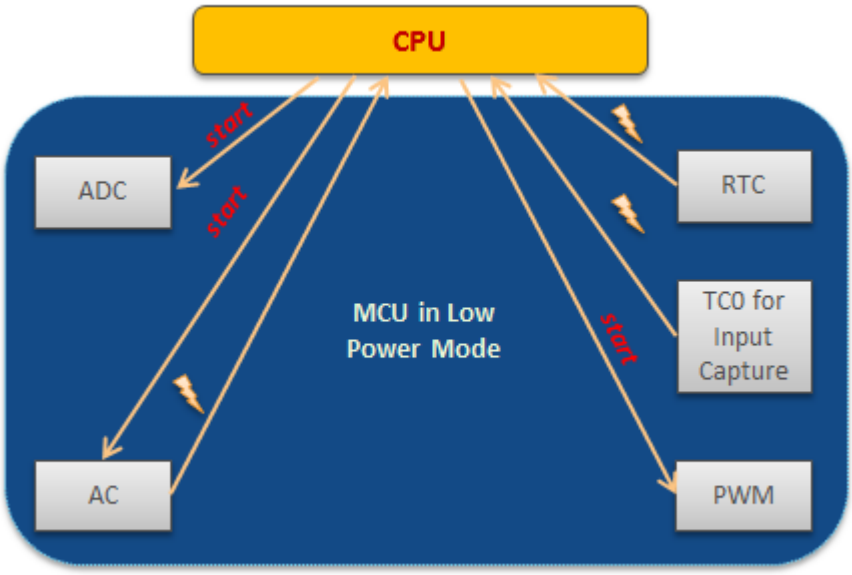
2. The Event System Helps in Reducing CPU Load

The advantages of the EVSYS are discussed in a couple of applications examples. Consider the following first application scenario.

- The microcontroller (MCU) is in Low-Power mode. The Real-Time Clock (RTC) wakes the CPU in a predefined interval
- The CPU starts the Analog-to-Digital Converter (ADC) to convert the data. After the conversion, the MCU goes back to Power-Down mode
- The Timer, TC0, wakes the CPU when any signal is detected using the input capture feature
- The CPU starts the Analog Comparator (AC) to check if the measured signal is within a threshold level
- If the measured signal is outside the threshold level, the TCC generates the PWM signal. Otherwise, the MCU goes back to Power-Down mode

The following figure shows the conditions if the EVSYS is not used; therefore, the operations previously mentioned need to be configured using the interrupts. Whenever an interrupt wakes the CPU, it consumes CPU bandwidth.

Figure 2-1. CPU Loading by Peripherals



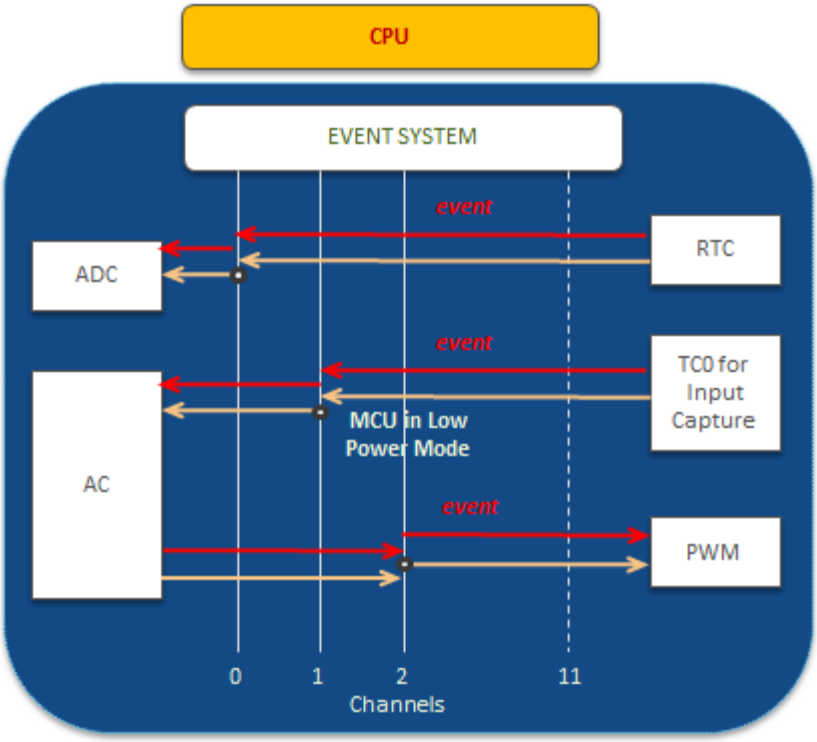
If EVSYS is used, the events can be managed between the peripherals using the EVSYS. This is shown in the following figure.

In this scenario,

- The RTC is the event generator, and the ADC is the event user
- The TC0 capture event is the event generator, and the AC is the event user
- The AC is the event generator, and the PWM is the event user

The use of the EVSYS helps in offloading the CPU bandwidth.

Figure 2-2. Event System Peripherals

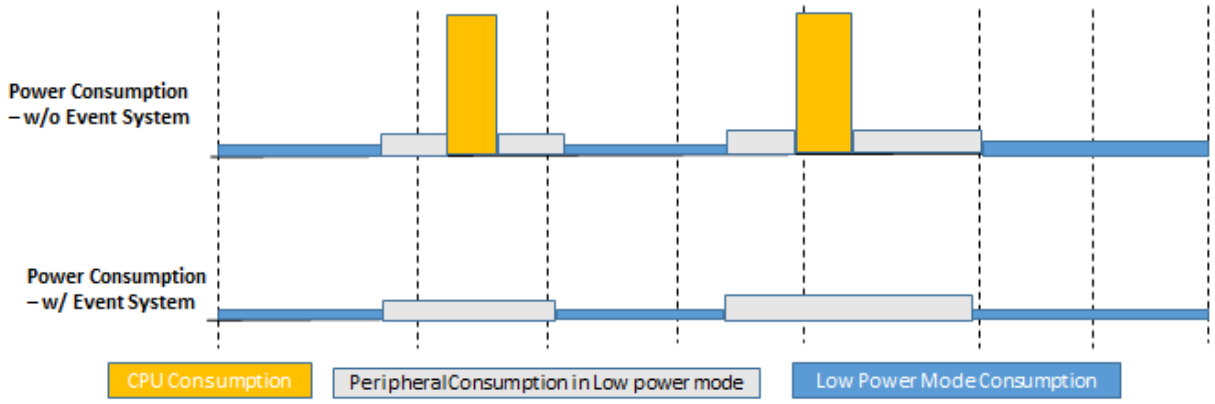


3. The Event System Helps in Lower Power Consumption

The Event System helps lower the overall power consumption of the system. As peripherals coordinate using the EVSYS, the CPU can remain in Sleep mode for longer periods. Typically, CPU consumption is higher than the peripheral consumption. When the MCU wakes up in Active mode, the consumption is higher. For instance, SAM L21 power consumption is 35 µA/MHz in Active mode, and 200 nA in Sleep mode. Using the EVSYS, the CPU is able to remain in Sleep mode for longer periods. The peripherals can continue to operate in Sleep mode, where the source clock is running. With implementation of the EVSYS, the peripherals can communicate between themselves in Sleep mode, without waking up the MCU to Active mode.

The approximate consumption comparison is shown in the following figure for these two application conditions:

Figure 3-1. Power Consumption With and Without the Event System



The EVSYS can be used to wake up the CPU from all sleep modes, even if the clock used by the EVSYS channel and the EVSYS bus clock are disabled. Some event generators can generate an event when their clocks are stopped.

Motor Control Application

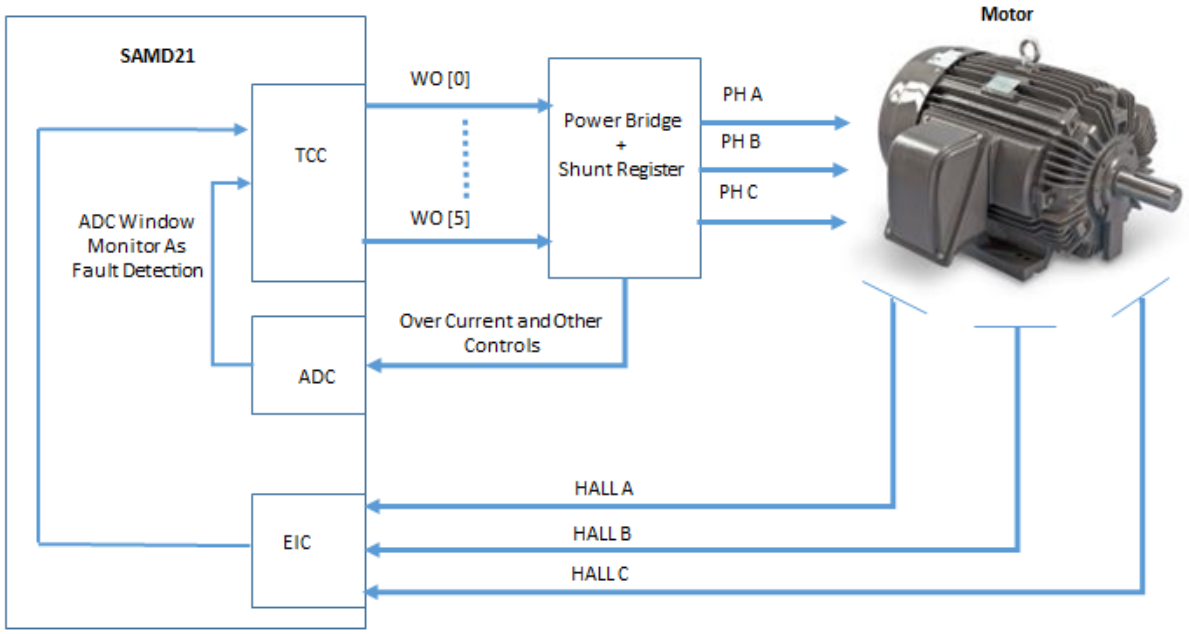
Consider the second example of a motor drive application with a PWM using a Cortex-M0+ MCU. The block diagram below shows the MCU performing multiple operations. The MCU control combines the motor speed or torque using a closed-loop. The ADC is used to measure the current going into the motor. It also detects erroneous situations, and overcurrent sensing using comparator features of the ADC. In an overcurrent situation, the PWM channels driving the motor need to be shutdown as soon as possible to prevent permanent damage to the circuit and for safety reasons.

Without an EVSYS, any fault or overcurrent situation will trigger an interrupt, but the interrupt service request might be delayed by a few cycles due to interrupt latency and priority if the CPU is performing other higher priority tasks. Using the Event System helps to connect the ADC directly to the timer TCC and take the required action (that is, shutdown the timer) within two to six cycles, regardless of what the rest of the MCU is doing.

In a motor control system having a single shunt and using the Field Oriented Control (FOC) algorithm, the timing of the phase current measurement by the ADC within the timer compare cycle is critical. The EVSYS can be used to accurately start the measurement of the phase currents.

Example of Motor Control Application

Figure 3-2. Motor Control Block Diagram



Some examples of application note references related to the EVSYS are provided in the Resources Section.

As shown in the previous examples, the EVSYS provides the following advantages:

- Predictable timing
- Reduced CPU overhead
- Reduced power consumption

4. Other Relevant Resources

- http://www.atmel.com/Images/Atmel-42471-SAM-L21-ADC-Sampling-using-Low-Power-Features_ApplicationNote_AT12705.pdf
- http://www.atmel.com/Images/Atmel-42108-SAM-Events-System-EVENTS-Driver_ApplicationNote_AT03245.pdf
- http://www.atmel.com/Images/Atmel-42267-TC-Capture-on-External-Interrupt-with-the-Event-System-on-SAM-D20_ApplicationNote_AT05567.pdf

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