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USB332x Transceiver Layout Guidelines

INTRODUCTION

Microchip's USB332x comes in a 25 ball Wafer-Level Chip-Scale Package (WLCSP) lead-free RoHS compliant package; (1.95 mm X 1.95 mm, 0.4mm pitch package). This application note provides general PCB layout guidelines for the USB332x family of devices. The Universal Serial Bus (USB) is capable of operating at 480 Mbps. Excellent signal integrity is required to operate reliably at high-speed data rates.The PCB layout is a critical component in maintaining signal integrity.

Audience

This document is written for a reader that is familiar with hardware design, USB protocols and the USB 2.0 specification. The goal of the application note is to provide information on sensitive areas of the PCB layout.

Overview

The following recommendations for PCB layout with Microchip parts is not the only way to layout a PCB for our WLCSP. PWB design engineers will have his/her own preference, and the implementation will be dependent on complexity and density of layout, PCB real estate, number and types of devices in circuit and the environment that the final product will reside in. The examples presented in this application note are taken from the USB332x Customer Reference Board (CRB).

References

The following documents should be referenced when using this application note:

- Microchip USB332x Data Sheet
- Microchip CRB-USB332x User's Guide
- Universal Serial Bus Specification Revision 2.0

GENERAL DESIGN GUIDELINES

This section provides guidelines for the sensitive circuits associated with the system application of the USB332x.

ULPI Bus

The layout of the ULPI interface should be analyzed with the timing requirements of the USB Link controller to ensure that proper timing is met. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Controlled Impedance for USB Traces

The USB 2.0 specification requires the USB DP/DM traces maintain nominally 90 Ohms differential impedance +/- 15 % (see USB specification Rev. 2.0, paragraph 7.1.1.3 for more details). In this design the traces are 6 mil (0.001 inch) wide with line spacing of 7 mils. These numbers are derived for 5 mil distance from ground reference plane. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be recalculated. A continuous reference plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines to maintain symmetry between DP/DM lines in regards to shape and length.

FIGURE 1: EXAMPLE OF ROUTING DP/DM TO TYPE B CONNECTOR

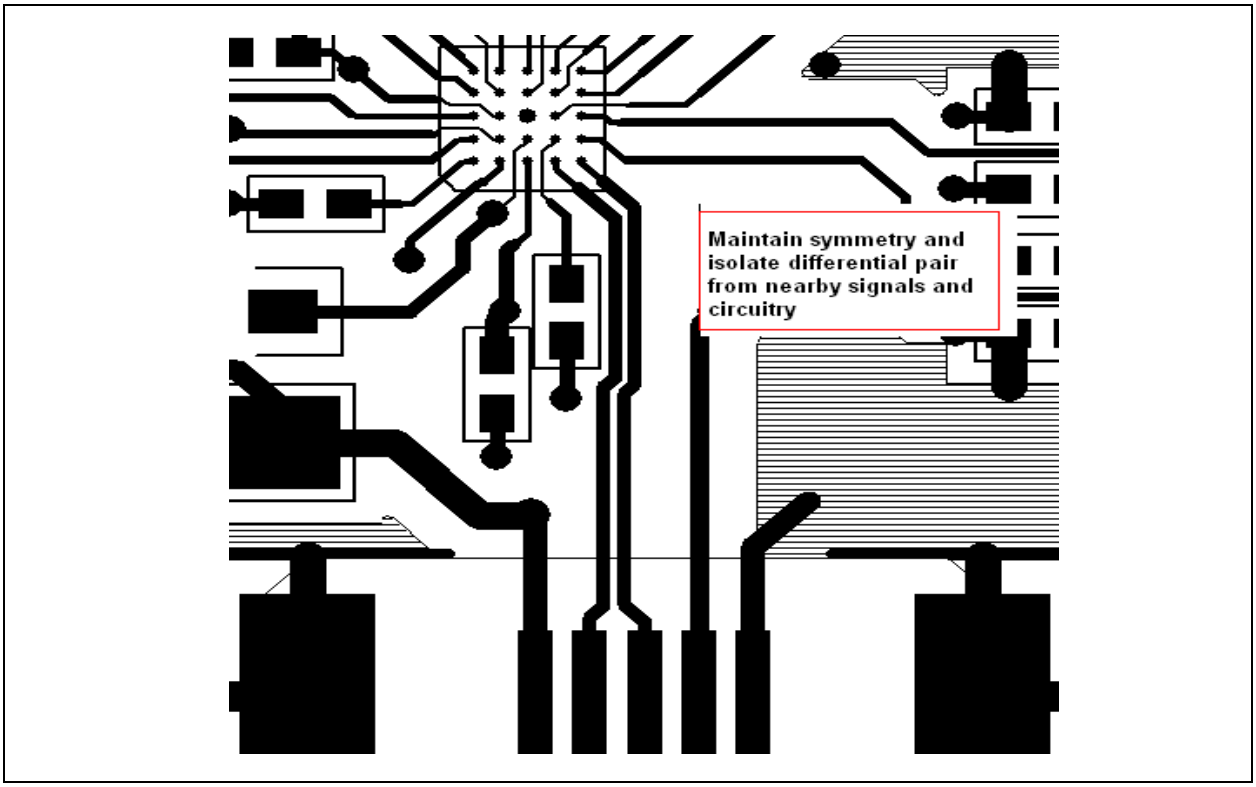


Figure 1 shows DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification.

Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of adjacent signals to lines that is greater than or equal to 5 times the distance of the 7 mil spacing between the traces. Do not route differential pairs under parts. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the reference plane from DP/DM.

USB Switch Pins

The integrated USB Switch may be used to connect sensitive analog signals such as audio or USB Full-Speed/Low-Speed data. For this reason, traces connected to the SPK_R and SPK_L pins should use design practices similar to those described in Controlled Impedance for USB Traces on page 2 and Isolation of DP/DM Traces on page 2.

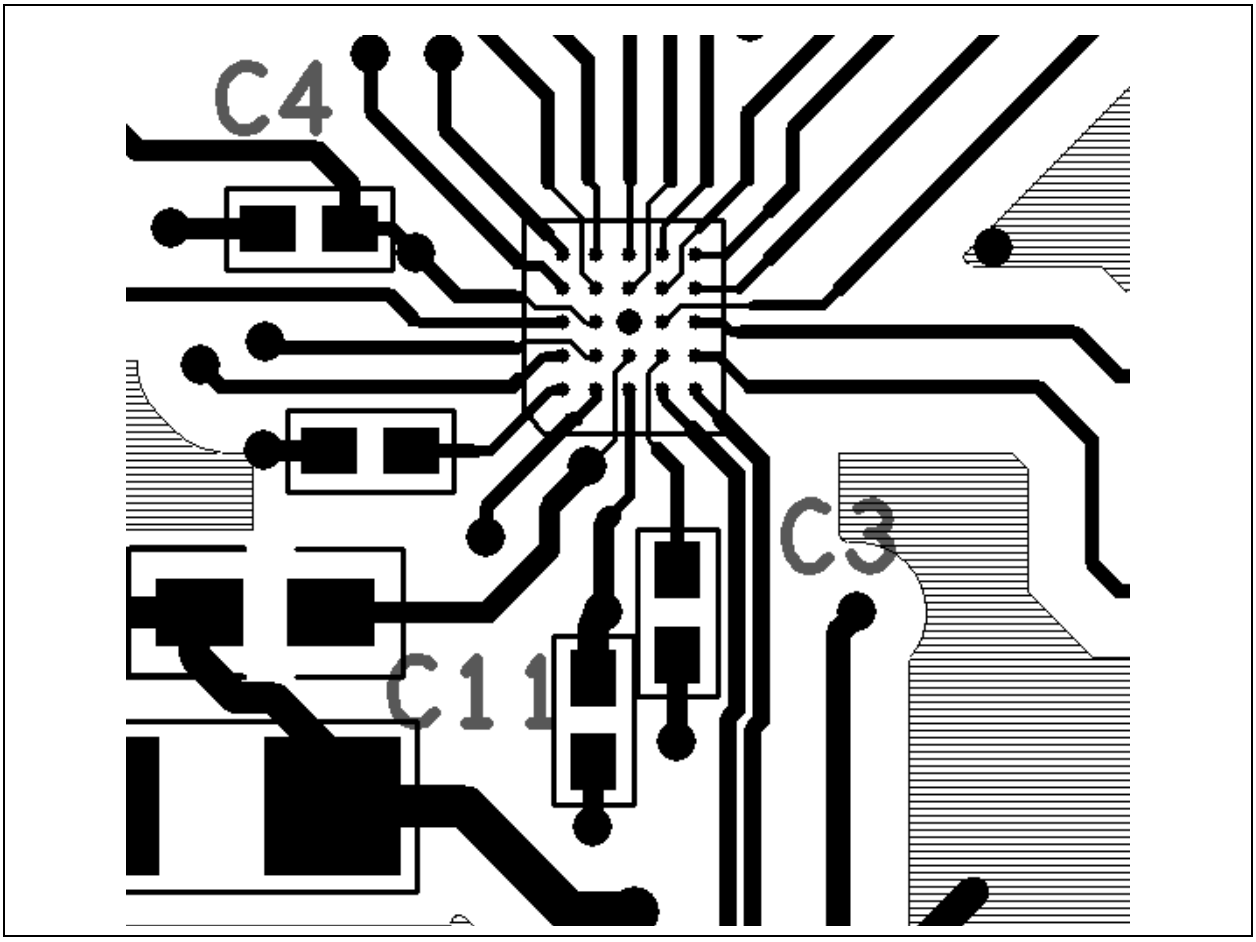
RBIAS

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and noise induced on the RBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS pin and the ground return should be short and direct to VSS with RBIAS placed the same way as bypass capacitors as described in Power Supply Bypass Capacitors. Traces for resistor should be very short and isolated from nearby traces if possible.

Power Supply Bypass Capacitors

Bypass capacitors should be placed close to respective supply pins of the USB332x for optimum power supply decoupling and connected with short, wide traces. The USB332x CRB has bypassing near respective power pins, with return current paths tied to internal ground plane. Refer to the USB332x data sheet for bypass cap values and ESR requirements.

FIGURE 2: C3, C4 AND C11 ARE THE DECOUPLING FOR SUPPLY PINS



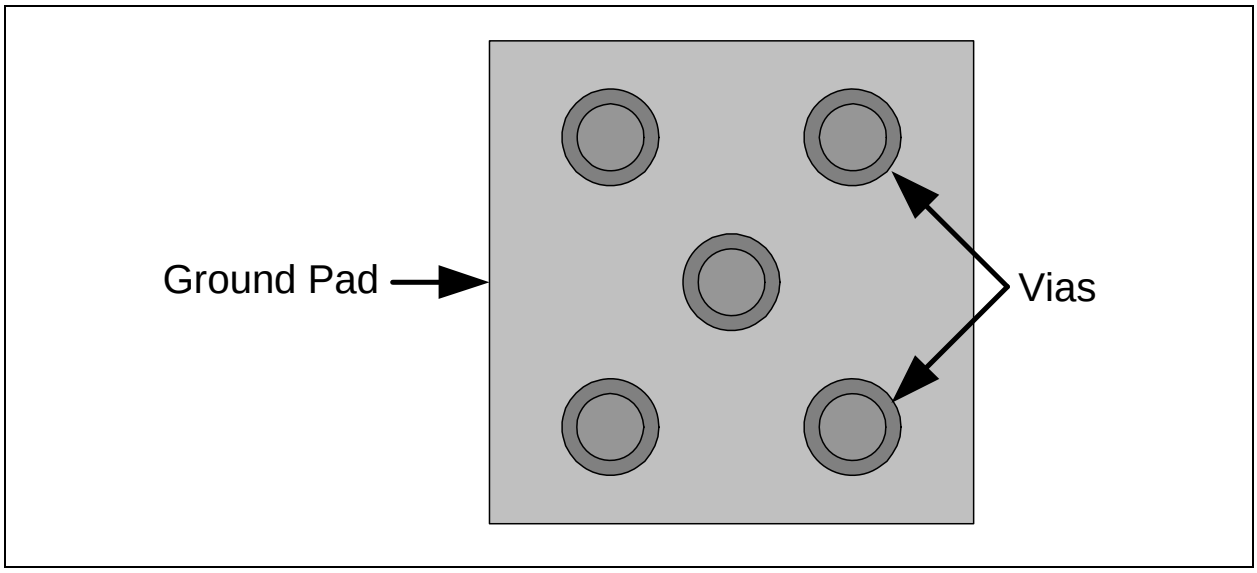
VIAS in Pad for WLCSP Package

The USB332x die is packaged in a 25 ball WLCSP package. The Microchip USB332x Customer Reference Board is routed with all signal traces on the primary side of the PCB with the center ground pin shorted directly to the underlying ground plane utilizing the via-in-pad technology. A 13 mil pad with 6 mil drill is used which has resulted in excellent signal integrity performance. Industry standards and practices need to be observed when using the via-in-pad technology.

VIAS in Ground Flag for QFN Package (USB3320 Only)

Vias to ground are required inside the ground pad under the USB3320. Microchip recommends using five vias in a symmetrical pattern, as shown in Figure 3.

FIGURE 3: RECOMMENDED GROUND PAD VIA ARRAY



Crystal Placement and Routing (USB3320 Only)

In addition to the general guidelines for the USB332x family of USB transceivers, the USB3320 requires some additional guidelines for the crystal placement and routing.

- The crystal should be placed as close as possible to the USB3320.
- The lengths of signals XO and XI should be kept as short as possible (<1”, if possible).
- Capacitors on XI and XO should be placed as close as possible to the crystal. (For applications using a ceramic resonator, capacitors are not required.)

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002958A (02-14-19)	Replaces previous SMSC version Rev. 1.0 (11-26-12)	
Rev. 1.0 (11-26-12)	Document co-branded: Microchip logo added, modification to legal disclaimer	
Rev. 0.9 (11-25-08)	Initial document creation	

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