USB3503

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB3503. These checklist items should be followed when utilizing the USB3503 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 17. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Optional External I^2C Configuration"
- Section 9.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The **VSS** pin (pin C3) should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.3 USB-IF-Compliant USB Connectors

- The USB3503 upstream port is HSIC, which is intended to be directly connected to an embedded host processor; standard USB connectors do not support HSIC. The hub downstream facing ports are Type-A. USB-IF-certified USB connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER

3.1 Power and Bypass Capacitance

- The **VBAT** pin (pin B2) and the **VDD_CORE_REG** pin (pin A3) should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDD33_BYP** pin (pins A5 and A2) requires a 4.7 µF bypass capacitor.
- The **VDD12_BYP** pin (pin D3) should include 1.0 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS

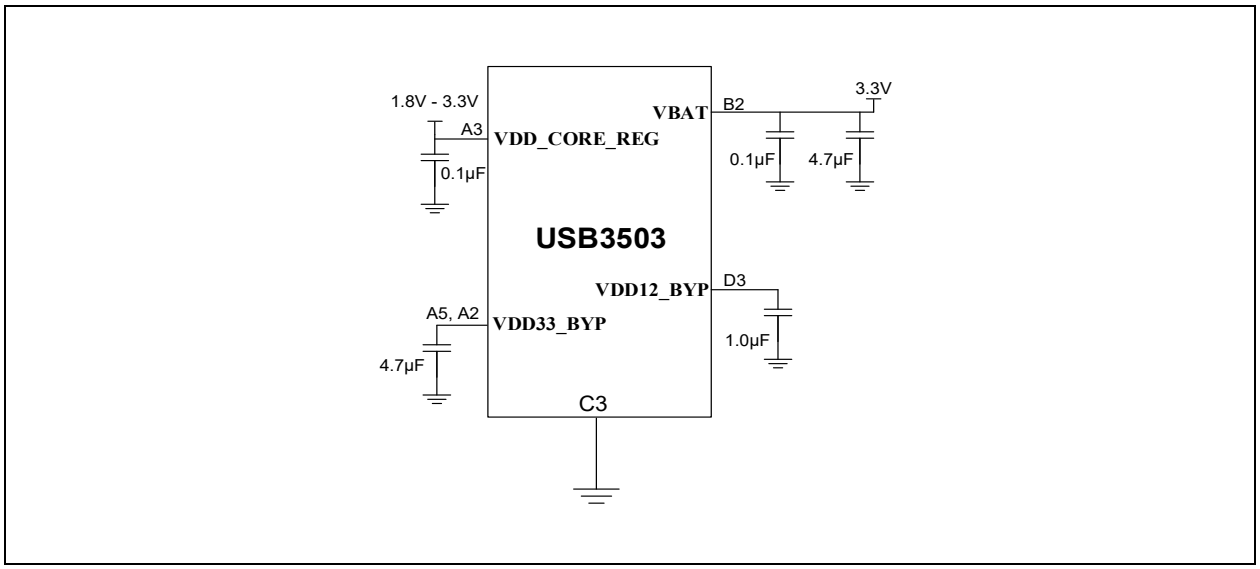
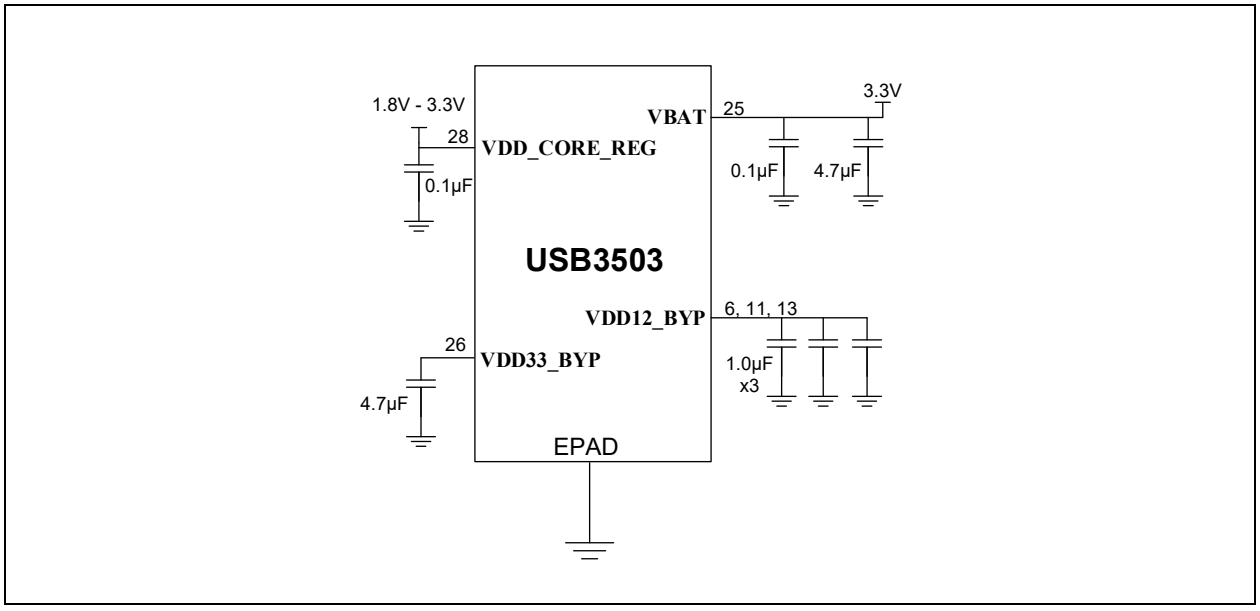


FIGURE 3-2: POWER AND GROUND CONNECTIONS—SQFN



4.0 USB SIGNALS

4.1 USB PHY Interface

- **DATA** (pin E2): This pin is the DATA signal of the upstream HSIC. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the DATA pin of a HSIC link partner.
- **STROBE** (pin E1): This pin is the STROBE signal of the upstream HSIC. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the STROBE pin of a HSIC link partner.
- **USBDNx_DP** (pins A1, C2, and C1): These pins are the positive (+) signal of the downstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D+/DP pin of a USB connector.

- **USBDNx_DM** (pins B1, D2, and D1): These pins are the negative (-) signal of the downstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D-/DM pin of a USB connector.

  Note: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^2C configuration registers.

For transmit and receive channel connections details, refer to Figure 4-1 and Figure 4-3.

FIGURE 4-1: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS UPSTREAM USB PORTS

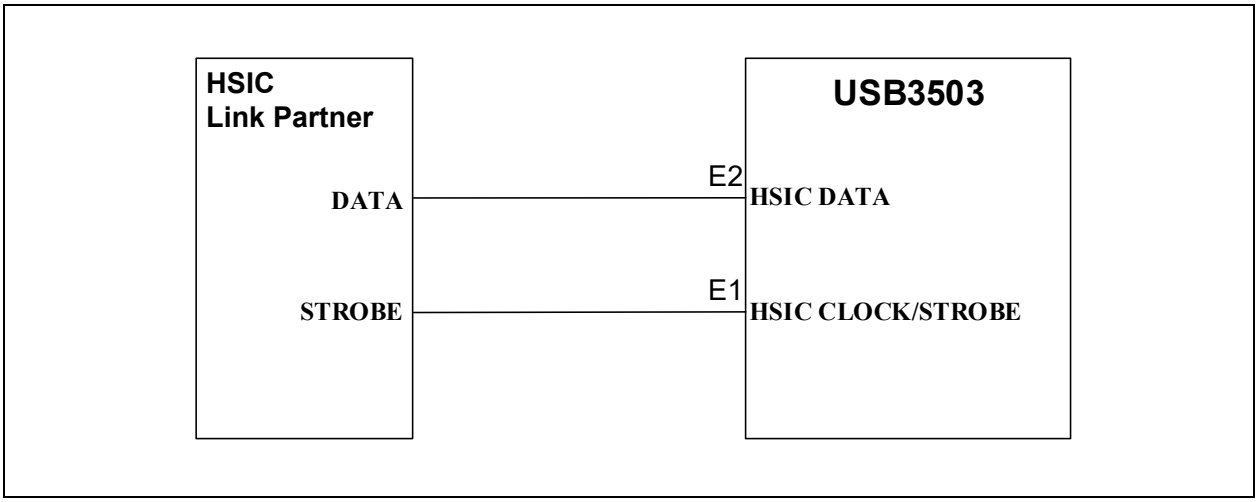


FIGURE 4-2: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS UPSTREAM USB PORTS—SQFN

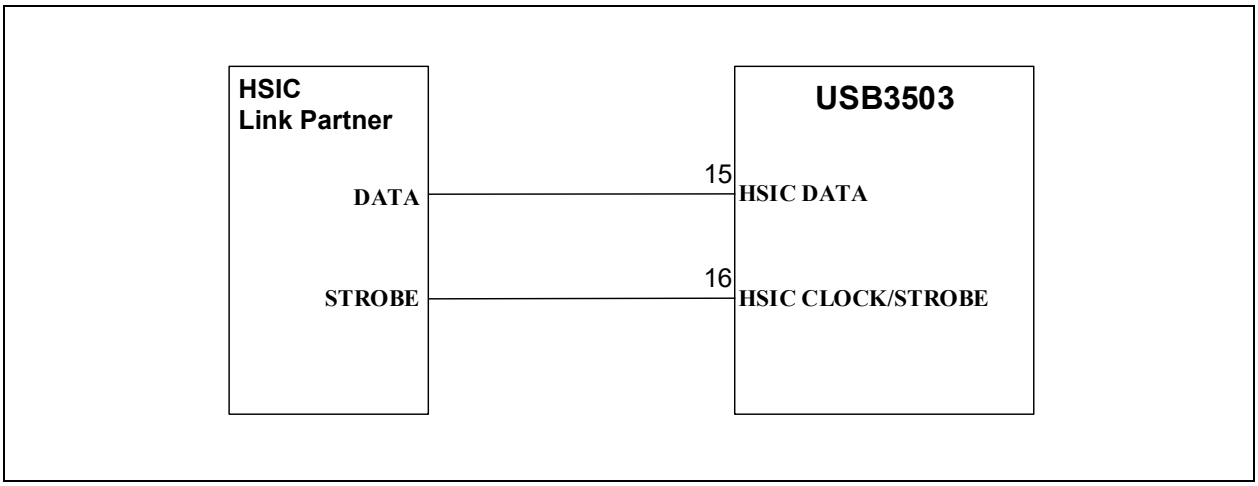


FIGURE 4-3: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS MIXED USB PORTS

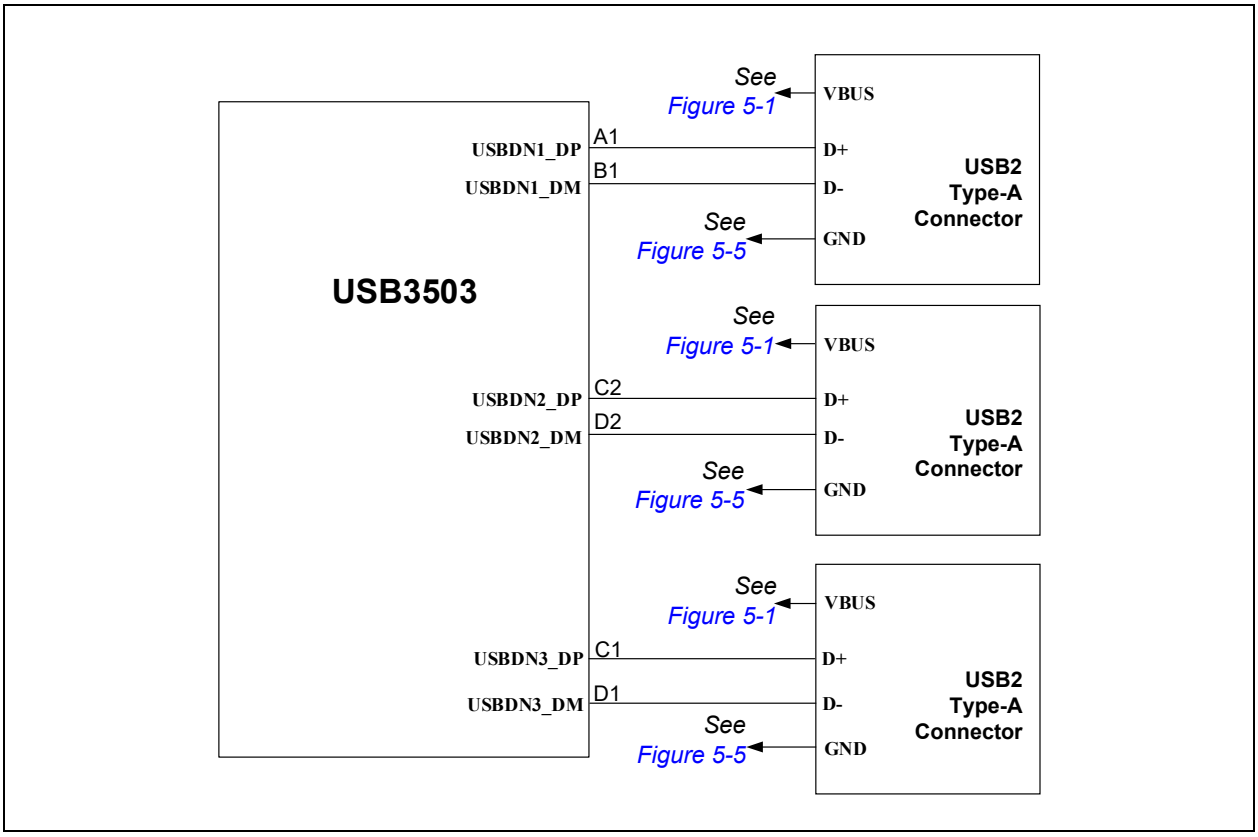
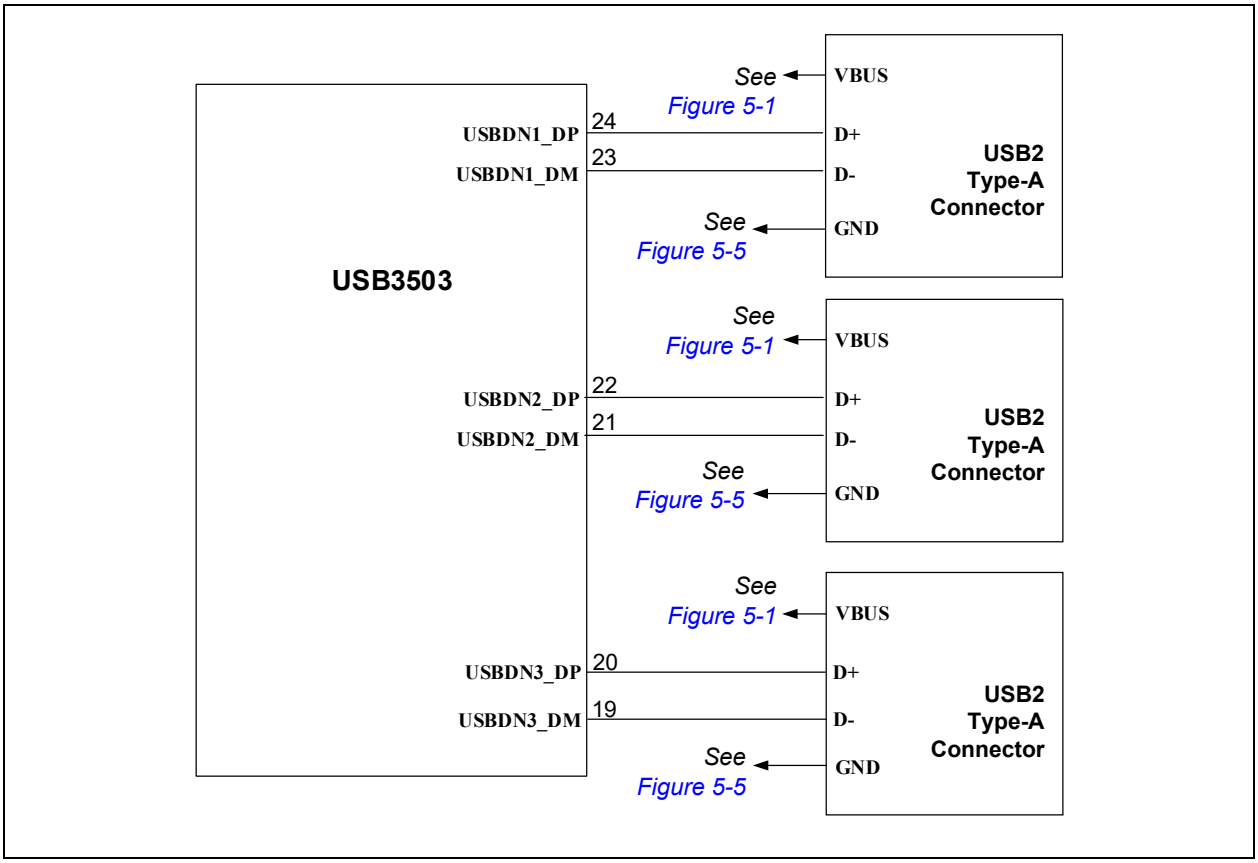


FIGURE 4-4: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS MIXED USB PORTS—SQFN



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

If downstream ports are unused, they should be disabled. This can be achieved through hub configuration (I^2C or OTP), or through a port disable strap option.

If using the port disable strap option, the USBDNx_DP and USBDNx_DM signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor.

4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC-overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB3503 can be used in conjunction with these types of devices, but these devices may have negative effect on USB signal integrity. Thus, it is important to select components accordingly and follow implementation guidelines from the device manufacturer. The following general guidelines for implementing these devices may also be followed:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place these devices as close as possible to the USB connector.

- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note: Microchip PHYBoost, VariSense, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate setting using lab experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and HUB_CONNECT

The USB3503 uses the HUB_CONNECT pin to detect the presence of an HSIC link partner. The USB3503 moves to the Hub Communication stage when this pin is asserted high. If the HUB_CONNECT pin is connected directly to the VDD33_BYP, the hub automatically transitions to the Hub Communication stage.

The INT_N is used as either a general interrupt that indicates when one of the interrupt status registers has been updated or a suspend interrupt that indicates the state of the hub.

The recommended implementation is shown in Figure 5-1.

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND HUB_CONNECT CONNECTIONS

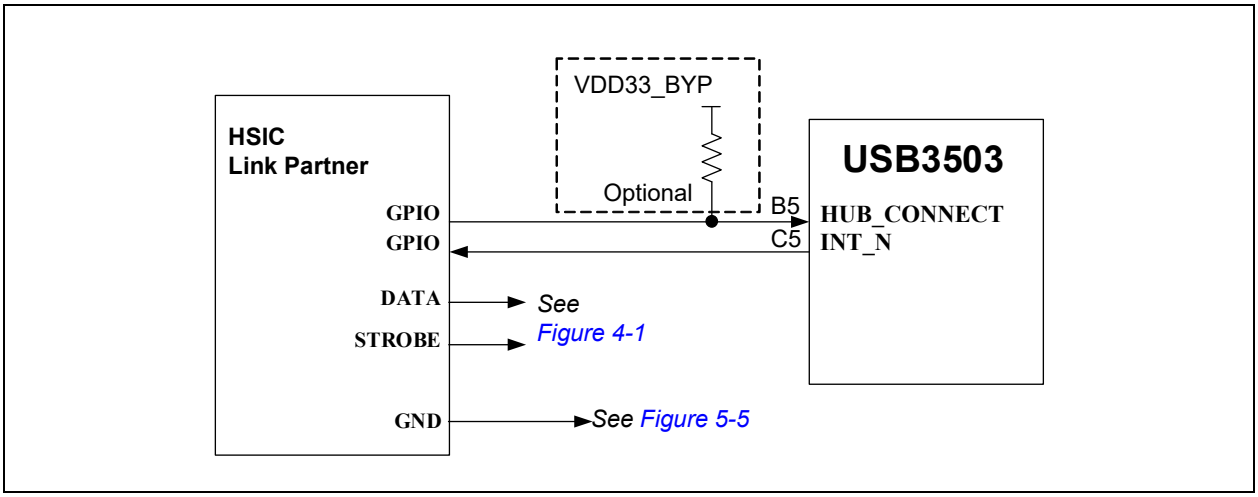
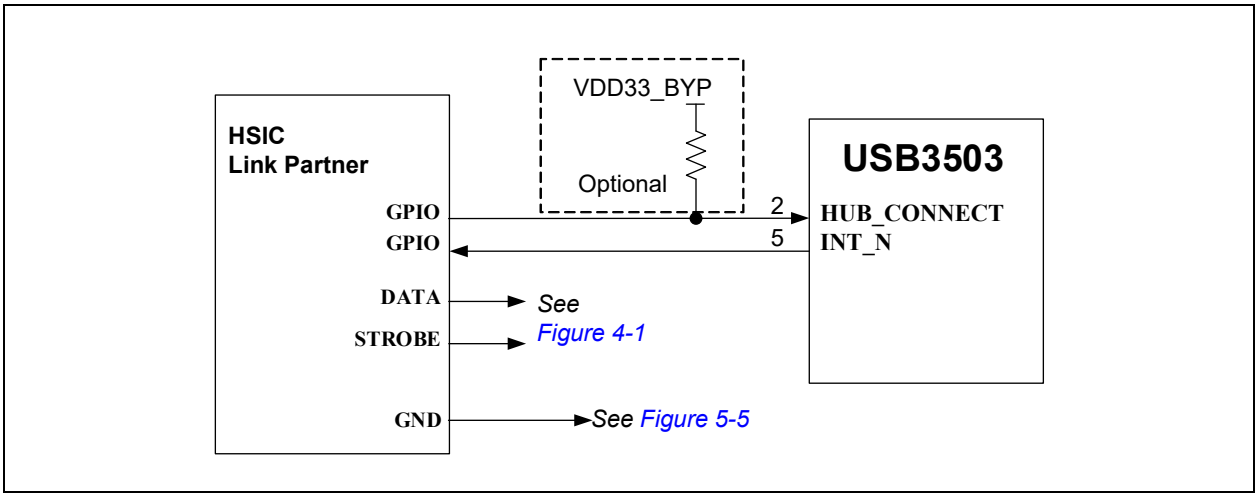


FIGURE 5-2: RECOMMENDED UPSTREAM PORT VBUS AND HUB_CONNECT CONNECTIONS—SQFN



5.2 Downstream Port VBUS and PRTPWR/OCS_N

The **PRTPWR** and the **OCS_N** pins are hybrid I/O pins that support the following states:

- *PORT OFF*: **PRTPWR** is an output and drives low. The **PRTPWR** pin only transitions to the PORT ON state through a specific command from the USB host.
- *PORT ON*: The **OCS_N** is an input buffer that monitors overcurrent events, which are indicated by the port power controller by pulling the OCS_N line low. Once an overcurrent event is detected, the PRTPWR automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRTPWR/OCS_N** pins to a port power controller, the signals should be connected to both the enable pin and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note: The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

A typical implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PRTCTL CONNECTIONS

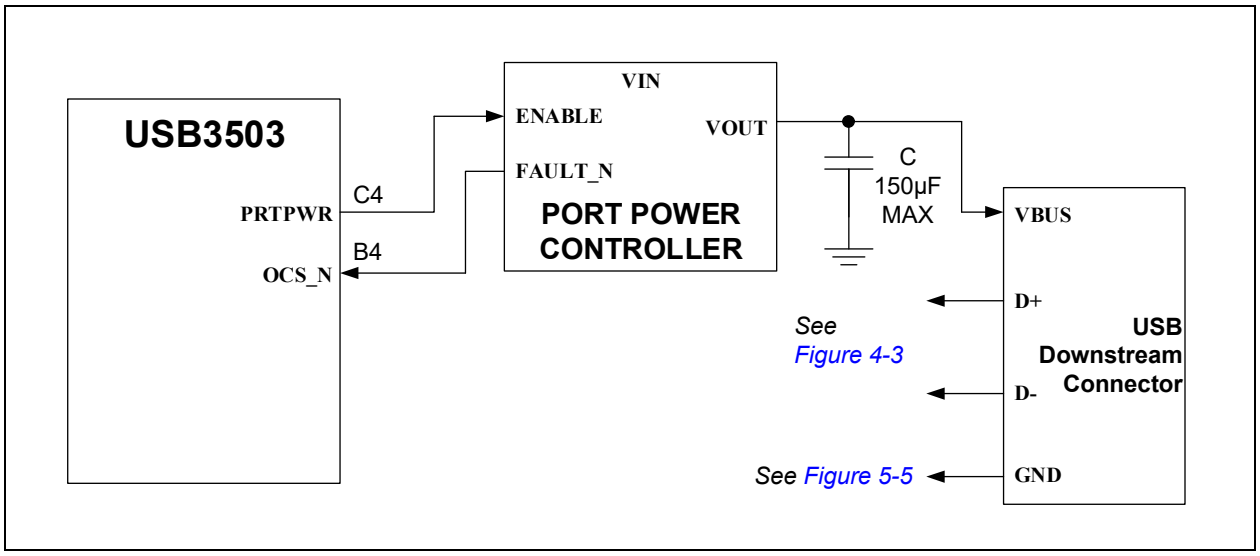
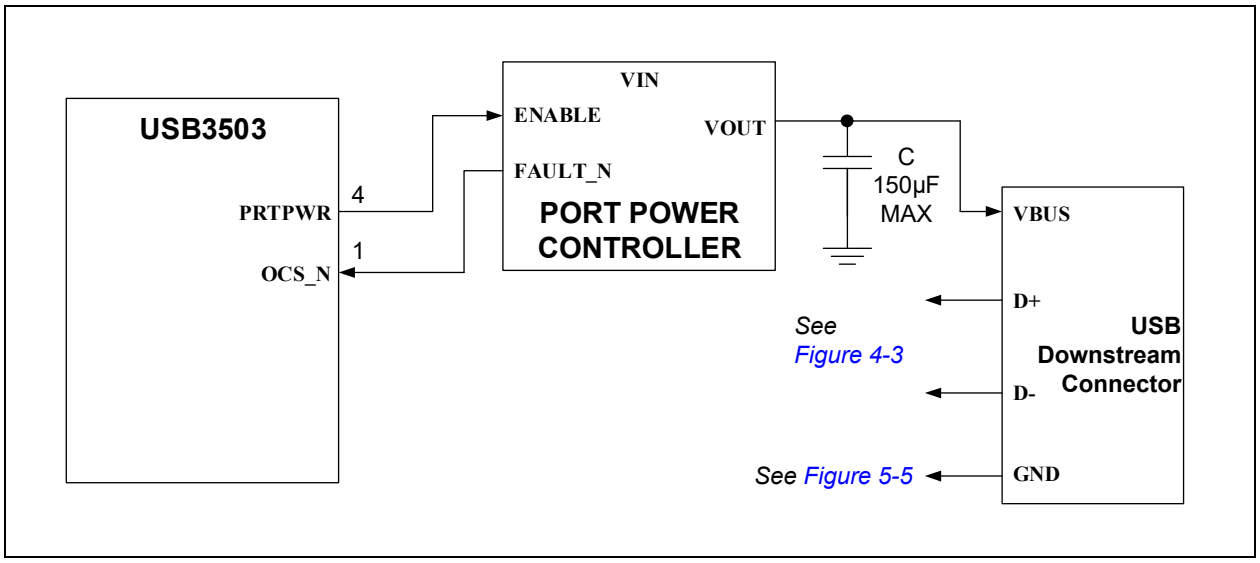


FIGURE 5-4: DOWNSTREAM VBUS AND PRTCTL CONNECTIONS—SQFN



Note: The implementation as shown in Figure 5-3 assumes that the port power controller has an active-high enable input, and an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 GND and EARTH Recommendations

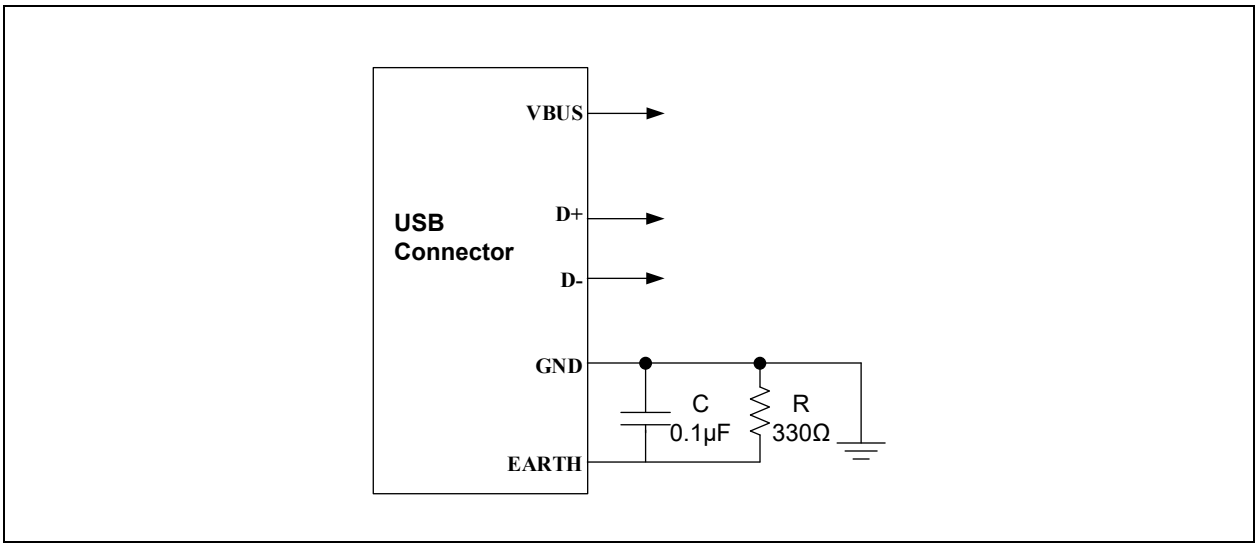
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) Connect to GND through a resistor and capacitor in parallel. A resistor-capacitor (RC) filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Connect directly to the GND plane.

The recommended implementation is shown in Figure 5-5.

FIGURE 5-5: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 External Clock Connection

The REFCLK reference clock is the source clock for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB3503 Data Sheet*.

- **REFCLK** (pin B3) is the clock circuit input for USB3503.
- **REF_SEL1** (pin D4) is the reference clock select 1 input for USB3503.
- **REF_SEL0** (pin E4) is the reference clock select 0 input for USB3503.

TABLE 6-1: REFERENCE CLOCK FREQUENCIES

REF_SEL[1:0]	Frequency
'00'	38.4 MHz
'01'	26 MHz
'10'	19.2 MHz
'11'	12 MHz

FIGURE 6-1: OSCILLATOR CONNECTIONS

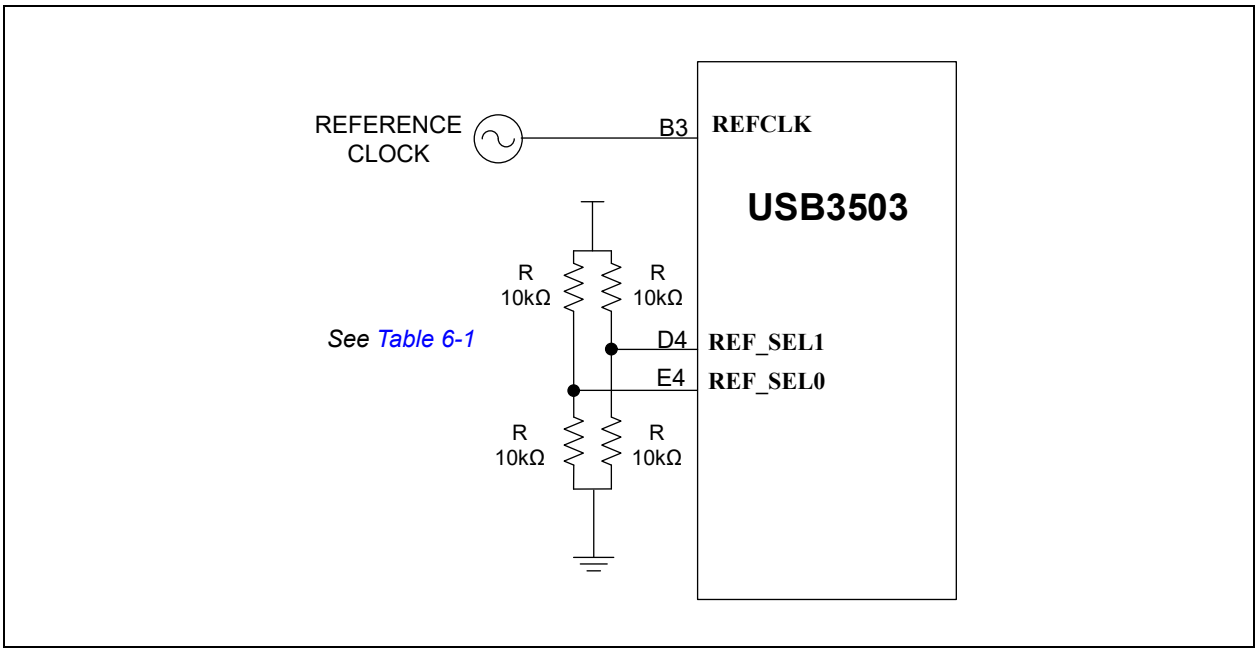
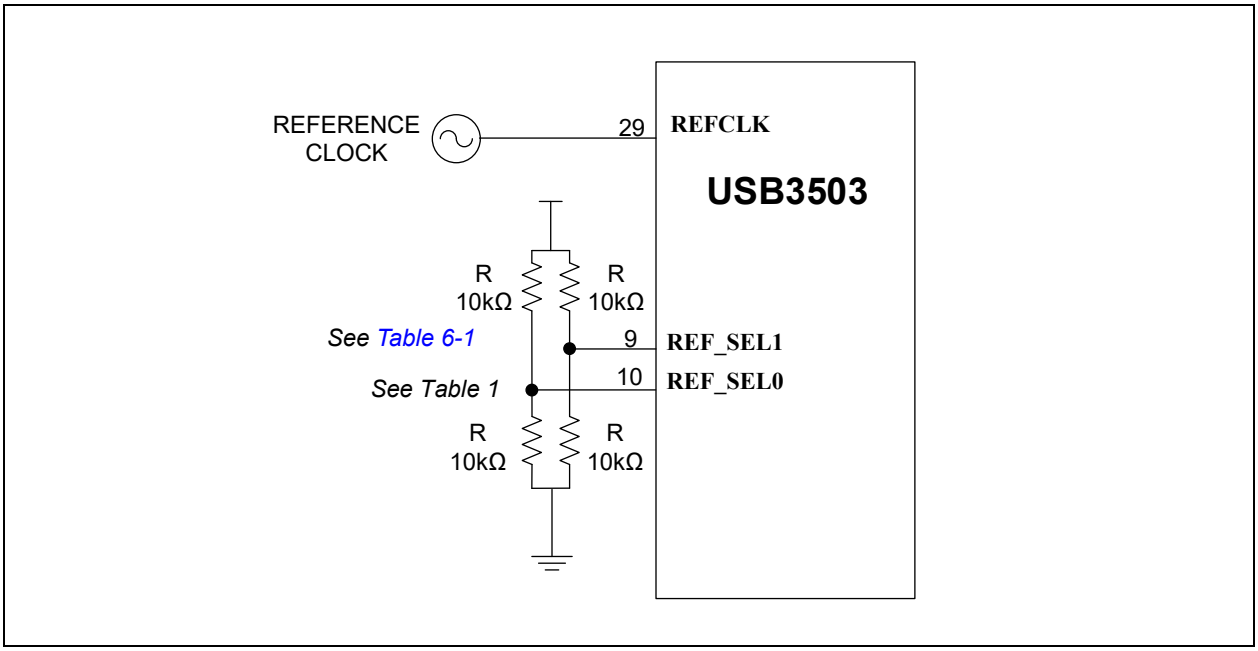


FIGURE 6-2: OSCILLATOR CONNECTIONS—SQFN



7.0 POWER AND STARTUP

7.1 Board Power Supplies

7.1.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB3503 Data Sheet*.

If a monotonic or fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

7.1.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. Please refer to the product data sheet for the power requirements for the specific device. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 2.4A (if certain vendor-specific current negotiation with the USB host is enabled) to the USB downstream port VBUS without dropping below the minimum voltage permissible in the USB specification.

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized, such that it is able to supply the maximum power consumption specification as displayed in the *USB3503 Data Sheet*.

7.2 Reset Circuit

RESET_N (pin E3) is an active-low reset input. This signal resets all logic and registers within the USB3503. A hardware reset (RESET_N assertion) is not required following power-up. Refer to the latest copy of the *USB3503 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB3503 when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

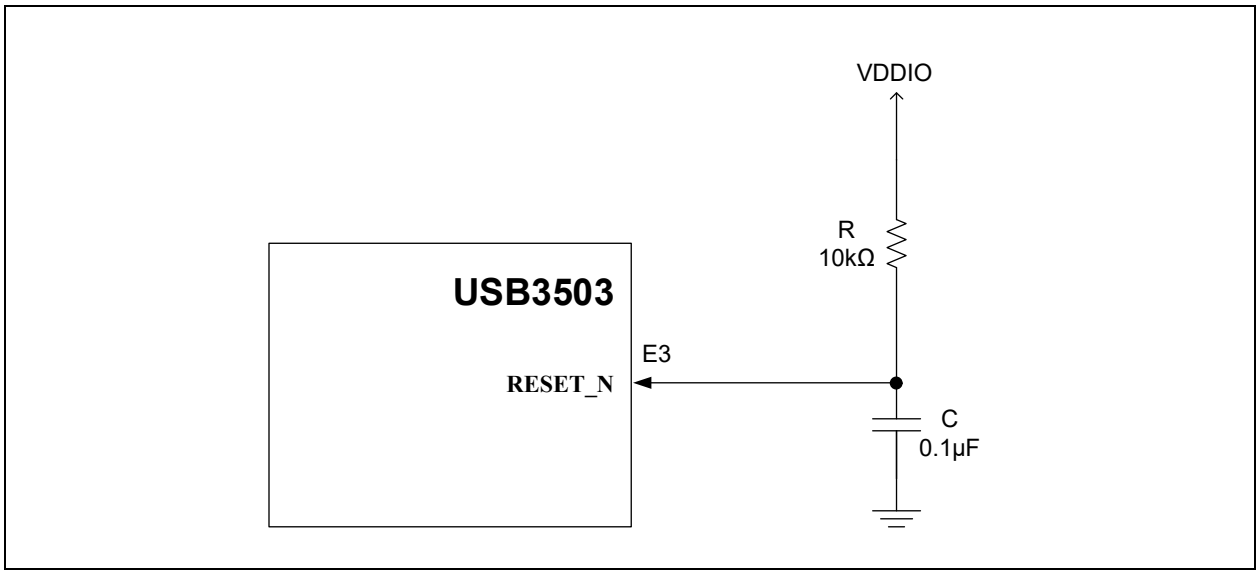


FIGURE 7-2: RESET TRIGGERED BY POWER SUPPLY—SQFN

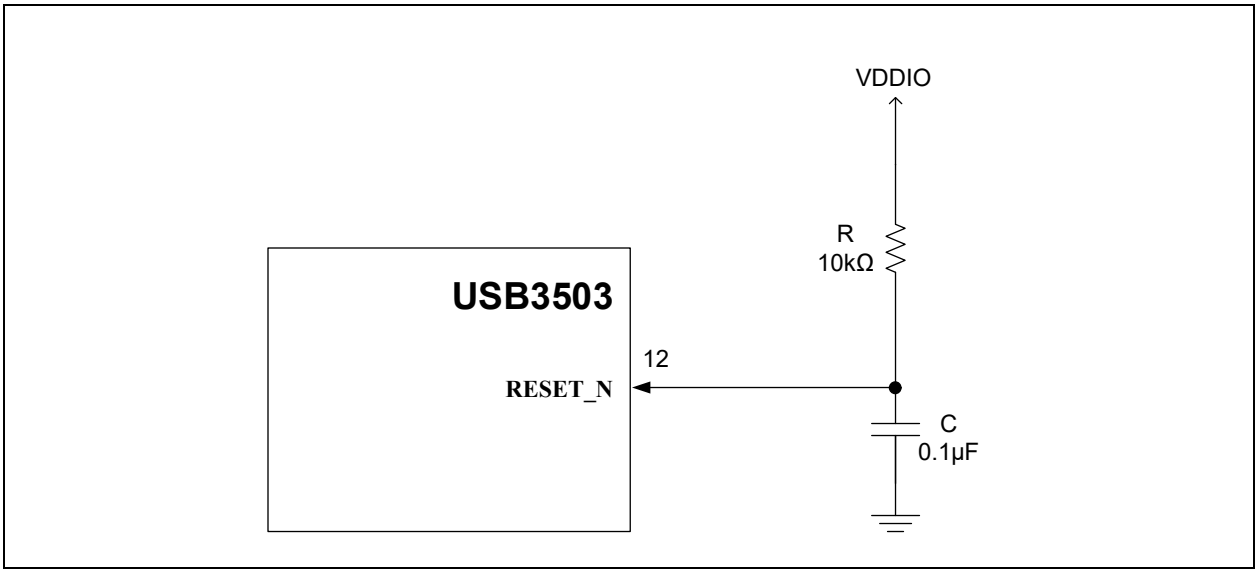


Figure 7-3 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm reset after power-up.

FIGURE 7-3: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT

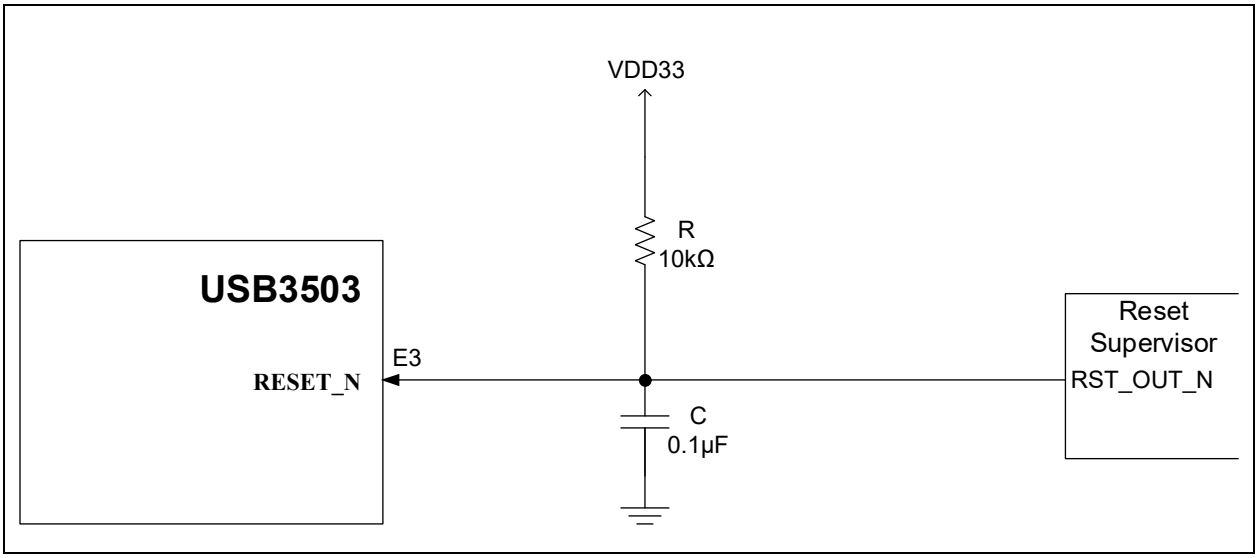
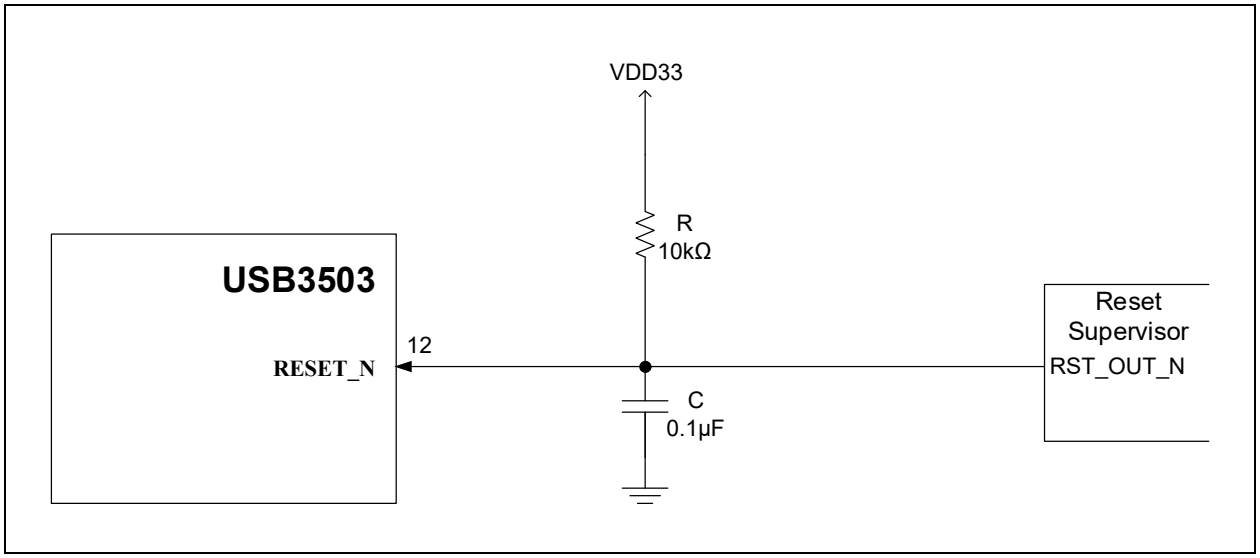


FIGURE 7-4: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT—SQFN



8.0 OPTIONAL EXTERNAL I²C CONFIGURATION

8.1 Optional I²C Operation Summary

By default, the USB3503 loads configuration registers from an internal read only memory (ROM). The USB3503 supports optional configuration execution from an external EEPROM device. An EEPROM is only required if a custom configuration settings are required for the application.

8.2 I²C Connection Diagrams

If an I²C device is used, the recommended schematic connections are shown in Figure 8-1.

FIGURE 8-1: I²C CONNECTIONS—WLCSP PACKAGE

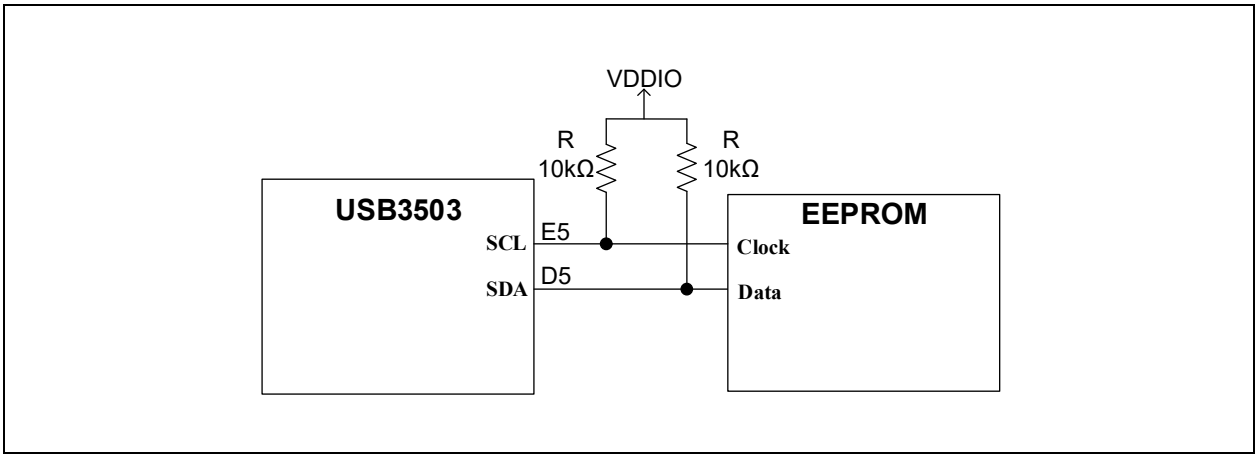
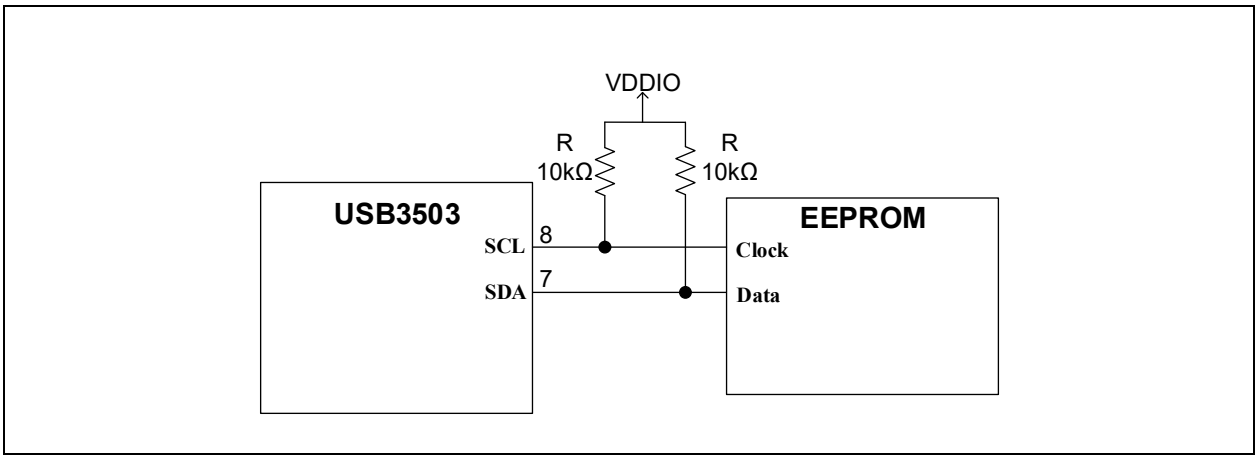


FIGURE 8-2: I²C CONNECTIONS—VQFN PACKAGE



9.0 MISCELLANEOUS

9.1 Self-Powered/Bus-Powered Settings

In a typical USB3503 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

Note: The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host typically limits the downstream ports of a bus-powered hub to 100 mA. Any device that connects to a bus-powered hub, which declares it needs more than 100 mA, will be prevented from operating by the USB host.

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
	Section 2.3, "USB-IF-Compliant USB Connectors"	Verify that USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.1, "Power and Bypass Capacitance"	• Ensure **VBAT** is in the range 3.0V to 3.6V and a 0.1 µF capacitor is on the pin • Ensure **VDD33_BYP** has a 1.0 µF capacitor to GND. • Ensure **VDD12_BYP** has a 0.1 µF capacitor connected to GND.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance of the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and HUB_CONNECT"	Ensure **HUB_CONNECT** is connected to the appropriate control signal of the host processor.		
	Section 5.2, "Downstream Port VBUS and PRTPWR/OCS_N"	Verify that **PRT_CTL** is properly connected to both the enable pin of the downstream port power controller and the fault indicator output of the port power controller.		
	Section 5.3, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. It is recommended that an RC filter be placed between the SHIELD pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "External Clock Connection"	Confirm the REFCLK input is connected to a positive square wave clock source from 0V to 3.6V.		
Section 7.0, "Power and Startup"	Section 7.1, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V to 3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the RESET_N line is held low until the power regulators reach a steady state.		
	Section 7.2, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Optional External I²C Configuration"	Section 8.1, "Optional I²C Operation Summary"	Determine if a custom configuration is required and which mode of operation the selected I²C device must support.		
	Section 8.2, "I²C Connection Diagrams"	If the USB to I²C/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I²C/SMBus master is correct. Verify that all slave devices have a different I²C/SMBus address. Verify that the hub and all slave devices can support the targeted bus speed. Note that pull-up resistors are detected on the I²C/SMBus slave interface, the USB hub will not enumerate to a USB host until it receives the special “Attach” command from the I²C/SMBus master.		
	Section 8.2, "I²C Connection Diagrams"	Verify that the I²C is connected according to the diagrams in Figure 8-1.		
Section 9.0, "Miscellaneous"	Section 9.1, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If Self-Powered operation is required, then no additional configuration or circuitry is required. If Bus-Powered operation is required, then the hub must be configured via OTP or I²C/SMBus.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004239A (10-15-21)	Initial release	

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