PolarFire SLVS-EC Receiver IP User Guide

Introduction (Ask a Question)

SLVS-EC is Sony's high-speed interface for next-generation high-resolution CMOS image sensors. This standard is tolerant of lane-to-lane skew because of embedded clock technology. It makes a board-level design easy in terms of high-speed and long-distance transmission.

SLVS-EC Rx IP core provides SLVS-EC interface for PolarFire® FPGA to receive image sensor data. The IP supports speed up to 4.752 Gbps. The IP core supports two, four, and eight lanes for RAW 8, RAW 10, and RAW 12 configurations.

SLVS_EC Receiver Summary

Core Version	This document applies to SLVS_EC Receiver v4.2.
Supported Device Families	• PolarFire® SoC • PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	• Native Interface • AXI4 Stream Interface
Licensing	The core is license-locked for clear text RTL. It supports the generation of Encrypted RTL for the Verilog version of the core with no license.
Installation Instructions	SLVS_EC Receiver must be installed in the IP Catalog automatically through the IP Catalog update function. Alternatively, SLVS_EC Receiver could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for SLVS_EC Receiver is listed in Resource Utilization.

Supported Features

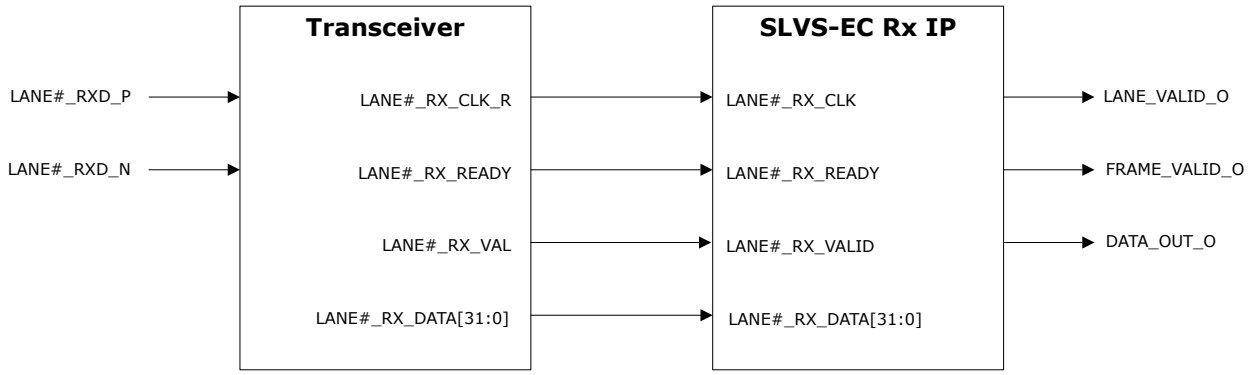
SLVS-EC Specification Version	SLVS-EC v2.0
Baud Grades	1:1188 2:2376 3:4752
Pixel Formats	Raw 8, Raw 10, and Raw 12
Lanes	2, 4, and 8
Embedded Data	Supports embedded packet decoding for 2, 4, and 8 lanes

Unsupported Features

Baud Grades	4:9216 to 10000
Lanes	1
CRC and ECC	Not supported

The following figure shows the system diagram for the SLVS-EC camera solution.

Figure 1. SLVS-EC IP Block Diagram



PolarFire transceiver is used as the PHY interface for the SLVS-EC sensor since the SLVS-EC interface uses embedded clock technology. It also uses 8b10b encoding, which can be recovered using the PolarFire transceiver. PolarFire FPGA has up to 24 low-power 12.7 Gbps transceiver lanes. These transceiver lanes can be configured as the SLVS-EC PHY receiver lanes. As shown in the preceding figure, the transceiver outputs are connected to SLVS-EC Rx IP core.

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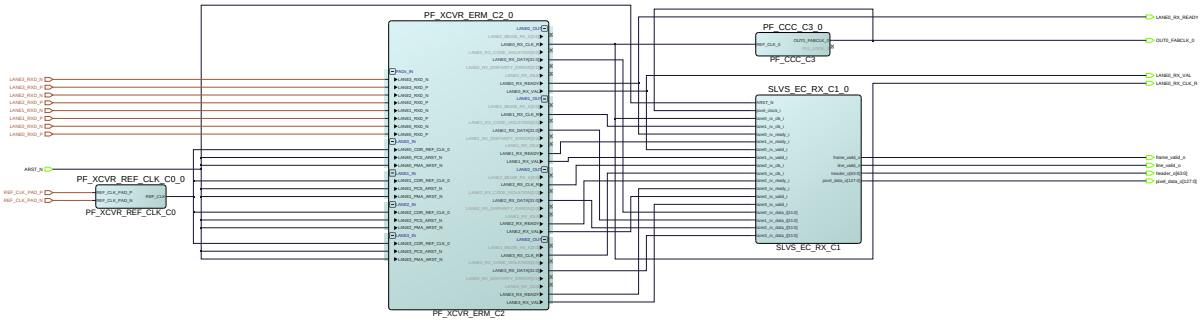
1. SLVS-EC Receiver Solution (Ask a Question)

The following figure shows the Libero SoC software top level design implementation of SLVS-EC IP and the required components for the SLVS-EC receiver solution.

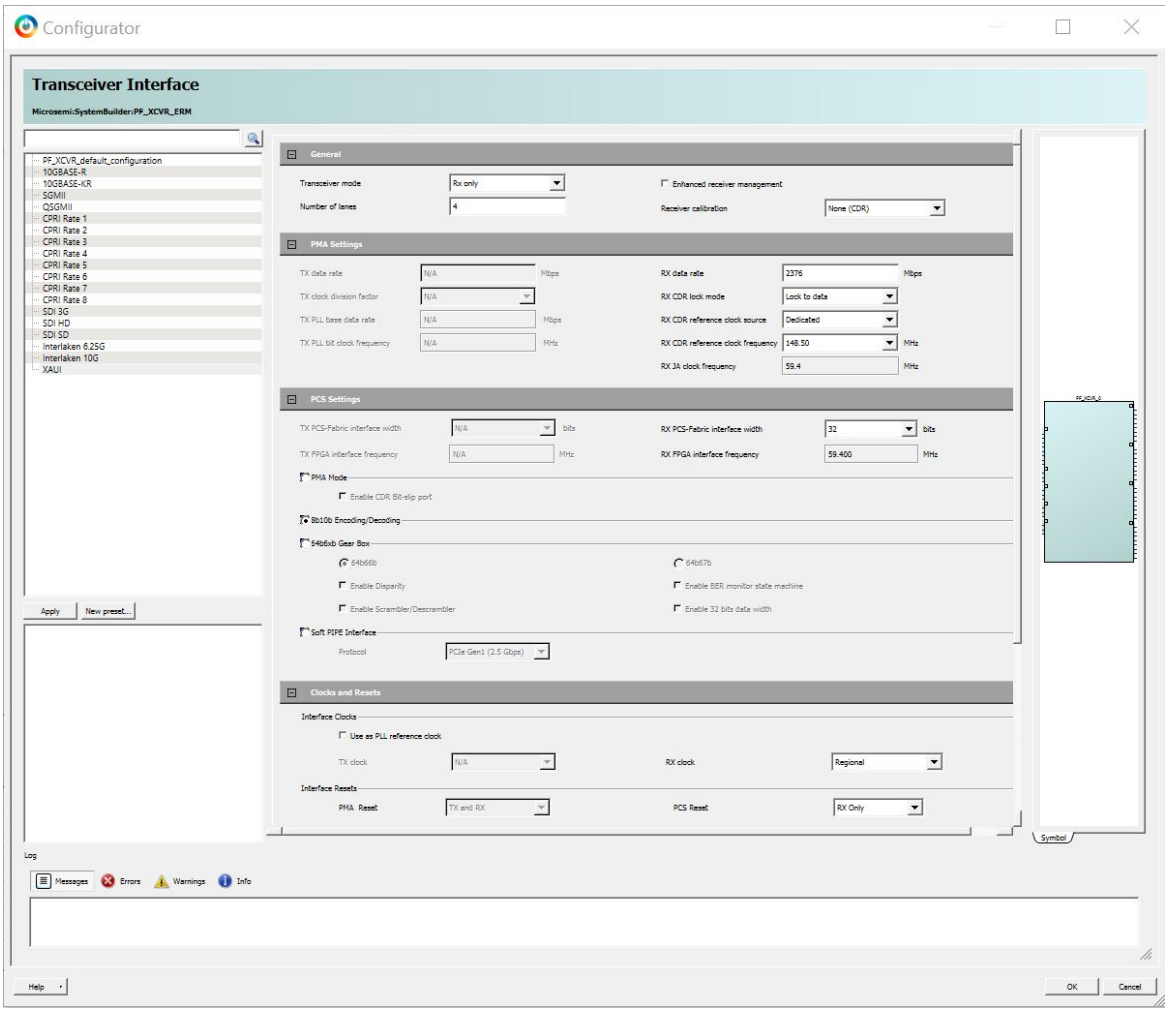
Figure 1-1. SLVS-EC IP SmartDesign



2. Transceiver Configuration (Ask a Question)

The following figure shows the transceiver interface configuration.

Figure 2-1. Transceiver Interface Configurator



The transceiver can be configured for either two or four lanes. The speed of the transceiver is set using the 'Transceiver Data Rate.' The following table shows the SLVS-EC interface, which supports two baud rates.

Table 2-1. SLVS-EC Baud Rate

Baud Grade	Baud Rate in Mbps
1	1188
2	2376
3	4752

Set the reference clock frequency as per the clock source connected to the transceiver.

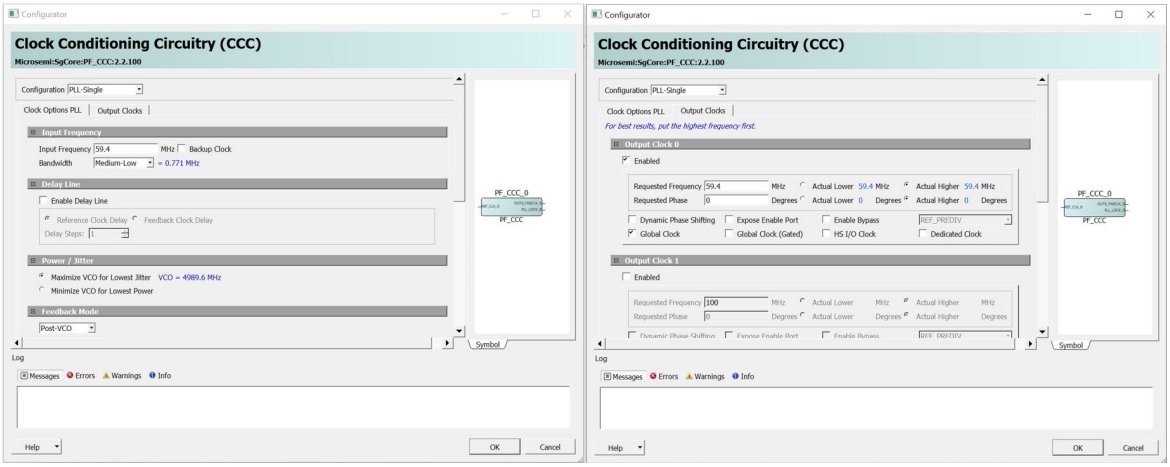
2.1 PLL for Pixel Clock Generation (Ask a Question)

A PLL is required to generate pixel clock from the Transceiver generated Fabric clock that is, LANE0_RX_CLOCK. Following is the formula to generate pixel clock.

Pixel clock = (LANE0_RX_CLOCK × 8)/DATA_WIDTH

Configure the PF_CCC for RAW 8 as shown in the following figure.

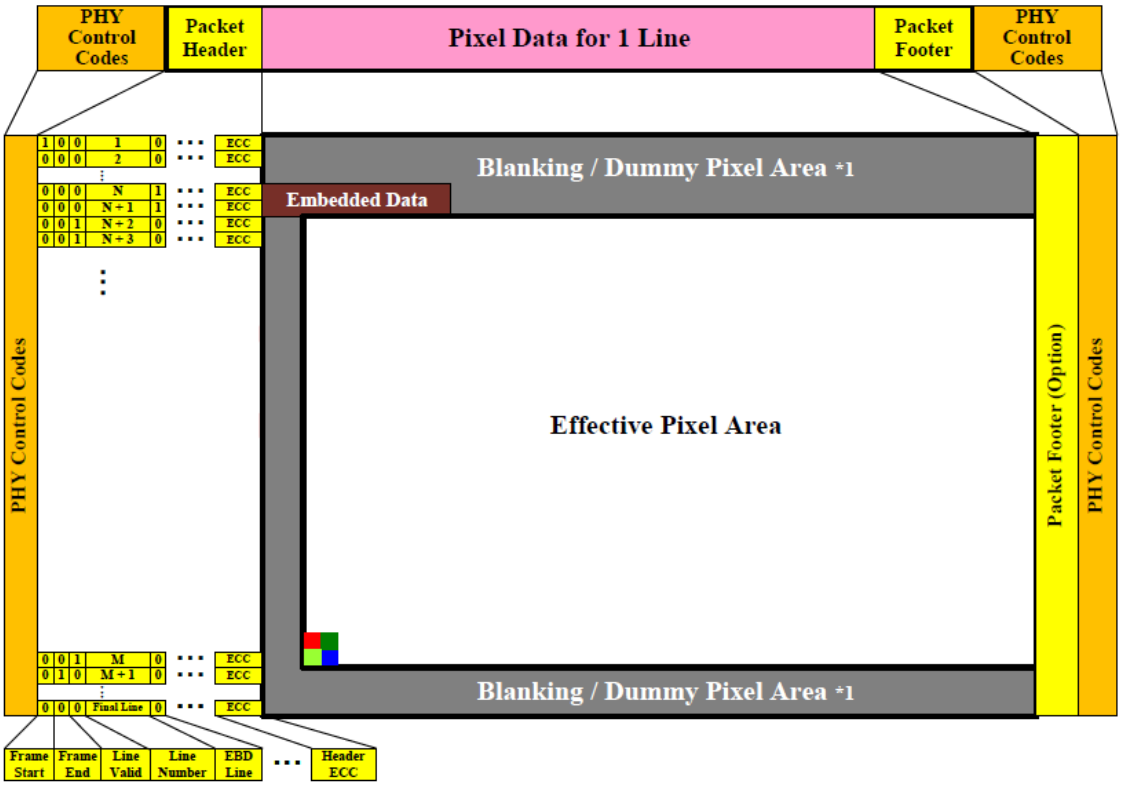
Figure 2-2. Clock Conditioning Circuitry



3. Design Description (Ask a Question)

The following figure shows the SLVS-EC Frame Format structure.

Figure 3-1. SLVS-EC Frame Format Structure



The Packet header contains information about the frame start and end signals along with the valid lines. PHY control codes are added above the packet header to form the SLVS-EC packet. The following table lists the different PHY control codes used in the SLVS-EC protocol.

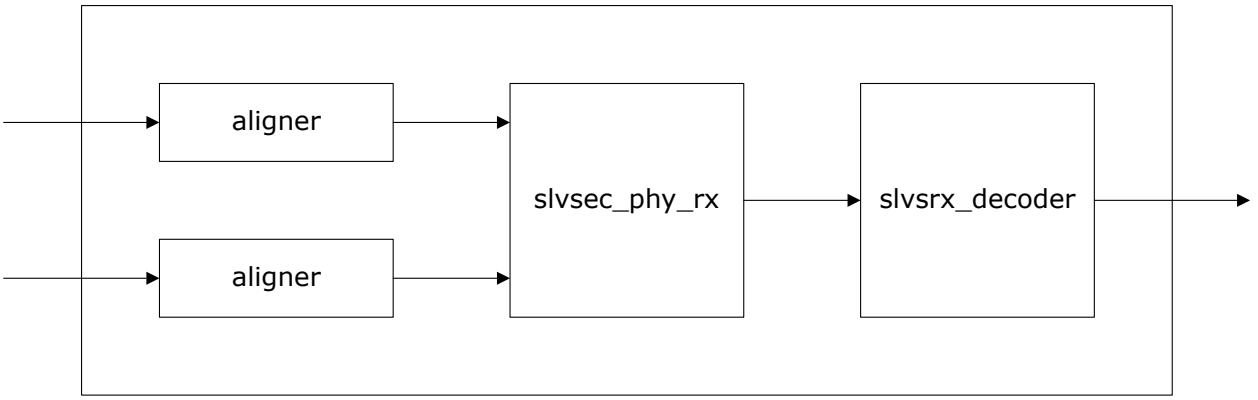
Table 3-1. PHY Control Code

PHY Control Code	8b10b Symbol Combination
Start Code	K.28.5 - K.27.7 - K.28.2 - K.27.7
End Code	K.28.5 - K.29.7 - K.30.7 - K.29.7
Pad Code	K.23.7 - K.28.4 - K.28.6 - K.28.3
Sync Code	K.28.5 - D.10.5 - D.10.5 - D.10.5
Idle Code	D.00.0 - D.00.0 - D.00.0 - D.00.0

3.1 SLVS-EC RX IP Core (Ask a Question)

This section describes the hardware implementation details of SLVS-EC Receiver IP. The following figure shows the Sony SLVS-EC receiver solution that contains the PolarFire SLVS-EC RX IP. This IP is used in conjunction with the PolarFire transceiver interface block. The following figure shows the internal blocks of the SLVS-EC Rx IP.

Figure 3-2. Internal Blocks of the SLVS-EC RX IP



3.1.1 aligner (Ask a Question)

This module receives the data from the PolarFire transceiver blocks and aligns to the sync code. This module looks for the sync code in the bytes received from the transceiver and locks to the byte boundary.

3.1.1.1 slvsec_phy_rx (Ask a Question)

This module receives the data from the aligner and decodes the incoming SLVS PHY packets. This module passes through the synchronization sequence and then, generates the pkt_en signal starting from Start code and ends at the end code. It also removes the PAD code from the data packets and sends the data to the next module that is slvsrx_decoder.

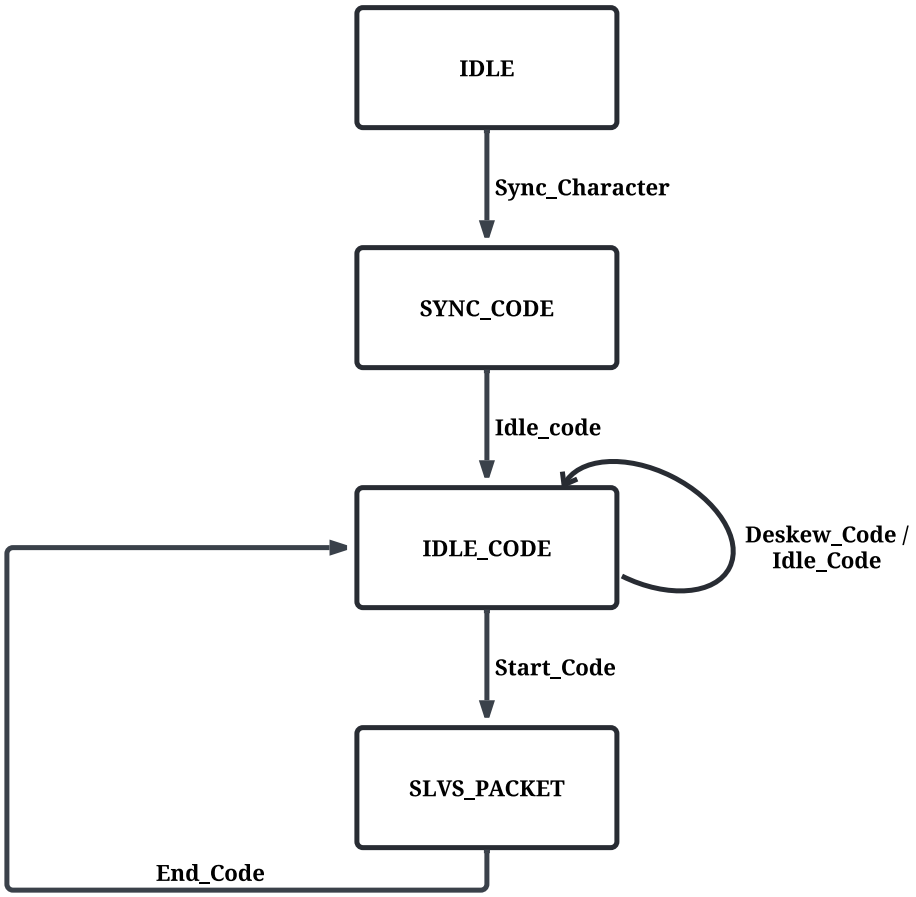
3.1.1.2 slvsrx_decoder (Ask a Question)

This module receives the data from the slvsec_phy_rx module and extracts the pixel data from the payload. This module extracts four pixels per clock per lane and sends to the output. It generates the line valid signal for the active lines validating the active video data. It also generates the Frame valid signal by looking at the frame start and frame end bits in the packet header of the SLVS-EC packets.

3.2 FSM with Data Decoding States (Ask a Question)

The following figure shows the FSM for SLVS-EC RX IP.

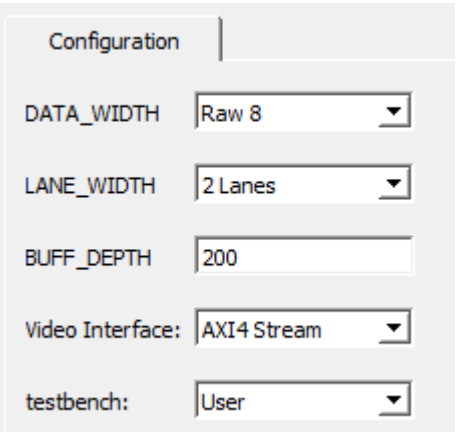
Figure 3-3. FSM for SLVS-EC RX IP



3.2.1 SLVS-EC Receiver IP Configuration (Ask a Question)

The following figure shows the SLVS-EC receiver IP configurator.

Figure 3-4. SLVS-EC Receiver IP Configurator



3.3 Configuration Parameters (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of SLVS-EC receiver IP block. These are generic parameters and can vary based on the application requirements.

Table 3-2. Configuration Parameters

Name	Description
DATA_WIDTH	Input pixel data width. Supports RAW 8, RAW 10, and RAW 12.
LANE_WIDTH	Number of SLVS-EC lanes. Supports two, four, and eight lanes.
BUFF_DEPTH	Depth of the buffer. Number of active pixels in active video line.
Video Interface	Native and AXI4 Stream

Buffer depth can be calculated by using the following equation:

BUFF_DEPTH = Ceil ((Horizontal Resolution × RAW width) / (32 × Lane width))

Example: RAW width = 8, Lane width = 4, and Horizontal Resolution = 1920 pixels

BUFF_DEPTH = Ceil ((1920 × 8)/ (32 × 4)) = 120

3.4 Inputs and Outputs (Ask a Question)

The following table lists the input and output ports of the SLVS-EC RX IP configuration parameters for the native video interface.

Table 3-3. Input and Output Ports For Native Video Interface

Signal Name	Direction	Width	Description
LANE#_RX_CLK_I	Input	1-bit	Recovered clock from the transceiver for that particular Lane
LANE#_RX_READY_I	Input	1-bit	Data ready signal for Lane
LANE#_RX_VALID_I	Input	1-bit	Data Valid signal for Lane
LANE#_RX_DATA_I	Input	32-bit	Lane recovered data from transceiver
LINE_VALID_O	Output	1-bit	Data valid signal for active pixels in a line
FRAME_VALID_O	Output	1-bit	Valid signal for Active lines in a frame
DATA_OUT_O	Output	DATA_WIDTH × LANE_WIDTH × 4	Pixel data output
HEADER_O	Output	64-bits	Packet Header
EBD_VALID_O	Output	1-bit	Embedded Data Valid Signal
LANE#_FSM_STATE_O	Output	4-bits	Current FSM state Value: FSM State 0: IDLE 1: SYNC_CODE 2: IDLE_CODE 3: SLVS_PACKET

The following table lists the input and output ports of the SLVS-EC RX IP configuration parameters for the AXI4 stream video interface.

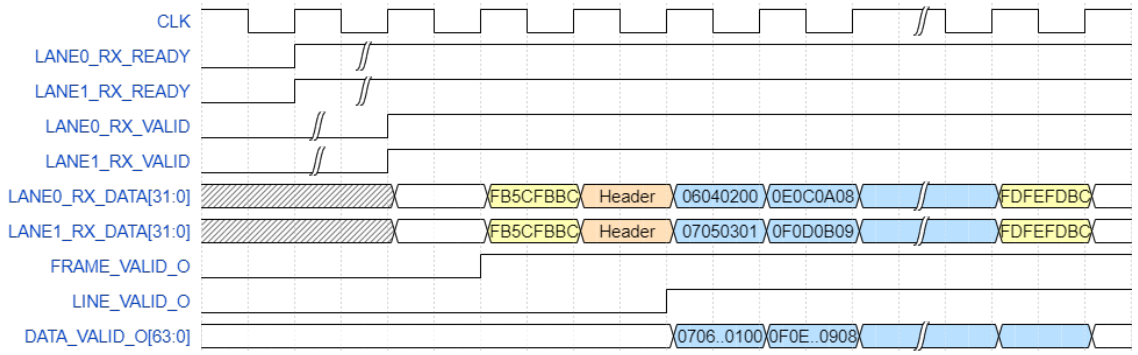
Table 3-4. Input and Output Ports for AXI4 Stream Video Interface

Port Name	Type	Width	Description
ARST_N	Input	1-bit	Active low asynchronous reset signal to design.
PIXEL_CLOCK_I	Input	1-bit	System clock
TDATA_O	Output	4 × g_LANE_WIDTH × g_DATAWIDTH bit	Output Video Data
TVALID_O	Output	1-bit	Output Video Valid
TUSER_O	Output	4-bit	Bit 0 = unused Bit 1 = unused Bit 2 = unused Bit 3 = frame valid
TLAST_O	Output	1-bit	Output Video End of Frame
TSTRB_O	Output	g_DATAWIDTH / 8	Output Video Data strobe
TKEEP_O	Output	g_DATAWIDTH / 8	Output Video Data Keep

4. Timing Diagram (Ask a Question)

The following figure shows the SLVS-EC IP timing diagram.

Figure 4-1. SLVS-EC IP Timing Diagram



SLVS-EC IP output is placed from LSB to MSB, and the most recent data is in MSB.

5. Resource Utilization (Ask a Question)

The following table shows the resource utilization of a sample SLVS-EC Receiver Core implemented in a PolarFire FPGA (MPF300TS-1FCG1152I package), for RAW 8 and four lanes and 1920 horizontal resolution configuration.

Table 5-1. Resource Utilization

Element	Usage
DFFs	3218
4-input LUTs	2155
LSRAMs	16

6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	10/2024	The following is the list of changes in revision A of the document: • The document was converted to Microchip template. • The document number was changed to DS50003779 from UG0877.
5.0	—	Added Table 3-4
4.0	—	• Replaced Figure 1-1, Figure 2-1, and Figure 4-1 • Removed section Transmit PLL • Updated Table 2-1, Table 3-2, Table 3-3, and Table 5-1 • Updated section PLL for Pixel Clock Generation • Updated section Configuration Parameters
3.0	—	• Introduction • Table 3-2
2.0	—	• Introduction • Transceiver Configuration • Table 3-2
1.0	—	Initial release

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