VSC8514

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8514 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8514 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "SerDes MAC Interface"
- Section 6.0, "Device Clocks"
- Section 7.0, "Digital Interface and I/O"
- Section 8.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8514 implementor should have the following documents on hand:

- *VSC8514-11 Quad-Port 10/100/1000BASE-T PHY with QSGMII MAC Data Sheet*
- VSC8514EV EVB documents, including the schematics, PCB file, BOM, and so on

The documents can be found at www.microchip.com/VSC8514 in the **Documents** tab under Board Design Files.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

3.0 POWER

Table 3-1 shows the power supply pins for VSC8514.

TABLE 3-1: POWER SUPPLY PINS

Name	Pin	Description	Comment
VDD1	E5, E7, E10, E13, E15, E17, E19, E21, E23, E25	1.0V Digital core power supply	Digital, no ferrite bead
VDD1A	E1, E11, E14, E16, E28, E30, E34, E36	1.0V Analog core power supply	Analog, use ferrite bead
VDD25	E3, E4, E6, E8, E12, E18, E20, E22, E24, E26	2.5V general digital power supply	Digital, no ferrite bead
VDD25A	E27, E29, E31, E33, E35, E37	2.5V general analog power supply	Analog, use ferrite bead
VDDMDIO	E9	1.2V or 2.5V power for SMI pins	Digital, no ferrite bead
VSS_CASE	Exposed pad, D9	Common device ground	—

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. Refer to Table 3-2. In system design, the current values in the table need an additional margin of 25-30%.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Power Rail	Voltage	Maximum Current
VDD1	1.0V	605 mA
VDD1A	1.0V	245 mA
VDD25	2.5V	10 mA
VDD25A	2.5V	560 mA
VDDMDIO	2.5V	4 mA

3.2 Power Supply Planes

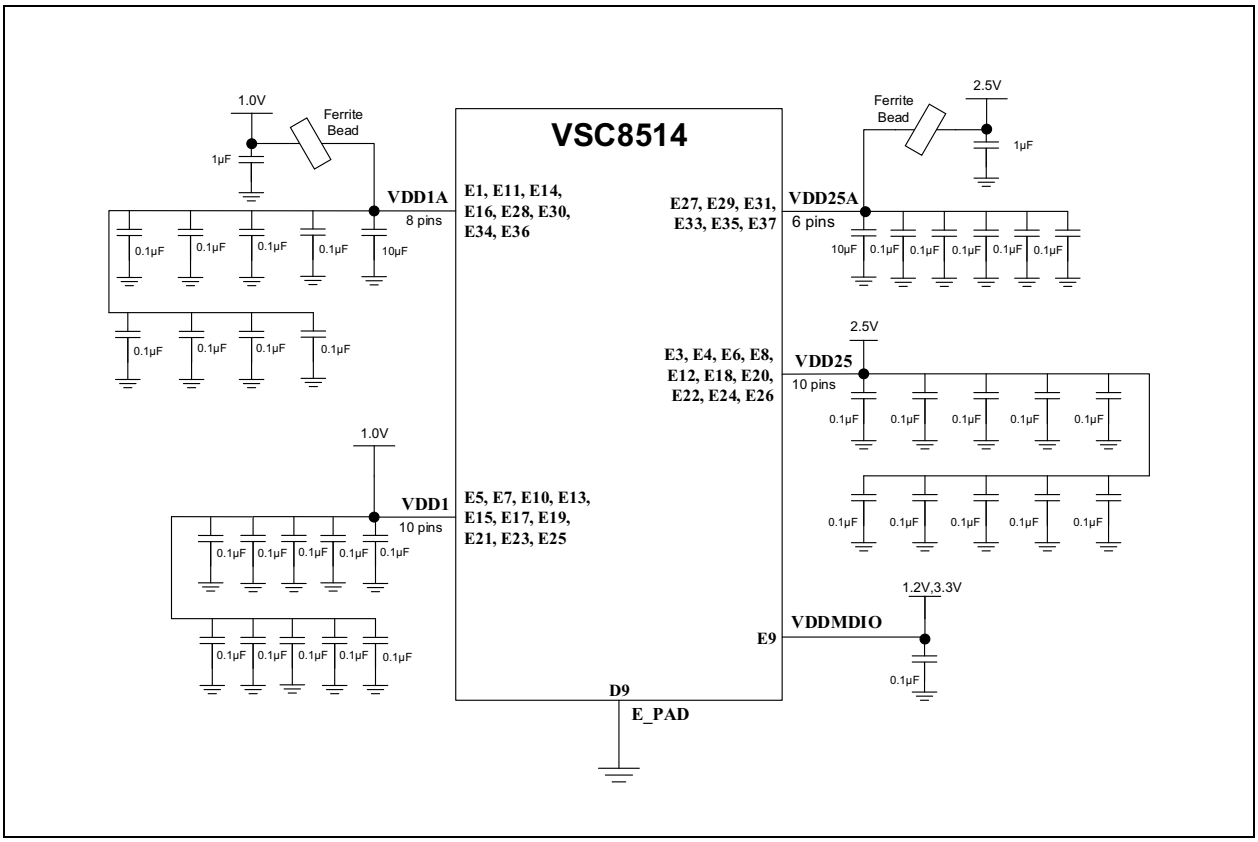
- The VSC8514 requires three power rails: 2.5V, 1.2V, and 1.0V when using 1.2V for VDDMDIO. It requires two power rails when using 2.5V for VDDMDIO. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are:
  - **VDD25A**
  - **VDD1A**
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended on digital supplies **VDD1**, **VDD25**, and **VDDMDIO**.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8514's power pins for every pin.
- Make sure that enough bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail.
- If the VSC8514 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 ETHERNET SIGNALS

4.1 10/100/1000 Mbps Interface Connection

The VSC8514 has four GPHY ports from PHY 0 to PHY 3 for port 1, port 2, port 3, and port 4. Detailed pin numbers from PHY 0 to PHY 3 sequence and descriptions as follows:

- **P[0:3]_D0N** (pins D30, B17, C32, and C36): These pins are the transmit/receive negative connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D0P** (pins D31, B18, C33, and C1): These pins are the transmit/receive positive connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D1N** (pins C24, C28, B19, and D34): These pins are the transmit/receive negative connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D1P** (pins C25, C29, B20, and D35): These pins are the transmit/receive positive connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D2N** (pins C23, B15, A9, and C34): These pins are the transmit/receive negative connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D2P** (pins D29, B16, A10, and C35): These pins are the transmit/receive positive connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D3N** (pins C21, C26, C30, and D32): These pins are the transmit/receive negative connection from Pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:3]_D3P** (pins C22, C27, C31, and D33): These pins are the transmit/receive positive connection from Pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

There are two 10/100/1000 Mbps channel connection solutions: (1) Solution #1 is for an external environment with no electrical noise and no ESD to be considered (see Figure 4-1), and (2) Solution #2 is for an external environment with electrical noise and with ESD to be considered (see Figure 4-2).

FIGURE 4-1: SOLUTION #1 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS

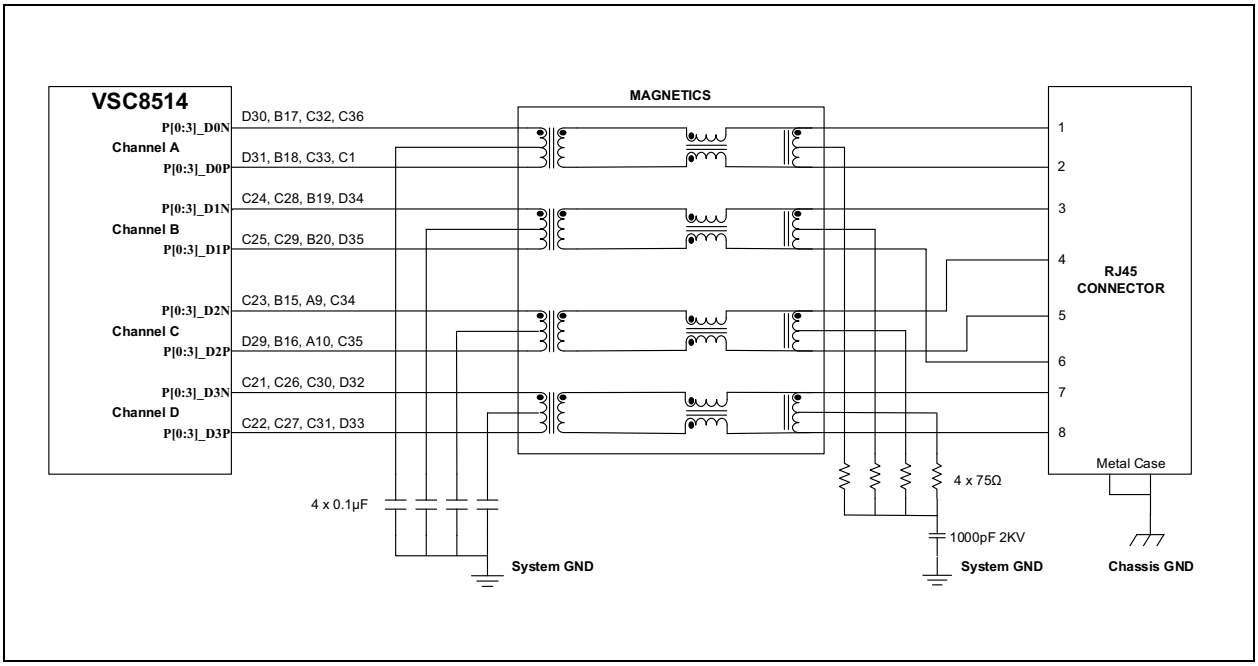
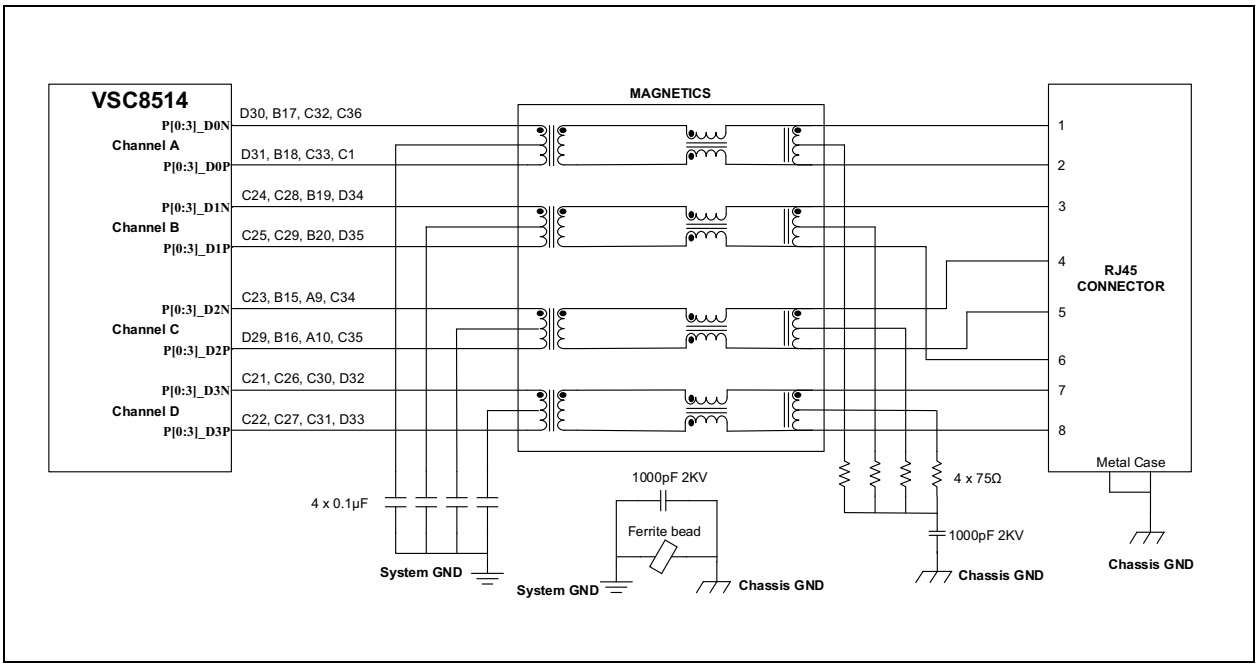


FIGURE 4-2: SOLUTION #2 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection and RJ45 Connection

- The center tap connection on the VSC8514 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8514 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8514 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8514 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetics should not be connected together without the 0.1 µF capacitor to GND. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground, it is shared by PHY 0, PHY 1, PHY 2, and PHY 3 for port 1, port 2, port 3, and port 4.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, "PCB Layout Considerations" for guidance on how chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on Microchip Technology product page) for reference.

4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss requiring the PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of pairs A, B, C, and D should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8514 device or other sensitive devices in the PCB layout placement for better ESD.

5.0 SERDES MAC INTERFACE

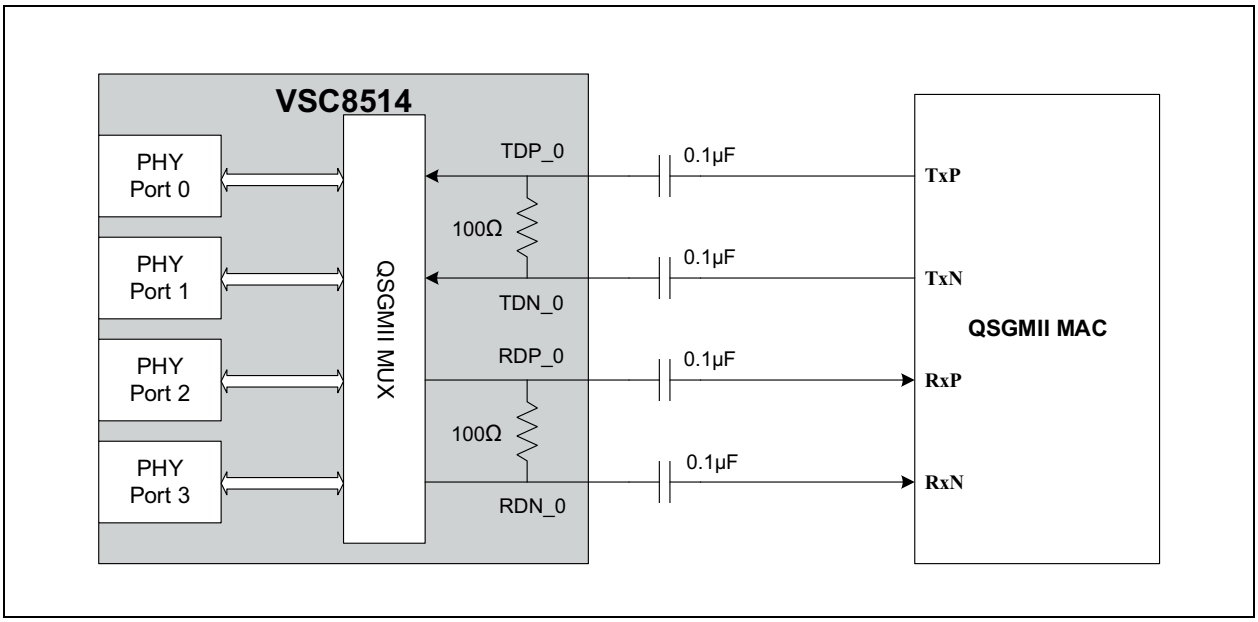
5.1 QSGMII MAC

- The VSC8514 device supports a QSGMII MAC to convey four ports of network data and port speed between 10BASE-T, 100BASE-TX, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. The MAC interface protocol for each port within QSGMII can be either 1000BASE-X or SGMII, if the QSGMII MAC which the VSC8514 is connecting to supports this functionality. The device also supports SGMII MAC-side auto-negotiation on each individual port, enabled through register 16E3, bit 7 of that port.
- For the detailed pins numbers and descriptions and QSGMII interface connection, see Table 5-1 and Figure 5-1.

TABLE 5-1: QSGMII INTERFACE PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
RDN_0	D13	Output	QSGMII MAC receiver output pair
RDP_0	D14	Output	
TDN_0	D15	Input	QSGMII MAC transmitter input pair
TDP_0	D16	Input	

FIGURE 5-1: QSGMII MAC INTERFACE CONNECTIONS



5.2 MAC SerDes Design Rules

- Use AC coupling with 0.1 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between SerDes pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.

6.0 DEVICE CLOCKS

6.1 Reference Clock

The device reference clock supports 125 MHz and 156.25 MHz compliant clock signals. The clock signal must be capacitively coupled and LVDS-compliant.

- **REFCLK_P/REFCLK_N** (pin D11/D12) is the reference clock differential input, which must be capacitor AC-coupled between the clock source and the VSC8514 device.
- **REFCLK_SEL0/REFCLK_SEL1** (pin B8/B7) is the reference clock frequency select signal.
- The VSC8514 supports multiple reference clock input options through the strap pins (B7, B8) of **REFCLK_SEL [1:0]** to select system clock frequency. See Table 6-1 for details on strap options.

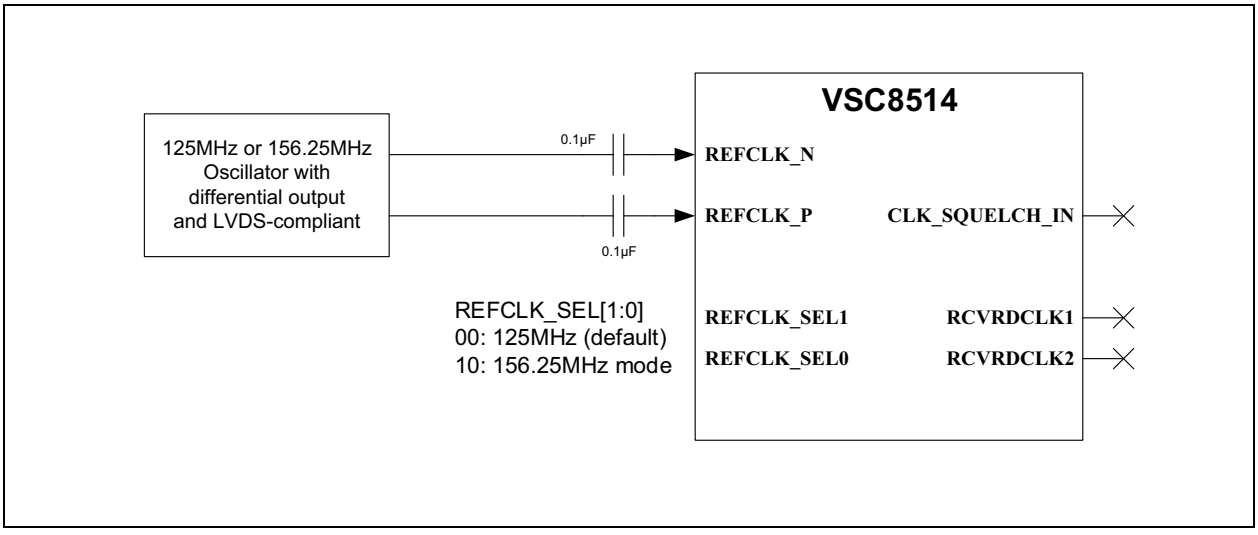
TABLE 6-1: REFCLK FREQUENCY SELECTION

REFCLK_SEL [1:0]	Clock Frequency	Used Pins
00	125 MHz	REFCLK_N/REFCLK_P
10	156.25 MHz	REFCLK_N/REFCLK_P

When reference clocks are used, ensure that:

- The jitter requirements in the data sheet are met.
- The amplitude specifications in the data sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 µF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC8514 side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- Unused reference clocks can be left floating (No Connect). See Figure 6-1.

FIGURE 6-1: REFERENCE CLOCK FOR NON-SYNCE

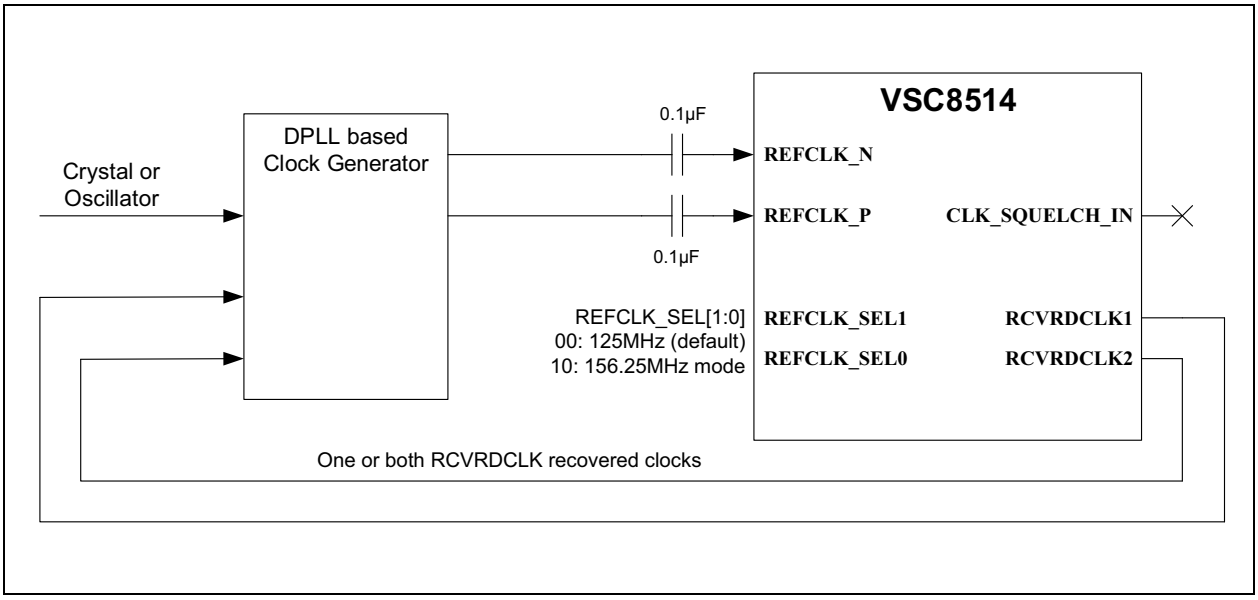


6.2 Media Recovered Clock Output

For Synchronous Ethernet applications, the VSC8514 includes two recovered clock output pins.

- **RCVRDCLK1** (pin B13) is controlled by register 23G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
- **RCVRDCLK2** (pin C20) is controlled by register 24G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
  - To enable recovered clock output, set register 23G or 24G, bit 15 to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 125 MHz), and squelch conditions.
- **CLK_SQUELCH_IN** (pin B7) is the input control to squelch the recovered clock. Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. The **CLK_SQUELCH_IN** pin controls the squelching of the clock. Both **RCVRDCLK1** and **RCVRDCLK2** are squelched when the **CLK_SQUELCH_IN** pin is high.
- For using Synchronous Ethernet applications, see Figure 6-2 for reference.

FIGURE 6-2: TYPICAL SYNCHRONOUS ETHERNET CLOCK CONFIGURATION



7.0 DIGITAL INTERFACE AND I/O

7.1 Serial Management Interface (SMI) Pins

- The VSC8514 device includes an IEEE 802.3-compliant serial management interface (SMI) that is controlled by its **MDC**, **MDIO**, and **MDINT** pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.
- Energy Efficient Ethernet (EEE) control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For information about available register settings, see the "MMD EEE Access, Address 13 (0x0D)" table and the "Clause 45 Registers Page Space" table in the *VSC8514 Data Sheet*.
- The SMI is a synchronous serial interface with input data to the VSC8514 on the MDIO pin that is clocked on the rising edge of the **MDC** pin. The output data is sent on the **MDIO** pin on the rising edge of the MDC signal. The interface can be clocked at a rate from minimum kHz, typical 2.5 MHz to maximum 12.5 MHz, depending on the total load on MDIO. An external 2 kΩ pull-up resistor is recommended on the **MDIO** pin when using maximum 12.5 MHz MDC clock. If using 2.5 MHz or less MDC frequency, it is acceptable to use 10 kΩ pull-up resistor for the **MDIO** pin. See Table 7-1 for SMI interface pin numbers and more information.

TABLE 7-1: SMI INTERFACE PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
MDC	C11	I, PD	A maximum of 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	D10	I/O, OD	Serial data is written or read from this pin bidirectionally between the PHY and the station manager synchronously on the positive edge of MDC. One external pull-up resistor is required. The pull-up resistor should be tied to the VDDMDIO power, and its value depends on the MDC clock frequency.
MDINT	C10	I/O, OD, OS	This pin is the Management interrupt signal. This output is open-drain and requires an external pull-up resistor. It may be wired-OR with other open-drain interrupt signals. If MDINT is unused, it may be left unconnected, without a resistor.

7.2 GPIO Pins

- VSC8514 provides 15 multiplexed general-purpose input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers. Table 7-2 shows an overview of the register controls for GPIO pins.
- These GPIO pins have internal pull-up (PU). Any unused GPIO pins can be left floating (No Connect).

TABLE 7-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Note
GPIO_0	D19	13G [1:0]	15G.0	16G.0	17G.0	Default
GPIO_1	C14	13G [3:2]	15G.1	16G.1	17G.1	—
GPIO_2	D20	13G [5:4]	15G.2	16G.2	17G.2	—
GPIO_3	C15	13G [7:6]	15G.3	16G.3	17G.3	—
GPIO_4	B9	13G [9:8]	15G.4	16G.4	17G.4	—
GPIO_5	C16	13G [11:10]	15G.5	16G.5	17G.5	—
GPIO_6	D21	13G [13:12]	15G.6	16G.6	17G.6	—
GPIO_7	B10	13G [15:14]	15G.7	16G.7	17G.7	—
GPIO_8	C17	14G [1:0]	15G.8	16G.8	17G.8	—

Note 1: For all GPIO-related register bits in the table, defaults are '0' or '00', and write '1' or '11' is valid.

TABLE 7-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL (CONTINUED)

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Note
GPIO_9	D22	14G [3:2]	15G.9	16G.9	17G.9	Also used to output the FASTLINK_FAIL signal
GPIO_10	D24	14G [5:4]	15G.10	16G.10	17G.10	—
GPIO_11	D23	14G [7:6]	15G.11	16G.11	17G.11	—
GPIO_12	C18	14G [15:14]	15G.12	16G.12	17G.12	—
GPIO_13	B11	14G [15:14]	15G.13	16G.13	17G.13	—
GPIO_14	D25	14G [15:14]	15G.14	16G.14	17G.14	—

Note 1: For all GPIO-related register bits in the table, defaults are ‘0’ or ‘00’, and write ‘1’ or ‘11’ is valid.

7.3 JTAG Pins

- If JTAG is not used, $\overline{\text{TRST}}$ should be pulled low. The other pins may be left floating (No Connect). See Table 7-3 for JTAG pin information.

TABLE 7-3: JTAG PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
TCK	B6	I, PU	Boundary scan, test clock input. Internally pulled high.
TDI	C9	I, PU	Boundary scan, test data input. Internally pulled high.
TDO	C8	O	Boundary scan, test data output
TMS	A3	I, PU	Boundary scan, test mode select. Internally pulled high.
TRST	C7	I, PU	Boundary scan, test Reset input. Internally pulled high. **Note:** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation.

8.0 MISCELLANEOUS

8.1 Reset

- The VSC8514 must be reset at power-up. One option is to hold **NRESET** low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **NRESET** low for a minimum 2 ms after power up. **NRESET** is typically driven by a voltage monitor device or by the management processor or FPGA. See Table 8-1 for more information on the reference clocks.

TABLE 8-1: RESET PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
NRESET	B5	I	Reset. Active low input that powers down the device and sets all register bits to their default state.

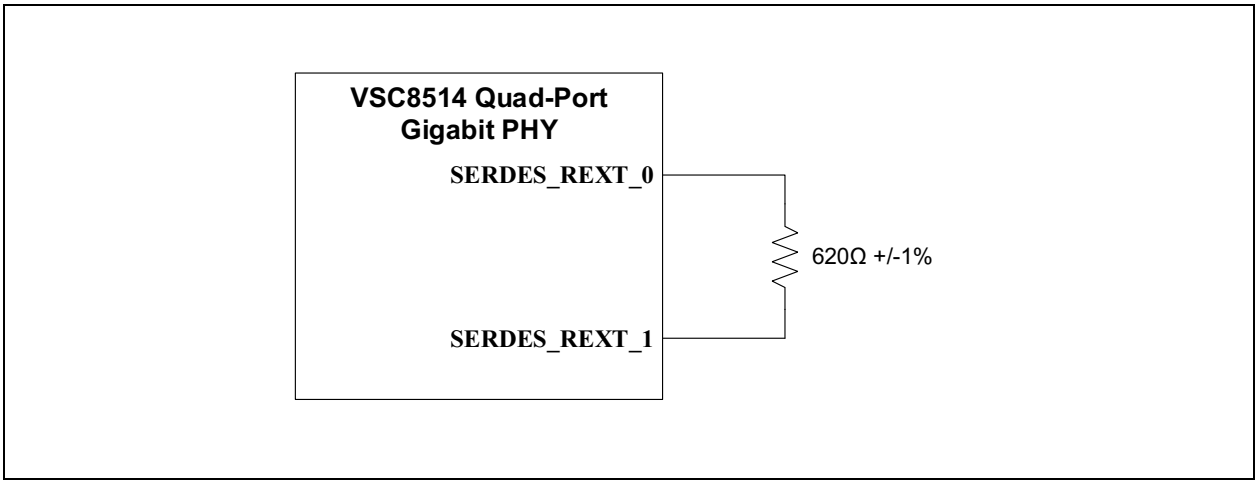
8.2 Reference Resistor

- Connect a 620Ω ±1% resistor between **SERDES_REXT_0** and **SERDES_REXT_1** as shown in Figure 8-1. See Table 8-2 for additional details on the pins.

TABLE 8-2: REFERENCE RESISTORS DESCRIPTIONS

Pin Name	Pin Number	Level	Description
SERDES_REXT_0	D17	Analog	SerDes bias pins. Connect to a 620Ω 1% resistor.
SERDES_REXT_1	D18	Analog	

FIGURE 8-1: SERDES BIAS RESISTOR



8.3 LED Pins

- The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits [13:10]. The default polarity is active low. The register 25G, register 29 and 30 can be configured for different LED modes.
- The VSC8514 LED pins are for quad-port status, refer to Table 8-3 for all indicator LED pins.
- Using 330Ω to 510Ω current limit resistor is recommended and VDD25 for LED power.

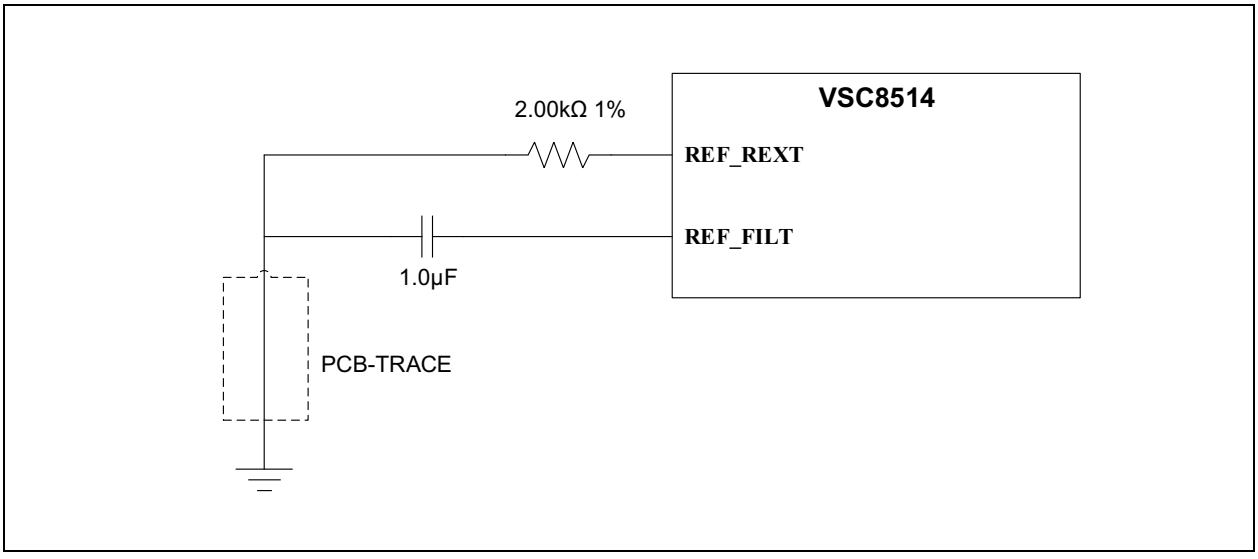
TABLE 8-3: LED PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
LED0_PHY [0:3]	E2, C3, C5, B4	O	PHY 0, Port 1 LEDs, LED direct-drive outputs. All LED pins are active-low.
LED1_PHY [0:3]	D1, B2, D5, C6	O	PHY 1, Port 2 LEDs, LED direct-drive outputs. All LED pins are active-low.
LED2_PHY [0:3]	D2, C4, B3, A2	O	PHY 2, Port 3 LEDs, LED direct-drive outputs. All LED pins are active-low.
LED3_PHY [0:3]	C2, D4, D6, D7	O	PHY 3, Port 4 LEDs, LED direct-drive outputs. All LED pins are active-low.

8.4 Analog Bias Pins

- The **REF_REXT** pin (pin A8) on the VSC8514 device should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0% and minimum 1/16W. This pin is used to set up critical bias currents for the Ethernet physical device.
- The **REF_FILT** pin (pin A7) on the VSC8514 device should connect to the system ground through a 1 µF capacitor with 10% tolerance; NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in Figure 8-2. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8514.

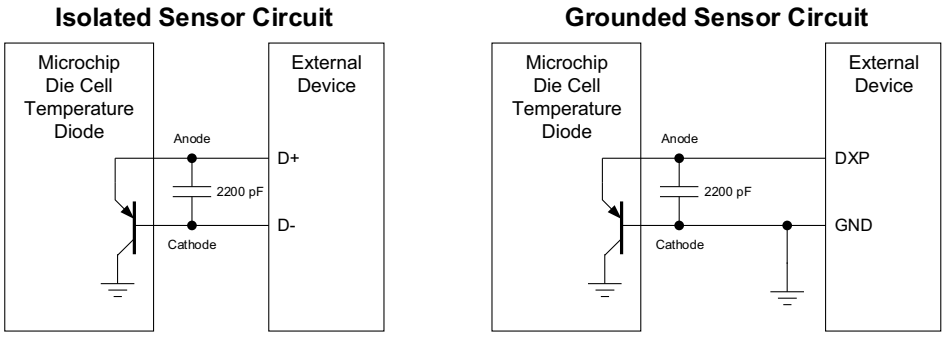
FIGURE 8-2: VOLTAGE REFERENCE SCHEMATIC



8.5 Temperature Sensor Diode

- The temperature sensor diode pins provide access to an on-die diode and internal circuitry for monitoring die temperature. To use it, connect an external thermal sensor located on the board or in a stand-alone measurement kit. The feature can be as an option in application.
- The **THERMDA** pin (pin B1) is the Thermal Diode Anode pin, which needs to be pulled down by a pull-down resistor if not used.
- The **THERMDC_VSS** pin (pin D3) is the Thermal Diode Cathode pin connected to system ground. The temperature sensor must be chosen accordingly. This pin needs to be pulled down by a pull-down resistor if not used.
- Temperature measurement using a thermal diode is very sensitive to noise. Figure 8-3 illustrates a generic application design.

FIGURE 8-3: THERMAL DIODE CONNECTIONS



Note: Microchip does not support or recommend operation of the thermal diode under reverse bias.

8.6 PHY Address Pins

- The VSC8514 device includes three external PHY address pins, **PHYADD [4:2]**, to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9. See Table 8-4 for more information on the PHY address.

TABLE 8-4: PHY ADDRESS PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
PHYADD2	C19	I, PD	PHYADD [4:2] for access each PHY's registers through SMI interface.
PHYADD3	B12	I, PD	
PHYADD4	D26	I, PD	

8.7 Other Pins

- The **COMA_MODE** (pin D8) provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of reset. Hence, this pin should be pulled down by a pull-down resistor.
- The **FASTLINK_FAIL** (pin D22) provides a Fast Link Failure indication signal. If this feature is not used, this pin **FASTLINK_FAIL/GPIO_9** can be floating.

8.8 Unused and No Connection Pins

- The **RESERVED_[1:4]** pins (pins C12, C13, D28, and B14) are reserved signals. Leave them unconnected.
- The **NC_[1:4]** pins (pins A1, A4, A5, and A6) are unconnected pins. Leave them floating.

8.9 General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 kΩ resistor is recommended to use.
- If there is no pull-down resistor value specified, a 1 kΩ or 4.7 kΩ resistor is recommended to use.

NOTES:

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.0, "Power", Section 3.1, "Current Requirements"	Refer to Table 3-1 and Table 3-2 to ensure that the power pins are correct. Select the correct power supply components with at least about 25-30% margin for the system power consumption.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection and filtering.		
	Section 3.4, "Decoupling Capacitors"	If doing a PCB layout, see this section for the bulk decoupling capacitor required.		
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pins connection for quad-port circuit design based on product design requirement to select the design according to Figure 4-1 or Figure 4-2.		
	Section 4.2, "10/100/1000 Magnetics Connection and RJ45 Connection"	Verify the magnetics and the common-mode capacitors connection based on Figure 4-1 or Figure 4-2.		
	Section 4.3, "PCB Layout Considerations"	Refer to this section for PCB layout design reference to check if the Gigabit copper port PCB layout request is met.		
Section 5.0, "SerDes MAC Interface"	Section 5.1, "QSGMII MAC"	Refer to Table 5-1 and Figure 5-1 to check if the QSGMII MAC interface design with output and input connection is correct.		
	Section 5.2, "MAC SerDes Design Rules"	For SerDes QSGMII MAC interface PCB layout, follow the SerDes design rules requirement in this partial PCB layout.		
Section 6.0, "Device Clocks"	Section 6.1, "Reference Clock"	Refer to Table 6-1 and Figure 6-1 to select the reference clock frequency and the correct reference clock circuit design and connection. Follow the layout required in the PCB design.		
	Section 6.2, "Media Recovered Clock Output"	Refer to Figure 6-2 for a typical recovered clock circuit design and for the correct recovered clock pins and configuration to use.		
Section 7.0, "Digital Interface and I/O"	Section 7.1, "Serial Management Interface (SMI) Pins"	Refer to Table 7-1 and the descriptions in this section for SMI interface circuit design.		
	Section 7.2, "GPIO Pins"	Refer to Table 7-2 and the descriptions in this section for all GPIO pins in the circuit design.		
	Section 7.3, "JTAG Pins"	Refer to Table 7-3 and the descriptions in this section for all JTAG pins in the circuit design.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Miscellaneous"	Section 8.1, "Reset"	Check if the designed reset circuit meets the reset time requirement.		
	Section 8.2, "Reference Resistor"	Make sure to connect a 620Ω ±1% resistor between the **RERDES_REXT_0** and **RERDES_REXT_1** pins.		
	Section 8.3, "LED Pins"	Check if correct LED pins are used based on Table 8-3, current limit resistors, and LED power.		
	Section 8.4, "Analog Bias Pins"	Check if the correct pull-down resistor value for **REF_REXT** pin is used. Check if the correct pull-down capacitor value for **REF_FILT** pin is used.		
	Section 8.5, "Temperature Sensor Diode"	If designing with the temperature sensor diode, see Figure 8-3 as the design reference.		
	Section 8.6, "PHY Address Pins"	Check if the correct PHY address pins are used based on Table 8-4 to configure the correct PHY address the design requires.		
	Section 8.7, "Other Pins"	For **COMA_MODE** and **FASTLINK_FAIL** pins, check this section for the correct design.		
	Section 8.8, "Unused and No Connection Pins"	Verify all reserved pins and NC pins are unconnected.		
	Section 8.9, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003985A (05-26-21)	Initial release	

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